Offset: 0x00CC			Register Name: IOMMU_DM_AUT_CTRL7_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
19	R/W	0x0	DM15_M1_WT_AUT_CTRL Domain15 write permission control for master1 0: The write-operation is permitted 1: The write-operation is prohibited
18	R/W	0x0	DM15_M1_RD_AUT_CTRL Domain15 read permission control for master1 0: The read-operation is permitted 1: The read-operation is prohibited
17	R/W	0x0	DM15_M0_WT_AUT_CTRL Domain15 write permission control for master0 0: The write-operation is permitted 1: The write-operation is prohibited
16	R/W	0x0	DM15_M0_RD_AUT_CTRL Domain15 read permission control for master0 0: The read-operation is permitted 1: The read-operation is prohibited
15:14	/	/	/
13	R/W	0x0	DM14_M6_WT_AUT_CTRL Domain14 write permission control for master6 0: The write-operation is permitted 1: The write-operation is prohibited **Note: The bit is not used.**
12	R/W	0x0	DM14_M6_RD_AUT_CTRL Domain14 read permission control for master6 0: The read-operation is permitted 1: The read-operation is prohibited **Note: The bit is not used.**
11	R/W	0x0	DM14_M5_WT_AUT_CTRL Domain14 write permission control for master5 0: The write-operation is permitted 1: The write-operation is prohibited
10	R/W	0x0	DM14_M5_RD_AUT_CTRL Domain14 read permission control for master5 0: The read-operation is permitted 1: The read-operation is prohibited
9	R/W	0x0	DM14_M4_WT_AUT_CTRL

Offset: 0x00CC			Register Name: IOMMU_DM_AUT_CTRL7_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			Domain14 write permission control for master4 0: The write-operation is permitted 1: The write-operation is prohibited
8	R/W	0x0	DM14_M4_RD_AUT_CTRL Domain14 read permission control for master4 0: The read-operation is permitted 1: The read-operation is prohibited
7	R/W	0x0	DM14_M3_WT_AUT_CTRL Domain14 write permission control for master3 0: The write-operation is permitted 1: The write-operation is prohibited
6	R/W	0x0	DM14_M3_RD_AUT_CTRL Domain14 read permission control for master3 0: The read-operation is permitted 1: The read-operation is prohibited
5	R/W	0x0	DM14_M2_WT_AUT_CTRL Domain14 write permission control for master2 0: The write-operation is permitted 1: The write-operation is prohibited
4	R/W	0x0	DM14_M2_RD_AUT_CTRL Domain14 read permission control for master2 0: The read-operation is permitted 1: The read-operation is prohibited
3	R/W	0x0	DM14_M1_WT_AUT_CTRL Domain14 write permission control for master1 0: The write-operation is permitted 1: The write-operation is prohibited
2	R/W	0x0	DM14_M1_RD_AUT_CTRL Domain14 read permission control for master1 0: The read-operation is permitted 1: The read-operation is prohibited
1	R/W	0x0	DM14_M0_WT_AUT_CTRL Domain14 write permission control for master0 0: The write-operation is permitted 1: The write-operation is prohibited
0	R/W	0x0	DM14_M0_RD_AUT_CTRL

Offset: 0x00CC			Register Name: IOMMU_DM_AUT_CTRL7_REG
Bit	Read/Write	Default/Hex	Description
			Domain14 read permission control for master0 0: The read-operation is permitted 1: The read-operation is prohibited

3.11.6.31 0x00D0 IOMMU Domain Authority Overwrite Register (Default Value: 0x0000_0000)

Setting the REG_ARD_OVWT can mask the Domain control defined by IOMMU_DM_AUT_CTRL_REG0–7. All the property of Level2 are covered by the property defined in REG_ARD_OVWT. Allow read and write for all by default.

Offset: 0x00D0			Register Name: IOMMU_DM_AUT_OVWT_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DM_AUT_OVWT_ENABLE Domain write/read permission overwrite enable 0: Disable 1: Enable
30:14	/	/	/
13	R/W	0x0	M6_WT_AUT_OVWT_CTRL Master6 write permission overwrite control 0: The write-operation is permitted 1: The write-operation is prohibited **Note: The bit is not used.**
12	R/W	0x0	M6_RD_AUT_OVWT_CTRL Master6 read permission overwrite control 0: The read-operation is permitted 1: The read-operation is prohibited **Note: The bit is not used.**
11	R/W	0x0	M5_WT_AUT_OVWT_CTRL Master5 write permission overwrite control 0: The write-operation is permitted 1: The write-operation is prohibited
10	R/W	0x0	M5_RD_AUT_OVWT_CTRL Master5 read permission overwrite control 0: The read-operation is permitted 1: The read-operation is prohibited
9	R/W	0x0	M4_WT_AUT_OVWT_CTRL Master5 write permission overwrite control

Offset: 0x00D0			Register Name: IOMMU_DM_AUT_OVWT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: The write-operation is permitted 1: The write-operation is prohibited
8	R/W	0x0	M4_RD_AUT_OVWT_CTRL Master5 read permission overwrite control 0: The read-operation is permitted 1: The read-operation is prohibited
7	R/W	0x0	M3_WT_AUT_OVWT_CTRL Master3 write permission overwrite control 0: The write-operation is permitted 1: The write-operation is prohibited
6	R/W	0x0	M3_RD_AUT_OVWT_CTRL Master3 read permission overwrite control 0: The read-operation is permitted 1: The read-operation is prohibited
5	R/W	0x0	M2_WT_AUT_OVWT_CTRL Master2 write permission overwrite control 0: The write-operation is permitted 1: The write-operation is prohibited
4	R/W	0x0	M2_RD_AUT_OVWT_CTRL Master2 read permission overwrite control 0: The read-operation is permitted 1: The read-operation is prohibited
3	R/W	0x0	M1_WT_AUT_OVWT_CTRL Master1 write permission overwrite control 0: The write-operation is permitted 1: The write-operation is prohibited
2	R/W	0x0	M1_RD_AUT_OVWT_CTRL Master1 read permission overwrite control 0: The read-operation is permitted 1: The read-operation is prohibited
1	R/W	0x0	M0_WT_AUT_OVWT_CTRL Master0 write permission overwrite control 0: The write-operation is permitted 1: The write-operation is prohibited
0	R/W	0x0	M0_RD_AUT_OVWT_CTRL Master0 read permission overwrite control

Offset: 0x00D0			Register Name: IOMMU_DM_AUT_OVWT_REG
Bit	Read/Write	Default/Hex	Description
			0: The read-operation is permitted 1: The read-operation is prohibited

3.11.6.32 0x0100 IOMMU Interrupt Enable Register (Default Value: 0x0000_0000)

Invalid page table and permission error can not make one device or multi-devices in system work normally.

Permission error usually happens in MicroTLB. The error generates interrupt and waits for processing through software.

Invalid page table usually happens in MacroTLB. The error can not influence the access of other devices. So the error page table needs go back the way it comes, but the error should not be written in each level TLB.

Offset: 0x0100			Register Name: IOMMU_INT_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20	R/W	0x0	DBG_PF_L2_IV_PT_EN. Debug or Prefetch Invalid Page Table Enable 0: Mask interrupt 1: Enable interrupt
19	R/W	0x0	DBG_PF_PC_IV_L1_PT_EN. Debug or Prefetch PTW Cache Invalid Level1 Page Table Enable 0: Mask interrupt 1: Enable interrupt
18	R/W	0x0	DBG_PF_DRAM_IV_L1_PT_EN. Debug or Prefetch DRAM Invalid Level1 Page Table Enable 0: Mask interrupt 1: Enable interrupt
17	R/W	0x0	L2_PAGE_TABLE_INVALID_EN Level2 page table invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
16	R/W	0x0	L1_PAGE_TABLE_INVALID_EN Level1 page table invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
15:7	/	/	/
6	R/W	0x0	MICRO_TLB6_INVALID_EN

Offset: 0x0100			Register Name: IOMMU_INT_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
			Micro TLB6 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
5	R/W	0x0	MICRO_TLB5_INVALID_EN Micro TLB5 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
4	R/W	0x0	MICRO_TLB4_INVALID_EN Micro TLB4 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
3	R/W	0x0	MICRO_TLB3_INVALID_EN Micro TLB3 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
2	R/W	0x0	MICRO_TLB2_INVALID_EN Micro TLB2 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
1	R/W	0x0	MICRO_TLB1_INVALID_EN Micro TLB1 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
0	R/W	0x0	MICRO_TLB0_INVALID_EN Micro TLB0 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt

3.11.6.33 0x0104 IOMMU Interrupt Clear Register (Default Value: 0x0000_0000)

Offset: 0x0104			Register Name: IOMMU_INT_CLR_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	W	0x0	L2_PAGE_TABLE_INVALID_CLR Level2 page table invalid interrupt clear bit 0: Invalid operation

Offset: 0x0104			Register Name: IOMMU_INT_CLR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			1: Clear interrupt
16	W	0x0	L1_PAGE_TABLE_INVALID_CLR Level1 page table invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
15:7	/	/	/
6	W	0x0	MICRO_TLB6_INVALID_CLR Micro TLB6 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt **Note: The bit is not used.**
5	W	0x0	MICRO_TLB5_INVALID_CLR Micro TLB5 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
4	W	0x0	MICRO_TLB4_INVALID_CLR Micro TLB4 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
3	W	0x0	MICRO_TLB3_INVALID_CLR Micro TLB3 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
2	W	0x0	MICRO_TLB2_INVALID_CLR Micro TLB2 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
1	W	0x0	MICRO_TLB1_INVALID_CLR Micro TLB1 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
0	W	0x0	MICRO_TLB0_INVALID_CLR Micro TLB0 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt

3.11.6.34 0x0108 IOMMU Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0108			Register Name: IOMMU_INT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R	0x0	L2_PAGE_TABLE_INVALID_STA Level2 page table invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
16	R	0x0	L1_PAGE_TABLE_INVALID_STA Level1 page table invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
15:7	/	/	/
6	R	0x0	MICRO_TLB6_INVALID_STA Micro TLB6 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens **Note: The bit is not used.**
5	R	0x0	MICRO_TLB5_INVALID_STA Micro TLB5 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
4	R	0x0	MICRO_TLB4_INVALID_STA Micro TLB4 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
3	R	0x0	MICRO_TLB3_INVALID_STA Micro TLB3 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
2	R	0x0	MICRO_TLB2_INVALID_STA Micro TLB2 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
1	R	0x0	MICRO_TLB1_INVALID_STA Micro TLB1 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens

Offset: 0x0108			Register Name: IOMMU_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
0	R	0x0	MICRO_TLB0_INVALID_STA Micro TLB0 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens

3.11.6.35 0x0110 IOMMU Interrupt Error Address 0 Register (Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: IOMMU_INT_ERR_ADDR0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR0 Virtual address that caused Micro TLB0 to interrupt

3.11.6.36 0x0114 IOMMU Interrupt Error Address 1 Register (Default Value: 0x0000_0000)

Offset: 0x0114			Register Name: IOMMU_INT_ERR_ADDR1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR1 Virtual address that caused Micro TLB1 to interrupt

3.11.6.37 0x0118 IOMMU Interrupt Error Address 2 Register (Default Value: 0x0000_0000)

Offset: 0x0118			Register Name: IOMMU_INT_ERR_ADDR2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR2 Virtual address that caused Micro TLB2 to interrupt

3.11.6.38 0x011C IOMMU Interrupt Error Address 3 Register (Default Value: 0x0000_0000)

Offset: 0x011C			Register Name: IOMMU_INT_ERR_ADDR3_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR3 Virtual address that caused Micro TLB3 to interrupt

3.11.6.39 0x0120 IOMMU Interrupt Error Address 4 Register (Default Value: 0x0000_0000)

Offset: 0x0120			Register Name: IOMMU_INT_ERR_ADDR4_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR4 Virtual address that caused Micro TLB4 to interrupt

3.11.6.40 0x0124 IOMMU Interrupt Error Address 5 Register (Default Value: 0x0000_0000)

Offset: 0x0124			Register Name: IOMMU_INT_ERR_ADDR5_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR5 Virtual address that caused Micro TLB5 to interrupt

3.11.6.41 0x0128 IOMMU Interrupt Error Address 6 Register (Default Value: 0x0000_0000)

Offset: 0x0128			Register Name: IOMMU_INT_ERR_ADDR6_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR6 Virtual address that caused Micro TLB6 to interrupt

3.11.6.42 0x0130 IOMMU Interrupt Error Address 7 Register (Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: IOMMU_INT_ERR_ADDR7_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR7 Virtual address that caused L1 page table to interrupt

3.11.6.43 0x0134 IOMMU Interrupt Error Address 8 Register (Default Value: 0x0000_0000)

Offset: 0x0134			Register Name: IOMMU_INT_ERR_ADDR8_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR8 Virtual address that caused L2 page table to interrupt

3.11.6.44 0x0150 IOMMU Interrupt Error Data 0 Register (Default Value: 0x0000_0000)

Offset: 0x0150			Register Name: IOMMU_INT_ERR_DATA0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA0 Corresponding page table of virtual address that caused Micro TLB0 to interrupt

3.11.6.45 0x0154 IOMMU Interrupt Error Data 1 Register (Default Value: 0x0000_0000)

Offset: 0x0154			Register Name: IOMMU_INT_ERR_DATA1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA1 Corresponding page table of virtual address that caused Micro TLB1 to interrupt

3.11.6.46 0x0158 IOMMU Interrupt Error Data 2 Register (Default Value: 0x0000_0000)

Offset: 0x0158			Register Name: IOMMU_INT_ERR_DATA2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA2 Corresponding page table of virtual address that caused Micro TLB2 to interrupt

3.11.6.47 0x015C IOMMU Interrupt Error Data 3 Register (Default Value: 0x0000_0000)

Offset: 0x015C			Register Name: IOMMU_INT_ERR_DATA3_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA3 Corresponding page table of virtual address that caused Micro TLB3 to interrupt

3.11.6.48 0x0160 IOMMU Interrupt Error Data 4 Register (Default Value: 0x0000_0000)

Offset: 0x0160			Register Name: IOMMU_INT_ERR_DATA4_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA4 Corresponding page table of virtual address that caused Micro TLB4 to interrupt

3.11.6.49 0x0164 IOMMU Interrupt Error Data 5 Register (Default Value: 0x0000_0000)

Offset: 0x0164			Register Name: IOMMU_INT_ERR_DATA5_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA5 Corresponding page table of virtual address that caused Micro TLB5 to interrupt

3.11.6.50 0x0168 IOMMU Interrupt Error Data 6 Register (Default Value: 0x0000_0000)

Offset: 0x0168			Register Name: IOMMU_INT_ERR_DATA6_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA6 Corresponding page table of virtual address that caused Micro TLB6 to interrupt **Note: This field is not used.**

3.11.6.51 0x0170 IOMMU Interrupt Error Data 7 Register (Default Value: 0x0000_0000)

Offset: 0x0170			Register Name: IOMMU_INT_ERR_DATA7_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA7 Corresponding page table of virtual address that caused L1 page table to interrupt

3.11.6.52 0x0174 IOMMU Interrupt Error Data 8 Register (Default Value: 0x0000_0000)

Offset: 0x0174			Register Name: IOMMU_INT_ERR_DATA8_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA8 Corresponding page table of virtual address that caused L2 page table to interrupt

3.11.6.53 0x0180 IOMMU L1 Page Table Interrupt Register (Default Value: 0x0000_0000)

Offset: 0x0180			Register Name: IOMMU_L1PG_INT_REG
Bit	Read/Write	Default/Hex	Description
31	R	0x0	DBG_MODE_L1PG_INT Debug mode address switch causes L1 page table to occur interrupt.
30:7	/	/	/
6	R	0x0	MASTER6_L1PG_INT Master6 address switch causes L1 page table to occur interrupt. **Note: The bit is not used.**
5	R	0x0	MASTER5_L1PG_INT Master5 address switch causes L1 page table to occur interrupt.
4	R	0x0	MASTER4_L1PG_INT Master4 address switch causes L1 page table to occur interrupt.
3	R	0x0	MASTER3_L1PG_INT Master3 address switch causes L1 page table to occur interrupt.
2	R	0x0	MASTER2_L1PG_INT Master2 address switch causes L1 page table to occur interrupt.
1	R	0x0	MASTER1_L1PG_INT Master1 address switch causes L1 page table to occur interrupt.
0	R	0x0	MASTER0_L1PG_INT Master0 address switch causes L1 page table to occur interrupt.

3.11.6.54 0x0184 IOMMU L2 Page Table Interrupt Register (Default Value: 0x0000_0000)

Offset: 0x0184			Register Name: IOMMU_L2PG_INT_REG
Bit	Read/Write	Default/Hex	Description
31	R	0x0	DBG_MODE_L2PG_INT

Offset: 0x0184			Register Name: IOMMU_L2PG_INT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			Debug mode address switch causes L2 page table to occur interrupt.
30:7	/	/	/
6	R	0x0	MASTER6_L2PG_INT Master6 address switch causes L2 page table to occur interrupt. **Note: The bit is not used.**
5	R	0x0	MASTER5_L2PG_INT Master5 address switch causes L2 page table to occur interrupt.
4	R	0x0	MASTER4_L2PG_INT Master4 address switch causes L2 page table to occur interrupt.
3	R	0x0	MASTER3_L2PG_INT Master3 address switch causes L2 page table to occur interrupt.
2	R	0x0	MASTER2_L2PG_INT Master2 address switch causes L2 page table to occur interrupt.
1	R	0x0	MASTER1_L2PG_INT Master1 address switch causes L2 page table to occur interrupt.
0	R	0x0	MASTER0_L2PG_INT Master0 address switch causes L2 page table to occur interrupt.

3.11.6.55 0x0190 IOMMU Virtual Address Register (Default Value: 0x0000_0000)

Offset: 0x0190			Register Name: IOMMU_VA _REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	VA Virtual address of read/write

3.11.6.56 0x0194 IOMMU Virtual Address Data Register (Default Value: 0x0000_0000)

Offset: 0x0194			Register Name: IOMMU_VA_DATA _REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	VA_DATA Data corresponding to read/write virtual address

3.11.6.57 0x0198 IOMMU Virtual Address Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0198			Register Name: IOMMU_VA_CONFIG _REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MODE_SEL 0: Prefetch 1: Debug Mode It is used to chose prefetch mode or Debug mode.
31:9	/	/	/
8	R/W	0x0	VA_CONFIG Virtual Address Configuration 0: Read operation 1: Write operation
7:1	/	/	/
0	R/WAC	0x0	VA_CONFIG_START 0: No operation or operation is completed 1: Start After the operation is completed, the bit can clear automatically.

Read operation process:

a) Write IOMMU_VA_REG[31:0];

b) Write IOMMU_VA_CONFIG_REG[8] to 0;

c) Write IOMMU_VA_CONFIG_REG[0] to 1 to start read-process;

d) Query IOMMU_VA_CONFIG_REG[0] until it is 0;

e) Read IOMMU_VA_DATA_REG[31:0];

Write operation process:

a) Write IOMMU_VA_REG[31:0];

b) Write IOMMU_VA_DATA_REG[31:0];

c) Write IOMMU_VA_CONFIG_REG[8] to 1;

d) Write IOMMU_VA_CONFIG_REG[0] to 1 to start write-process;

e) Query IOMMU_VA_CONFIG_REG[0] until it is 0;

3.11.6.58 0x0200 IOMMU PMU Enable Register (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: IOMMU_PMU_ENABLE _REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	PMU_ENABLE

Offset: 0x0200			Register Name: IOMMU_PMU_ENABLE _REG
Bit	Read/Write	Default/Hex	Description
			0: Disable statistical function 1: Enable statistical function

3.11.6.59 0x0210 IOMMU PMU Clear Register (Default Value: 0x0000_0000)

Offset: 0x0210			Register Name: IOMMU_PMU_CLR _REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/WAC	0x0	PMU_CLR 0: No clear operation or clear operation is completed 1: Clear counter data After the operation is completed, the bit can clear automatically.

3.11.6.60 0x0230 IOMMU PMU Access Low 0 Register (Default Value: 0x0000_0000)

Offset: 0x0230			Register Name: IOMMU_PMU_ACCESS_LOW0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW0 Record total number of Micro TLB0 access, lower 32-bit register

3.11.6.61 0x0234 IOMMU PMU Access High 0 Register (Default Value: 0x0000_0000)

Offset: 0x0234			Register Name: IOMMU_PMU_ACCESS_HIGH0_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH0 Record total number of Micro TLB0 access, higher 11-bit register

3.11.6.62 0x0238 IOMMU PMU Hit Low 0 Register (Default Value: 0x0000_0000)

Offset: 0x0238			Register Name: IOMMU_PMU_HIT_LOW0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW0

Offset: 0x0238			Register Name: IOMMU_PMU_HIT_LOW0_REG
Bit	Read/Write	Default/Hex	Description
			Record total number of Micro TLB0 hit, lower 32-bit register

3.11.6.63 0x023C IOMMU PMU Hit High 0 Register (Default Value: 0x0000_0000)

Offset: 0x023C			Register Name: IOMMU_PMU_HIT_HIGH0_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH0 Record total number of Micro TLB0 hit, higher 11-bit register

3.11.6.64 0x0240 IOMMU PMU Access Low 1 Register (Default Value: 0x0000_0000)

Offset: 0x0240			Register Name: IOMMU_PMU_ACCESS_LOW1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW1 Record total number of Micro TLB1 access, lower 32-bit register

3.11.6.65 0x0244 IOMMU PMU Access High 1 Register (Default Value: 0x0000_0000)

Offset: 0x0244			Register Name: IOMMU_PMU_ACCESS_HIGH1_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH1 Record total number of Micro TLB1 access, higher 11-bit register

3.11.6.66 0x0248 IOMMU PMU Hit Low 1 Register (Default Value: 0x0000_0000)

Offset: 0x0248			Register Name: IOMMU_PMU_HIT_LOW1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW1 Record total number of Micro TLB1 hit, lower 32-bit register

3.11.6.67 0x024C IOMMU PMU Hit High 1 Register (Default Value: 0x0000_0000)

Offset: 0x024C			Register Name: IOMMU_PMU_HIT_HIGH1_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH1 Record total number of Micro TLB1 hit, higher 11-bit register

3.11.6.68 0x0250 IOMMU PMU Access Low 2 Register (Default Value: 0x0000_0000)

Offset: 0x0250			Register Name: IOMMU_PMU_ACCESS_LOW2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW2 Record total number of Micro TLB2 access, lower 32-bit register

3.11.6.69 0x0254 IOMMU PMU Access High 2 Register (Default Value: 0x0000_0000)

Offset: 0x0254			Register Name: IOMMU_PMU_ACCESS_HIGH2_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH2 Record total number of Micro TLB2 access, higher 11-bit register

3.11.6.70 0x0258 IOMMU PMU Hit Low 2 Register (Default Value: 0x0000_0000)

Offset: 0x0258			Register Name: IOMMU_PMU_HIT_LOW2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW2 Record total number of Micro TLB2 hit, lower 32-bit register

3.11.6.71 0x025C IOMMU PMU Hit High 2 Register (Default Value: 0x0000_0000)

Offset: 0x025C			Register Name: IOMMU_PMU_HIT_HIGH2_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/

Offset: 0x025C			Register Name: IOMMU_PMU_HIT_HIGH2_REG
Bit	Read/Write	Default/Hex	Description
10:0	R	0x0	PMU_HIT_HIGH2 Record total number of Micro TLB2 hit, higher 11-bit register

3.11.6.72 0x0260 IOMMU PMU Access Low 3 Register (Default Value: 0x0000_0000)

Offset: 0x0260			Register Name: IOMMU_PMU_ACCESS_LOW3_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW3 Record total number of Micro TLB3 access, lower 32-bit register

3.11.6.73 0x0264 IOMMU PMU Access High 3 Register (Default Value: 0x0000_0000)

Offset: 0x0264			Register Name: IOMMU_PMU_ACCESS_HIGH3_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH3 Record total number of Micro TLB3 access, higher 11-bit register

3.11.6.74 0x0268 IOMMU PMU Hit Low 3 Register (Default Value: 0x0000_0000)

Offset: 0x0268			Register Name: IOMMU_PMU_HIT_LOW3_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW3 Record total number of Micro TLB3 hit, lower 32-bit register

3.11.6.75 0x026C IOMMU PMU Hit High 3 Register (Default Value: 0x0000_0000)

Offset: 0x026C			Register Name: IOMMU_PMU_HIT_HIGH3_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH3 Record total number of Micro TLB3 hit, higher 11-bit register

3.11.6.76 0x0270 IOMMU PMU Access Low 4 Register (Default Value: 0x0000_0000)

Offset: 0x0270			Register Name: IOMMU_PMU_ACCESS_LOW4_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW4 Record total number of Micro TLB4 access, lower 32-bit register

3.11.6.77 0x0274 IOMMU PMU Access High 4 Register (Default Value: 0x0000_0000)

Offset: 0x0274			Register Name: IOMMU_PMU_ACCESS_HIGH4_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH4 Record total number of Micro TLB4 access, higher 11-bit register

3.11.6.78 0x0278 IOMMU PMU Hit Low 4 Register (Default Value: 0x0000_0000)

Offset: 0x0278			Register Name: IOMMU_PMU_HIT_LOW4_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW4 Record total number of Micro TLB4 hit, lower 32-bit register

3.11.6.79 0x027C IOMMU PMU Hit High 4 Register (Default Value: 0x0000_0000)

Offset: 0x027C			Register Name: IOMMU_PMU_HIT_HIGH4_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH4 Record total number of Micro TLB4 hit, higher 11-bit register

3.11.6.80 0x0280 IOMMU PMU Access Low 5 Register (Default Value: 0x0000_0000)

Offset: 0x0280			Register Name: IOMMU_PMU_ACCESS_LOW5_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW5 Record total number of Micro TLB5 access, lower 32-bit register

3.11.6.81 0x0284 IOMMU PMU Access High 5 Register (Default Value: 0x0000_0000)

Offset: 0x0284			Register Name: IOMMU_PMU_ACCESS_HIGH5_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH5 Record total number of Micro TLB5 access, higher 11-bit register

3.11.6.82 0x0288 IOMMU PMU Hit Low 5 Register (Default Value: 0x0000_0000)

Offset: 0x0288			Register Name: IOMMU_PMU_HIT_LOW5_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW5 Record total number of Micro TLB5 hit, lower 32-bit register

3.11.6.83 0x028C IOMMU PMU Hit High 5 Register (Default Value: 0x0000_0000)

Offset: 0x028C			Register Name: IOMMU_PMU_HIT_HIGH5_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH5 Record total number of Micro TLB5 hit, higher 11-bit register

3.11.6.84 0x0290 IOMMU PMU Access Low 6 Register (Default Value: 0x0000_0000)

Offset: 0x0290			Register Name: IOMMU_PMU_ACCESS_LOW6_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW6 Record total number of Micro TLB6 access, lower 32-bit register **Note: The field is not used.**

3.11.6.85 0x0294 IOMMU PMU Access High 6 Register (Default Value: 0x0000_0000)

Offset: 0x0294			Register Name: IOMMU_PMU_ACCESS_HIGH6_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH6 Record total number of Micro TLB6 access, higher 11-bit register **Note: The field is not used.**

3.11.6.86 0x0298 IOMMU PMU Hit Low 6 Register (Default Value: 0x0000_0000)

Offset: 0x0298			Register Name: IOMMU_PMU_HIT_LOW6_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW6 Record total number of Micro TLB6 hit, lower 32-bit register **Note: The field is not used.**

3.11.6.87 0x029C IOMMU PMU Hit High 6 Register (Default Value: 0x0000_0000)

Offset: 0x029C			Register Name: IOMMU_PMU_HIT_HIGH6_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH6 Record total number of Micro TLB6 hit, higher 11-bit register **Note: The field is not used.**

3.11.6.88 0x02D0 IOMMU PMU Access Low 7 Register (Default Value: 0x0000_0000)

Offset: 0x02D0			Register Name: IOMMU_PMU_ACCESS_LOW7_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW7 Record total number of Micro TLB7 access, lower 32-bit register

3.11.6.89 0x02D4 IOMMU PMU Access High 7 Register (Default Value: 0x0000_0000)

Offset: 0x02D4			Register Name: IOMMU_PMU_ACCESS_HIGH7_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH7 Record total number of Micro TLB7 access, higher 11-bit register

3.11.6.90 0x02D8 IOMMU PMU Hit Low 7 Register (Default Value: 0x0000_0000)

Offset: 0x02D8			Register Name: IOMMU_PMU_HIT_LOW7_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW7 Record total number of Micro TLB7 hit, lower 32-bit register

3.11.6.91 0x02DC IOMMU PMU Hit High 7 Register (Default Value: 0x0000_0000)

Offset: 0x02DC			Register Name: IOMMU_PMU_HIT_HIGH7_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH7 Record total number of Micro TLB7 hit, higher 11-bit register

3.11.6.92 0x02E0 IOMMU PMU Access Low 8 Register (Default Value: 0x0000_0000)

Offset: 0x02E0			Register Name: IOMMU_PMU_ACCESS_LOW8_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW8 Record total number of PTW Cache access, lower 32-bit register

3.11.6.93 0x02E4 IOMMU PMU Access High 8 Register (Default Value: 0x0000_0000)

Offset: 0x02E4			Register Name: IOMMU_PMU_ACCESS_HIGH8_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/

Offset: 0x02E4			Register Name: IOMMU_PMU_ACCESS_HIGH8_REG
Bit	Read/Write	Default/Hex	Description
10:0	R	0x0	PMU_ACCESS_HIGH8 Record total number of PTW Cache access, higher 11-bit register

3.11.6.94 0x02E8 IOMMU PMU Hit Low 8 Register (Default Value: 0x0000_0000)

Offset: 0x02E8			Register Name: IOMMU_PMU_HIT_LOW8_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW8 Record total number of PTW Cache hit, lower 32-bit register

3.11.6.95 0x02EC IOMMU PMU Hit High 8 Register (Default Value: 0x0000_0000)

Offset: 0x02EC			Register Name: IOMMU_PMU_HIT_HIGH8_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH8 Record total number of PTW Cache hit, higher 11-bit register

3.11.6.96 0x0300 IOMMU Total Latency Low 0 Register (Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: IOMMU_PMU_TL_LOW0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_TL_LOW0 Record total latency of Master0, lower 32-bit register

3.11.6.97 0x0304 IOMMU Total Latency High 0 Register (Default Value: 0x0000_0000)

Offset: 0x0304			Register Name: IOMMU_PMU_TL_HIGH0_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH0 Record total latency of Master0, higher 18-bit register

3.11.6.98 0x0308 IOMMU Max Latency 0 Register (Default Value: 0x0000_0000)

Offset: 0x0308			Register Name: IOMMU_PMU_ML0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ML0 Record the max latency of Master0.

3.11.6.99 0x0310 IOMMU Total Latency Low 1 Register (Default Value: 0x0000_0000)

Offset: 0x0310			Register Name: IOMMU_PMU_TL_LOW1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_TL_LOW1 Record total latency of Master1, lower 32-bit register

3.11.6.100 0x0314 IOMMU Total Latency High 1 Register (Default Value: 0x0000_0000)

Offset: 0x0314			Register Name: IOMMU_PMU_TL_HIGH1_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH1 Record total latency of Master1, higher 18-bit register

3.11.6.101 0x0318 IOMMU Max Latency 1 Register (Default Value: 0x0000_0000)

Offset: 0x0318			Register Name: IOMMU_PMU_ML1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ML1 Record the max latency of Master1.

3.11.6.102 0x0320 IOMMU Total Latency Low 2 Register (Default Value: 0x0000_0000)

Offset: 0x0320			Register Name: IOMMU_PMU_TL_LOW2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_TL_LOW2 Record total latency of Master2, lower 32-bit register

3.11.6.103 0x0324 IOMMU Total Latency High 2 Register (Default Value: 0x0000_0000)

Offset: 0x0324			Register Name: IOMMU_PMU_TL_HIGH2_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH2 Record total latency of Master2, higher 18-bit register

3.11.6.104 0x0328 IOMMU Max Latency 2 Register (Default Value: 0x0000_0000)

Offset: 0x0328			Register Name: IOMMU_PMU_ML2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ML2 Record the max latency of Master2.

3.11.6.105 0x0330 IOMMU Total Latency Low 3 Register (Default Value: 0x0000_0000)

Offset: 0x0330			Register Name: IOMMU_PMU_TL_LOW3_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_TL_LOW3 Record total latency of Master3, lower 32-bit register

3.11.6.106 0x0334 IOMMU Total Latency High 3 Register (Default Value: 0x0000_0000)

Offset: 0x0334			Register Name: IOMMU_PMU_TL_HIGH3_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH3 Record total latency of Master3, higher 18-bit register

3.11.6.107 0x0338 IOMMU Max Latency 3 Register (Default Value: 0x0000_0000)

Offset: 0x0338			Register Name: IOMMU_PMU_ML3_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ML3 Record the max latency of Master3.

3.11.6.108 0x0340 IOMMU Total Latency Low 4 Register (Default Value: 0x0000_0000)

Offset: 0x0340			Register Name: IOMMU_PMU_TL_LOW4_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_TL_LOW4 Record total latency of Master4, lower 32-bit register

3.11.6.109 0x0344 IOMMU Total Latency High 4 Register (Default Value: 0x0000_0000)

Offset: 0x0344			Register Name: IOMMU_PMU_TL_HIGH4_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH4 Record total latency of Master4, higher 18-bit register

3.11.6.110 0x0348 IOMMU Max Latency 4 Register (Default Value: 0x0000_0000)

Offset: 0x0348			Register Name: IOMMU_PMU_ML4_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ML4 Record the max latency of Master4.

3.11.6.111 0x0350 IOMMU Total Latency Low 5 Register (Default Value: 0x0000_0000)

Offset: 0x0350			Register Name: IOMMU_PMU_TL_LOW5_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_TL_LOW5 Record total latency of Master5, lower 32-bit register

3.11.6.112 0x0354 IOMMU Total Latency High 5 Register (Default Value: 0x0000_0000)

Offset: 0x0354			Register Name: IOMMU_PMU_TL_HIGH5_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH5 Record total latency of Master5, higher 18-bit register

3.11.6.113 0x0358 IOMMU Max Latency 5 Register (Default Value: 0x0000_0000)

Offset: 0x0358			Register Name: IOMMU_PMU_ML5_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ML5 Record the max latency of Master5.

3.11.6.114 0x0360 IOMMU Total Latency Low 6 Register (Default Value: 0x0000_0000)

Offset: 0x0360			Register Name: IOMMU_PMU_TL_LOW6_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_TL_LOW6 Record total latency of Master6, lower 32-bit register **Note: The field is not used.**

3.11.6.115 0x0364 IOMMU Total Latency High 6 Register (Default Value: 0x0000_0000)

Offset: 0x0364			Register Name: IOMMU_PMU_TL_HIGH6_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH6 Record total latency of Master6, higher 18-bit register **Note: The field is not used.**

3.11.6.116 0x0368 IOMMU Max Latency 6 Register (Default Value: 0x0000_0000)

Offset: 0x0368			Register Name: IOMMU_PMU_ML6_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ML6 Record the max latency of Master6. **Note: The field is not used.**

3.12 Message Box

3.12.1 Overview

The Message Box (MSGBOX) provides interrupt communication mechanism for on-chip processor.

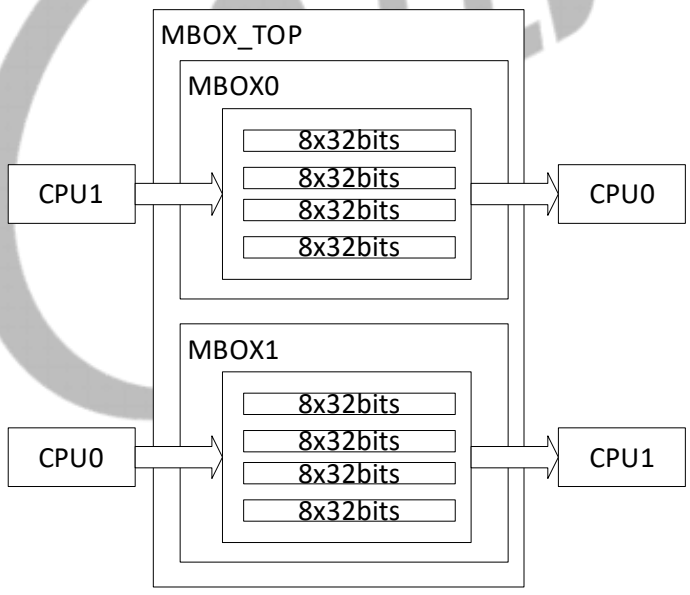
The MSGBOX has the following features:

- Supports 2 CPU to transmit information through channels. Each CPU has a MSGBOX.
  - CPU 0: ARM CPUX
  - CPU 1: DSP
- The channel between two CPU has 4 channels, and the FIFO depth of a channel is 8 x 32 bits
- Supports interrupts

3.12.2 Block Diagram

The following figure shows the block diagram of the message box.

Figure 3-36 Message Box Block Diagram



For MSGBOX0, CPU1: write; CPU0: read
For MSGBOX1, CPU0: write; CPU1: read

Each CPU has 4 channels. The two channels can be configured to be secure by software, the other two channels can be configured to be non-secure by software. The two secure channels or two non-secure channels can be configured as one synchronous box (Sending a message requires a response) or one asynchronous box (Sending a message does not require a response).

3.12.3 Functional Description

3.12.3.1 Clock and Reset

The MSGBOX is mounted on AHB0. Before accessing the MSGBOX registers, you need to de-assert the MSGBOX reset signal on AHB0 bus and then open the MSGBOX gating signal on AHB0 bus.

3.12.3.2 Typical Application

Several masters can build communication by configuring the MSGBOX. The communication parties have 4 channels. In a channel, the user1 is fixed as the transmitter and the user0 is fixed as the receiver. During the communication process, the current status can be judged through the interrupt or FIFO status.

3.12.3.3 Transmitter/Receiver Mode

At the same channel, user1 is fixed as transmitter, user0 is fixed as receiver.

3.12.3.4 Interrupt

Each channel can configure indepedently the interrupt enable bit, a read interrupt will be generated when the channel is empty, a write interrupt will be generated when the channel is non-full. For each CPU, all channels generate a read interrupt together, that is, if only a channel is non-full, the read interrupt will be generated, this channel can be obtained by quering the interrupt status register.

3.12.3.5 FIFO Status

When channel FIFO is non-full, the FIFO_FULL_FLAG is 0, at the moment the FIFO can be written.

When channel FIFO is full, the FIFO_FULL_FLAG is 1, at the moment if FIFO is written again, the first data of FIFO can be covered.

See **MSGBOX_MSG_STATUS_REG** for FIFO status.

3.12.4 Programming Guidelines

3.12.4.1 Checking the Transfer Status via the Interrupt

Follow the steps below to check the transfer status:

Step 1 Enable the interrupt for the channel: Configure the interrupt enable bits of transmitter/receiver through MSGBOX_WR_IRQ_EN_REG/MSGBOX_RD_IRQ_EN_REG. (user1: RX interrupt enable; user2: TX interrupt enable)

Step 2 Check the IRQ status of the corresponding queue through MSGBOX_WR_IRQ_STATUS_REG/MSGBOX_RD_IRQ_STATUS_REG.

- If the FIFO is not full, the channel generates a transmission interrupt to remind the transmitter to transmit data. Write data to the FIFO in the interrupt handler, then clear the pending bit of the transmitter in MSGBOX_WR_IRQ_STATUS_REG and the enable bit of the transmitter in MSGBOX_WR_IRQ_EN_REG.
- If the FIFO has new data, the channel generates a reception interrupt to remind the receiver to receive data. Read data from the FIFO in interrupt handler, then clear the pending bit of the receiver in MSGBOX_RD_IRQ_STATUS_REG and the enable bit of the receiver in MSGBOX_RD_IRQ_EN_REG.

3.12.4.2 Checking the Transfer Status via the FIFO

Follow the steps below to check the FIFO status of the corresponding queue:

- If the FIFO is not full, the transmitter fills the FIFO to 8*32 bits.
- If the FIFO is full, the receiver reads the FIFO data, and reads MSGBOX_FIFO_STATUS_REG to acquire the current FIFO data amount and the FIFO data amount before reading, which means no data is dropped.

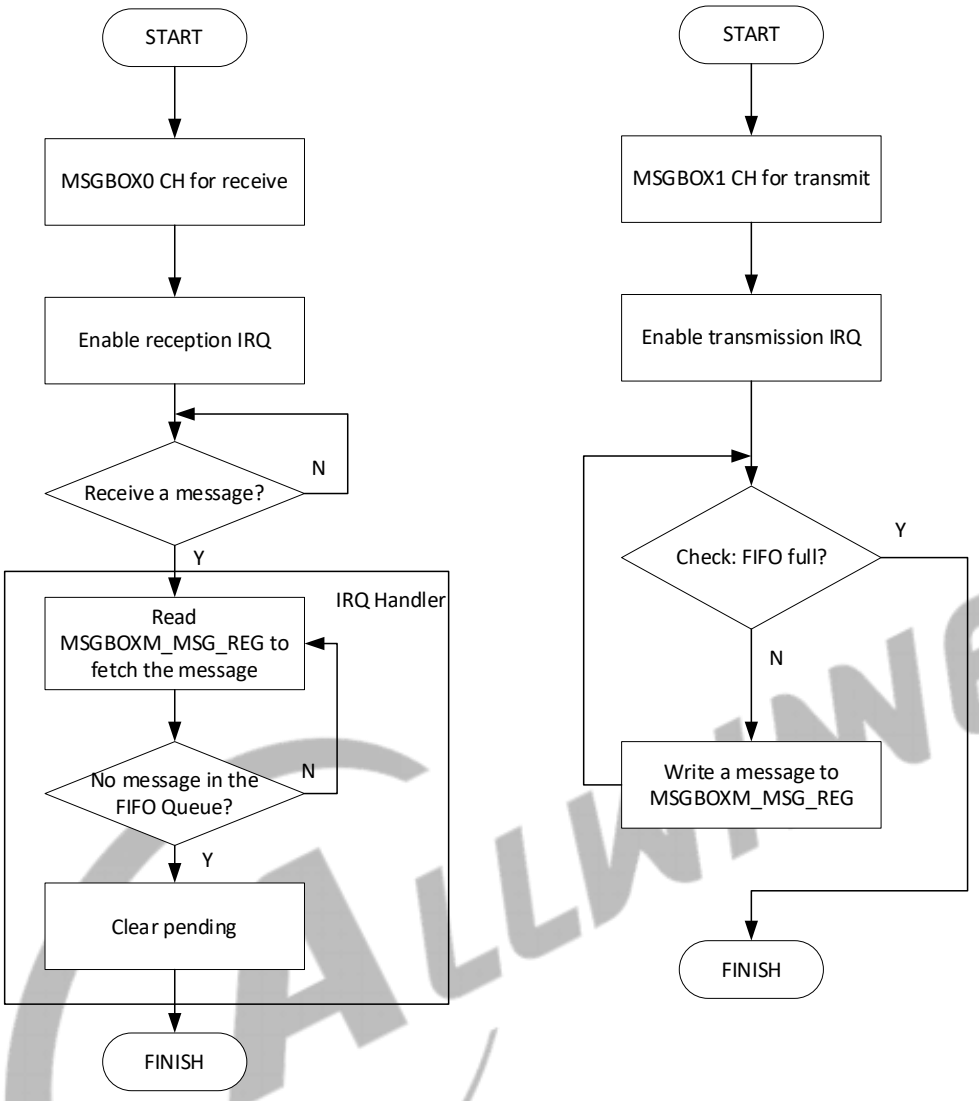
3.12.4.3 Transmitting/Receiving Message

The following figure shows the communication process between MSGBOX0 and MSGBOX1.

MSGBOX0: receiving message

MSGBOX1: transmitting message

Figure 3-37 The Communication Process between MSGBOX0 and MSGBOX1



3.12.5 Register List

Module Name	Base Address
ARM CPUX_MSGBOX	0x03003000
DSP_MSGBOX	0x01701000

Symbol	Description	Value
N	The CPU numbers that communicates with the current CPU	0–1
P	The channel numbers between two communication users	0–3

MSGBOX	CPU	The Value of N
MSGBOX (ARM CPUX)	DSP -> ARM CPUX	N=0
MSGBOX (DSP)	ARM CPUX -> DSP	N=0

Register Name	Offset	Description
MSGBOX_RD_IRQ_EN_REG	0x0020+N*0x0100 (N=0–1)	MSGBOX Read IRQ Enable Register
MSGBOX_RD_IRQ_STATUS_REG	0x0024+N*0x0100 (N=0–1)	MSGBOX Read IRQ Status Register
MSGBOX_WR_IRQ_EN_REG	0x0030+N*0x0100 (N=0–1)	MSGBOX Write IRQ Enable Register
MSGBOX_WR_IRQ_STATUS_REG	0x0034+N*0x0100 (N=0–1)	MSGBOX Write IRQ Status Register
MSGBOX_DEBUG_REG	0x0040+N*0x0100 (N=0–1)	MSGBOX Debug Register
MSGBOX_FIFO_STATUS_REG	0x0050+N*0x0100+P*0x0004 (N=0–1)(P=0–3)	MSGBOX FIFO Status Register
MSGBOX_MSG_STATUS_REG	0x0060+N*0x0100+P*0x0004 (N=0–1)(P=0–3)	MSGBOX Message Status Register
MSGBOX_MSG_REG	0x0070+N*0x0100+P*0x0004 (N=0–1)(P=0–3)	MSGBOX Message Queue Register
MSGBOX_WR_INT_THRESHOLD_REG	0x0080+N*0x0100+P*0x0004 (N=0–1)(P=0–3)	MSGBOX Write IRQ Threshold Register

3.12.6 Register Description

3.12.6.1 0x0020 + N*0x0100 MSGBox Read IRQ Enable Register (Default Value: 0x0000_0000)

Offset: 0x0020 + N*0x0100 (N=0–1)			Register Name: MSGBOX_RD_IRQ_EN_REG
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W	0x0	RECEPTION_MQ3_IRQ_EN Reception Channel3 Interrupt Enable 0: Disable 1: Enable (It notifies user 0 by interrupt when Message Queue 3 received a new message.)
5	/	/	/

Offset: 0x0020 + N*0x0100 (N=0–1)			Register Name: MSGBOX_RD_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
4	R/W	0x0	RECEPTION_MQ2_IRQ_EN Reception Channel2 Interrupt Enable 0: Disable 1: Enable (It notifies user 0 by interrupt when Message Queue 2 received a new message.)
3	/	/	/
2	R/W	0x0	RECEPTION_MQ1_IRQ_EN Reception Channel1 Interrupt Enable 0: Disable 1: Enable (It notifies user 0 by interrupt when Message Queue 1 received a new message.)
1	/	/	/
0	R/W	0x0	RECEPTION_MQ0_IRQ_EN Reception Channel0 Interrupt Enable 0: Disable 1: Enable (It notifies user 0 by interrupt when Message Queue 0 received a new message.)

3.12.6.2 0x0024 + N*0x0100 MSGBox Read IRQ Status Register (Default Value: 0x0000_0000)

Offset: 0x0024 + N*0x0100 (N=0–1)			Register Name: MSGBOX_RD_IRQ_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W1C	0x0	RECEPTION_MQ3_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user 0 when Message Queue 3 received a new message. Setting 1 to this bit clears it.
5	/	/	/
4	R/W1C	0x0	RECEPTION_MQ2_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user 0 when Message Queue 2 received a new message. Setting 1 to this bit clears it.
3	/	/	/

Offset: 0x0024 + N*0x0100 (N=0–1)			Register Name: MSGBOX_RD_IRQ_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
2	R/W1C	0x0	RECEPTION_MQ1_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user 0 when Message Queue 1 received a new message. Setting 1 to this bit clears it.
1	/	/	/
0	R/W1C	0x0	RECEPTION_MQ0_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user 0 when Message Queue 0 received a new message. Setting 1 to this bit clears it.

3.12.6.3 0x0030 + N*0x0100 MSGBox Write IRQ Enable Register (Default Value: 0x0000_0000)

Offset: 0x0030 + N*0x0100 (N=0–1)			Register Name: MSGBOX_WR_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	TRANSMIT_MQ3_IRQ_EN 0: Disable 1: Enable (It notifies user 1 by interrupt when Message Queue 3 empty level reaches the configured threshold.)
6	/	/	/
5	R/W	0x0	TRANSMIT_MQ2_IRQ_EN 0: Disable 1: Enable (It notifies user 1 by interrupt when Message Queue 2 empty level reaches the configured threshold.)
4	/	/	/
3	R/W	0x0	TRANSMIT_MQ1_IRQ_EN 0: Disable 1: Enable (It notifies user 1 by interrupt when Message Queue 1 empty level reaches the configured threshold.)
2	/	/	/
1	R/W	0x0	TRANSMIT_MQ0_IRQ_EN 0: Disable 1: Enable (It notifies user 1 by interrupt when Message Queue 0 empty level reaches the configured threshold.)
0	/	/	/

3.12.6.4 0x0034 + N*0x0100 MSGBox Write IRQ Status Register (Default Value: 0x0000_0000)

Offset: 0x0034 + N*0x0100 (N=0–1)			Register Name: MSGBOX_WR_IRQ_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W1C	0x0	TRANSMIT_MQ3_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user 1 when Message Queue 3 empty level reaches the configured threshold. Setting 1 to this bit clears it.
6	/	/	/
5	R/W1C	0x0	TRANSMIT_MQ2_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user 1 when Message Queue 2 empty level reaches the configured threshold. Setting 1 to this bit clears it.
4	/	/	/
3	R/W1C	0x0	TRANSMIT_MQ1_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user 1 when Message Queue 1 empty level reaches the configured threshold. Setting 1 to this bit clears it.
2	/	/	/
1	R/W1C	0x0	TRANSMIT_MQ0_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user 1 when Message Queue 0 empty level reaches the configured threshold. Setting 1 to this bit clears it.
0	/	/	/

3.12.6.5 0x0050+N*0x0100+P*0x0004 MSGBox FIFO Status Register (Default Value: 0x0000_0000)

Offset: 0x0050+N*0x0100+P*0x0004 (N=0–1)(P=0–3)			Register Name: MSGBOX_FIFO_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31: 1	/	/	/

Offset: 0x0050+N*0x0100+P*0x0004 (N=0–1)(P=0–3)			Register Name: MSGBOX_FIFO_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
0	R	0x0	FIFO_NOT_AVA_FLAG FIFO is not available flag 0: The Message FIFO queue empty level reaches the configured threshold 1: The Message FIFO queue empty level does not reach the configured threshold This FIFO status register has the status related to the message queue.

3.12.6.6 0x0060+N*0x0100+P*0x0004 MSGBox Message Status Register m (Default Value: 0x0000_0000)

Offset: 0x0060+N*0x0100+P*0x0004 (N=0–1)(P=0–3)			Register Name: MSGBOX_MSG_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R	0x0	MSG_NUM Message Number Number of unread messages in the message queue. Here, limited to eight messages per message queue. 0000: There is no message in the message FIFO queue. 0001: There is 1 message in the message FIFO queue. 0010: There are 2 messages in the message FIFO queue. 0011: There are 3 messages in the message FIFO queue. 0100: There are 4 messages in the message FIFO queue. 0101: There are 5 messages in the message FIFO queue. 0110: There are 6 messages in the message FIFO queue. 0111: There are 7 messages in the message FIFO queue. 1000: There are 8 messages in the message FIFO queue. 1001~1111:/

3.12.6.7 0x0070+N*0x0100+P*0x0004 MSGBox Message Queue Register (Default Value: 0x0000_0000)

Offset: 0x0070+N*0x0100+P*0x0004 (N=0–1)(P=0–3)			Register Name: MSGBOX_MSG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	MSG_QUE The message register stores the next to be read message of the message FIFO queue.

3.12.6.8 0x0080+N*0x0100+P*0x0004 MSGBox Write IRQ Threshold Register (Default Value: 0x0000_0000)

Offset: 0x0080+N*0x0100+P*0x0004 (N=0–1)(P=0–3)			Register Name: MSGBOX_WR_INT_THRESHOLD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x0	MSG_WR_INT_THRESHOLD_CFG Configure the FIFO empty level to trigger the write interrupt for user1 00: 1 01: 2 10: 4 11: 8

3.13 Spinlock

3.13.1 Overview

The spinlock provides hardware synchronization mechanism in multi-core systems. With the lock operation, the spinlock prevents multiple processors from handling the sharing data simultaneously and thus ensure the coherence of data.

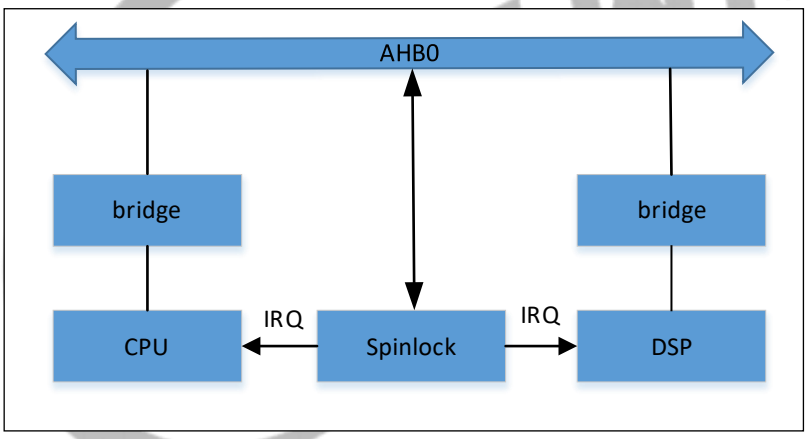
The spinlock has the following features:

- Supports 32 lock units
- Two kinds of lock status: locked and unlocked
- Lock time of the processor is predictable (less than 200 cycles)

3.13.2 Block Diagram

The following figure shows the block diagram of the spinlock.

Figure 3-38 Spinlock Block Diagram



3.13.3 Functional Description

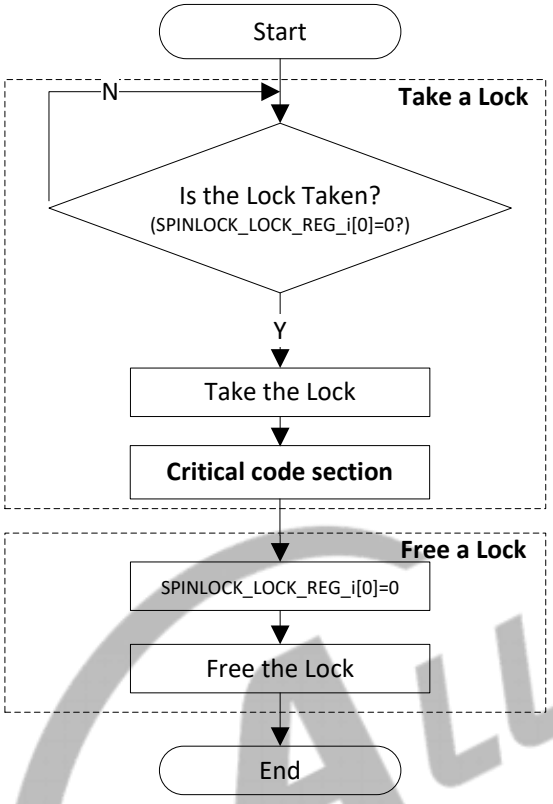
3.13.3.1 Clock and Reset

The spinlock is mounted on AHB0. Before accessing the spinlock registers, you need to de-assert the reset signal on AHB0 bus and then open the corresponding gating signal on AHB0 bus.

3.13.3.2 Typical Application

The following figure shows a typical application of the spinlock. A processor locks spinlock0 before executing specific codes, and then unlocks the codes. After the lock is freed, other processors can read or write the data.

Figure 3-39 Spinlock Typical Application Diagram



3.13.3.3 Spinlock State Machine

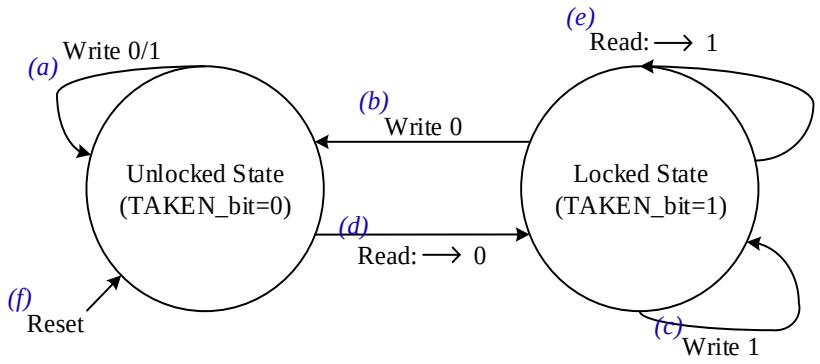
When a processor uses spinlock, it needs to acquire the spinlock status through **SPINLOCK_STATUS_REG**.

Reading operation: when the return value is 0, it indicates that the spinlock enters the locked status; reading this status bit again can return 1, it indicates that the spinlock is the locked status.

Writing operation: when the spinlock is in the locked status, writing 0 can convert the spinlock to the unlocked status, the writing operation for other status is invalid.

The following figure shows the spinlock state machine.

Figure 3-40 Spinlock State Machine



a) When the spinlock is in the unlocked state, writing 0/1 has no effect;

b) When the spinlock is in the locked state, writing 0 can convert the corresponding spinlock to the unlocked state;

c) When the spinlock is in the locked state, writing 1 has no effect;

d) When the spinlock is in the unlocked state, reading the bit can return 0 (it indicates spinlock enters into the locked state);

e) When the spinlock is in the locked state, reading the bit can return 1 (it indicates spinlock is in the locked state);

f) After reset, the spinlock is in the unlock state by default.

3.13.4 Programming Guidelines

3.13.4.1 Switching the Status

Follow the steps below to switch the lock status of a spinlock.

Step 1 When the read value from **SPINLOCKN_LOCK_REG (N=0–31)** is 0, the spinlock comes into the locked status.

Step 2 Execute the application codes, and the status of **SPINLOCK_STATUS_REG** is 1.

Step 3 Write 0 to **SPINLOCKN_LOCK_REG (N=0–31)**, the spinlock converts into the unlocked status, and the corresponding spinlock is released.

3.13.4.2 Processing the Interrupt

The spinlock generates an interrupt when a lock is freed (the lock status converts from the locked status to the unlocked status).

Follow the steps below to process the interrupt:

Step 1 Configure the interrupt enable bit of the corresponding spinlock in **SPINLOCK_IRQ_EN_REG** to enable the interrupt.

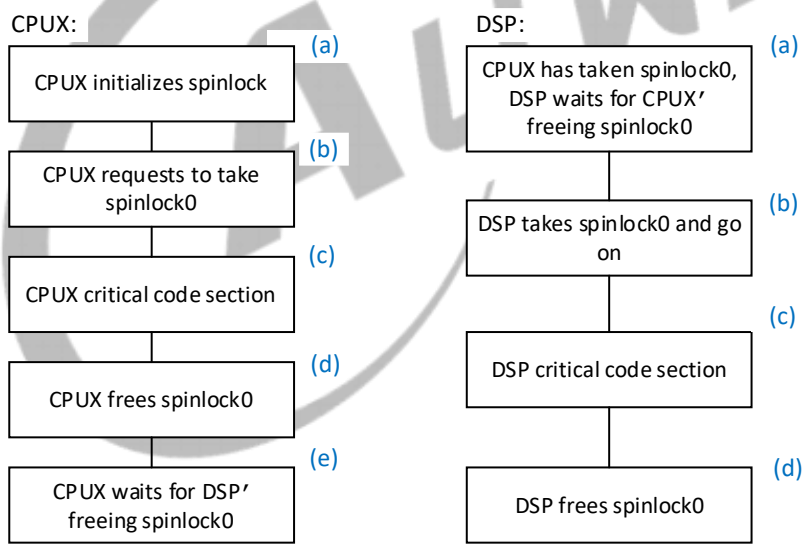
Step 2 The spinlock generates an interrupt when its status converts from the locked status to the unlocked status, and the corresponding bit of the **SPINLOCK_IRQ_STA_REG** turns to 1.

Step 3 Execute the interrupt handle function and clear the pending bit.

3.13.4.3 Taking/Freeing Spinlock

Take the synchronization between CPUX and DSP with Spinlock0 as an example, the CPUX and DSP perform the following steps.

Figure 3-41 CPUX and DSP Taking/Freeing Spinlock0 Process



CPUX:

(a) The CPUX initializes Spinlock.

(b) Check lock register0 (SPINLOCK_STATUS_REG0) status. If it is taken, check until CPUX frees spinlock0 and then request to take spinlock0. Otherwise, retry until the lock register0 is taken.

(c) Execute CPUX critical code.

(d) After executing CPUX critical code, the CPUX frees spinlock0.

(e) The CPUX waits for DSP to free spinlock0.

DSP:

(a) If the CPUX has taken spinlock0, the DSP waits for CPUX to free spinlock0.

(b) The DSP requests to take spinlock0. If it fails, retry until the lock register0 is taken.

(c) Execute DSP critical code.

(d) After executing DSP critical code, the DSP frees spinlock0.

The following codes are for reference.

----------**CPUX**----------

Step 1 CPUX initializes Spinlock

```
put_wvalue(SPINLOCK_BGR_REG,0x00010000);
put_wvalue(SPINLOCK_BGR_REG,0x00010001);
```

Step 2 CPUX requests to take spinlock0

```
rdata=readl(SPINLOCK_STATUS_REG0);              //Check lock register0 status
if(rdata != 0) writel(0, SPINLOCK_LOCK_REG0);   //If it is taken, check till CPUX frees spinlock0
rdata=readl(SPINLOCK_LOCK_REG0);                //Request to take spinlock0
if(rdata != 0) rdata=readl(SPINLOCK_LOCK_REG0); //If it fails, retry till lock register0 is taken
```

---------- **CPUX critical code section** ----------

Step 3 CPUX frees spinlock0

```
writel(0, SPINLOCK_LOCK_REG0);                  //CPUX frees spinlock0
```

Step 4 CPUX waits for DSP' freeing spinlock0

```
writel(readl(SPINLOCK_STATUS_REG0) == 1);       //CPUX waits for DSP' freeing spinlock0
```

----------**DSP**----------

Step 1 CPUX has taken spinlock0, DSP waits for CPUX' freeing spinlock0

```
while(readl(SPINLOCK_STATUS_REG0) == 1);        //DSP waits for CPUX' freeing spinlock0
```

Step 2 DSP takes spinlock0 and go on

```
rdata=readl(SPINLOCK_LOCK_REG0);                //Request to take spinlock0
if(rdata != 0) rdata=readl(SPINLOCK_LOCK_REG0); //If it fails, retry till lock register0 is taken
```

---------- **DSP critical code section** ----------

Step 3 DSP frees spinlock0

```
writel(0, SPINLOCK_LOCK_REG0);                    //DSP frees spinlock0
```

3.13.5 Register List

Module Name	Base Address
Spinlock	0x03005000

Register Name	Offset	Description
SPINLOCK_SYSTATUS_REG	0x0000	Spinlock System Status Register
SPINLOCK_STATUS_REG	0x0010	Spinlock Status Register
SPINLOCK_IRQ_EN_REG	0x0020	Spinlock Interrupt Enable Register
SPINLOCK_IRQ_STA_REG	0x0040	Spinlock Interrupt Status Register
SPINLOCK_LOCKID0_REG	0x0080	Spinlock Lockid0 Register
SPINLOCK_LOCKID1_REG	0x0084	Spinlock Lockid1 Register
SPINLOCK_LOCKID2_REG	0x0088	Spinlock Lockid2 Register
SPINLOCK_LOCKID3_REG	0x008C	Spinlock Lockid3 Register
SPINLOCK_LOCKID4_REG	0x0090	Spinlock Lockid4 Register
SPINLOCK_LOCK_REGN	0x0100 + N*0x0004	Spinlock Register N (N = 0 to 31)

3.13.6 Register Description

3.13.6.1 0x0000 Spinlock System Status Register (Default Value: 0x1000_0000)

Offset: 0x0000			Register Name: SPINLOCK_SYSTATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:28	R	0x1	LOCKS_NUM Number of lock registers implemented 00: This instance has 256 lock registers 01: This instance has 32 lock registers 10: This instance has 64 lock registers 11: This instance has 128 lock registers

Offset: 0x0000			Register Name: SPINLOCK_SYSTATUS_REG
Bit	Read/Write	Default/Hex	Description
27:9	/	/	/
8	R	0x0	IU0 In-Use flag0, covering lock register0-31 0: All lock registers 0-31 are in the NotTaken state. 1: At least one of the lock register 0-31 is in the Taken state.
7:0	/	/	/

3.13.6.2 0x0010 Spinlock Register Status Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: SPINLOCK_STATUS_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	LOCK_REG_STATUS SpinLock[i] status 0: The Spinlock is free 1: The Spinlock is taken

3.13.6.3 0x0020 Spinlock Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SPINLOCK_IRQ_EN_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	LOCK_IRQ_EN SpinLock[i] interrupt enable 0: Disable 1: Enable

3.13.6.4 0x0040 Spinlock Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: SPINLOCK_IRQ_STA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W1C	0x0	LOCK_IRQ_STATUS SpinLock[i] interrupt status 0: No effect 1: Pending Writing 1 clears this bit.

3.13.6.5 0x0080 Spinlock Lockid0 Register (Default Value: 0x7777_7777)

Offset: 0x0080			Register Name: SPINLOCK_LOCKIN0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x77777777	LOCKID0

3.13.6.6 0x0084 Spinlock Lockid1 Register (Default Value: 0x7777_7777)

Offset: 0x0084			Register Name: SPINLOCK_LOCKIN1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x77777777	LOCKID1

3.13.6.7 0x0088 Spinlock Lockid2 Register (Default Value: 0x7777_7777)

Offset: 0x0088			Register Name: SPINLOCK_LOCKIN2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x77777777	LOCKID2

3.13.6.8 0x008C Spinlock Lockid3 Register (Default Value: 0x7777_7777)

Offset: 0x008C			Register Name: SPINLOCK_LOCKIN3_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x77777777	LOCKID3

3.13.6.9 0x0090 Spinlock Lockid4 Register (Default Value: 0x7777_7777)

Offset: 0x0090			Register Name: SPINLOCK_LOCKIN4_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x77777777	LOCKID4

3.13.6.10 0x0100 + N*0x04 Spinlock Register N (N = 0 to 31) (Default Value: 0x0000_0000)

Offset: 0x0100 + N*0x0004 (N = 0 to 31)			Register Name: SPINLOCKN_LOCK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	TAKEN Lock State Read 0x0: The lock was previously Not Taken (free). The requester is granted the lock. Write 0x0: Set the lock to Not Taken (free). Read 0x1: The lock was previously Taken. The requester is not granted the lock and must retry. Write 0x1: No update to the lock value.

3.14 RTC

3.14.1 Overview

The Real Time Clock (RTC) is used to implement time counter and timing wakeup functions. The RTC can display the year, month, day, week, hour, minute, second in real time. The RTC has the independent power to continue to work in system power-off.

The RTC has the following features:

- Provides a 16-bit counter for counting day, 5-bit counter for counting hour, 6-bit counter for counting minute, 6-bit counter for counting second
- External connect a 32.768 kHz low-frequency oscillator for count clock
- Timer frequency is 1 kHz
- Configurable initial value by software anytime
- Supports timing alarm, and generates interrupt and wakeup the external devices
- Eight 32-bit user registers for storing power-off information

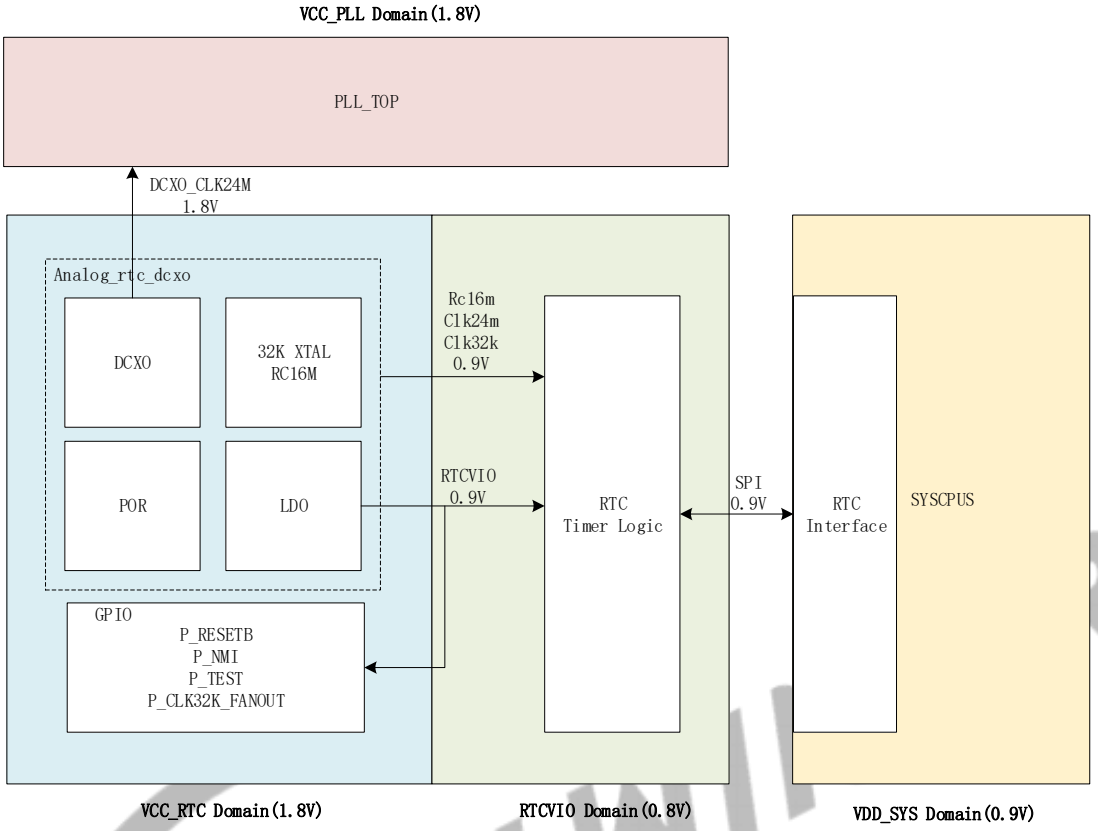
CAUTION

The register configuration of RTC is AHB bus, it only can support word operation, not byte operation and half-word operation.

3.14.2 Block Diagram

The following figure shows the block diagram of the RTC.

Figure 3-42 RTC Block Diagram



3.14.3 Functional Description

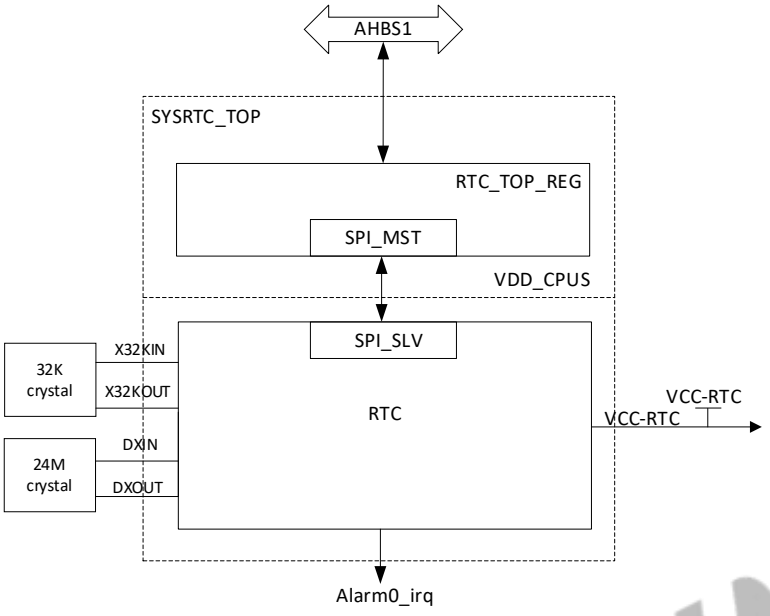
3.14.3.1 External Signals

Table 3-18 RTC External Signals

Signal	Description
X32KIN	32.768 kHz oscillator input
X32KOUT	32.768 kHz oscillator output
VCC-RTC	RTC high voltage, generated via external power

3.14.3.2 Typical Application

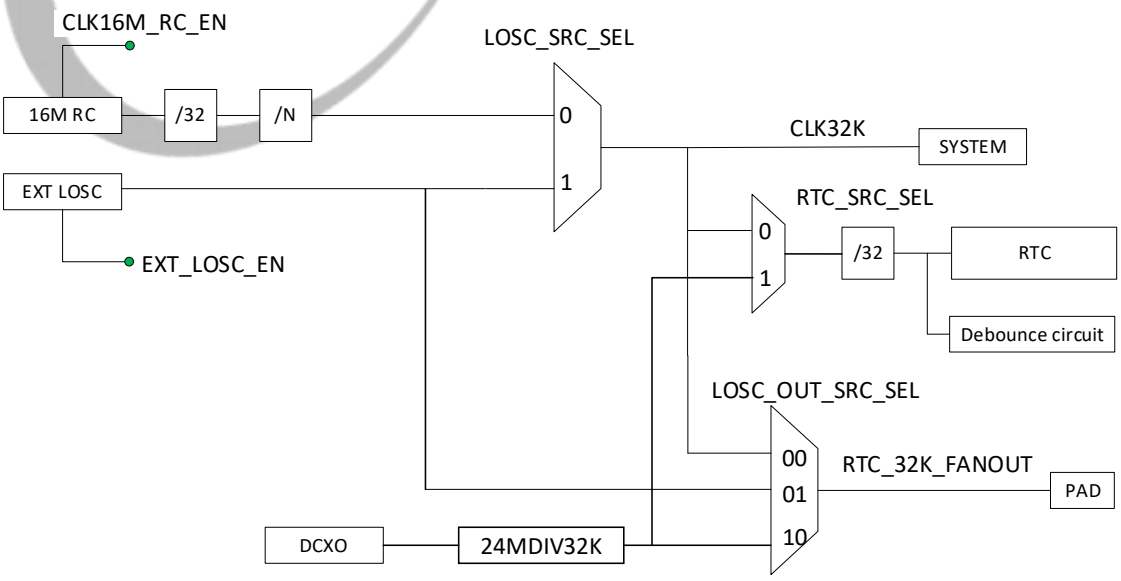
Figure 3-43 RTC Application Diagram



3.14.3.3 Clock Tree

The following figure shows the clock tree of the RTC.

Figure 3-44 RTC Clock Tree



- **LOSC**

The LOSC has 2 clock sources: internal RC, external low frequency crystal. The LOSC selects the internal RC by default, when the system starts, the LOSC can select by software the external low frequency crystal to provide much accuracy clock. The clock accurate of the LOSC is related to the accurate of the external low frequency crystal. Usually select 32.768 kHz crystal with ±20 ppm frequency tolerance. When using internal RC, the clock can be changed by changing division ratio. When using external clock, the clock cannot be changed.

- **RTC**

The clock sources of RTC can be selected by related switches, including 32K divided by internal 16 MHz RC, 32K divided by external DCXO, and external 32.768 kHz crystal.

- **System 32K**

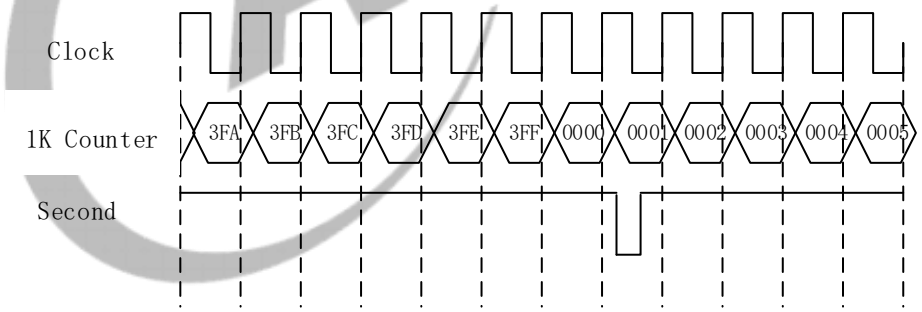
The clock sources of system 32K are from external 32.768 kHz crystal and 32K divided by the internal 16 MHz RC.

- **RTC_32K_FANOUT**

The clock source of RTC_32K_FANOUT can select CLK32K, external 32.768 kHz crystal or 32K divided by external DCXO.

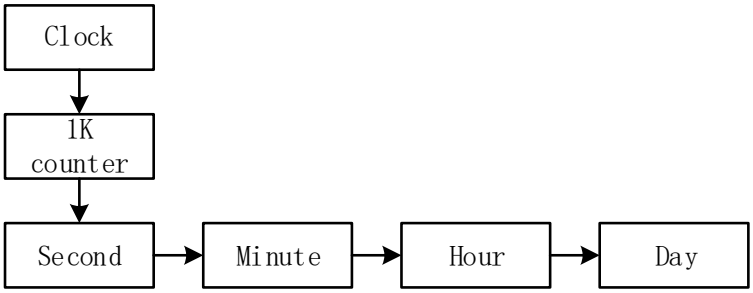
3.14.3.4 Real Time Clock

Figure 3-45 RTC Counter



The 1K counter adds 1 on each rising edge of the clock. When the clock number reaches 0x3FF, 1K counter starts to count again from 0, and the second counter adds 1. The step structure of 1 kHz counter is as follows.

Figure 3-46 RTC 1 kHz Counter Step Structure



According to above implementation, the changing range of each counter is as follows.

Table 3-19 RTC Counter Changing Range

Counter	Range
Second	0 to 59
Minute	0 to 59
Hour	0 to 23
Day	0 to 65535 (The year, month, day need be transformed by software according to day counter)

CAUTION

Because there is no error correction mechanism in the hardware, note that each counter configuration should not exceed a reasonable counting range.

3.14.3.5 Alarm 0

The principle of alarm0 is a comparator. When RTC timer reaches the scheduled time, the RTC generates the interrupt, or outputs low level signal by NMI pin to wakeup power management chip.

The RTC only generates one interrupt when RTC timer reached the scheduled day, hour, minute and second counter, then the RTC needs to be set a new scheduled time, the next interrupt can be generated.

3.14.3.6 Power-off Information Storage

The RTC provides eight 32-bit general purpose register to store power-off information.

Because VCC-RTC always holds non-power-off state after VCC-RTC cold starts, when the system is in shutdown or standby scene, the CPU can judge software process by the storing information.

3.14.3.7 RTC_VIO

The RTC module has a LDO, the input source of the LDO is VCC_RTC, the output of the LDO is RTC_VIO, the value of RTC_VIO is adjustable, the RTC_VIO is mainly used for internal digital logic.

3.14.3.8 RC Calibration Usage Scenario

- Power-on: Select non-accurate 32K divided by internal RC.
- Normal scenario: Select external accurate 32K, or external calibrated 32K.
- Standby or power-off scenario: Select external accurate 32K, or external calibrated 32K.

3.14.4 Programming Guidelines

3.14.4.1 RTC Clock Control

Step 1 Select clock source: Select clock source by the bit0 of **LOSC_CTRL_REG**, the clock source is the internal RC oscillator by default. When the system starts, the clock source can be switched to the external 32K oscillator by software.

Step 2 Auto switch: After enabled the bit[15:14] of **LOSC_CTRL_REG**, the RTC automatically switches clock source to the internal oscillator when the external crystal could not output waveform, the switch status can query by the bit[1] of **LOSC_AUTO_SWT_STA_REG**.

NOTE

If only configuring the bit[15] of **LOSC_CTRL_REG**, the clock source status bit cannot be changed after the auto switch is valid, because the two functions are independent.

Here is the basic code samples.

```
Write (0x16aa4000,LOSC_Ctrl);    //Write key field
Write (0x16aa4001,LOSC_Ctrl);    //Select the external 32K clock
```

3.14.4.2 RTC Calendar

Step 1 Write time initial value: Write the current time to RTC_DAY_REG and RTC_HH_MM_SS_REG.

Step 2 After updated time, the RTC restarts to count again. The software can read the current time anytime.

NOTE

- The RTC can only provide day counter, so the current day counter need be converted to year, month, day and week by software.
- Ensure the bit[8:7] of LOSC_CTRL_REG is 0 before the next time configuration is performed.

Here is the basic code samples.

For example: set time to 21st, 07:08:09 and read it.

RTC_DAY_REG = 0x00000015;

RTC_HH_MM_SS_REG = 0x00070809; //0000 0000 000|0 0000(Hour) 00|00 0000(Minute) 00|00 0000(Second)

Read (RTC_DAY_REG);

Read (RTC_HH_MM_SS_REG);

3.14.4.3 Alarm0

Step 1 Enable alram0 interrupt by writing ALARM0_IRQ_EN.

Step 2 Set the counter comparator, write the count-down day, hour, minute, second number to ALARM0_DAY_SET_REG and ALARM0_HH-MM-SS_SET_REG.

Step 3 Enable alarm0 function by writing ALARM0_ENABLE_REG, then the software can query alarm count value in real time by ALARM0_DAY_SET_REG and ALARM0_HH-MM-SS_SET_REG**.** When the setting time reaches, ALARM0_IRQ_STA_REG is set to 1 to generate interrupt.

Step 4 After enter the interrupt process, write ALARM0_IRQ_STA_REG to clear the interrupt pending, and execute the interrupt process.

Step 5 Resume the interrupt and continue to execute the interrupted process.

Step 6 The power-off wakeup is generated via SoC hardware and PMIC, the software only needs to set the pending condition of alarm0, and set ALARM_CONFIG_REG to 1.

3.14.5 Register List

Module Name	Base Address
RTC	0x07090000

Register Name	Offset	Description
LOSC_CTRL_REG	0x0000	Low Oscillator Control Register
LOSC_AUTO_SWT_STA_REG	0x0004	LOSC Auto Switch Status Register
INTOSC_CLK_PRESCAL_REG	0x0008	Internal OSC Clock Pre-scalar Register
RTC_DAY_REG	0x0010	RTC Year-Month-Day Register
RTC_HH_MM_SS_REG	0x0014	RTC Hour-Minute-Second Register
ALARM0_DAY_SET_REG	0x0020	Alarm 0 Day Setting Register
ALARM0_CUR_VLU_REG	0x0024	Alarm 0 Counter Current Value Register
ALARM0_ENABLE_REG	0x0028	Alarm 0 Enable Register
ALARM0_IRQ_EN	0x002C	Alarm 0 IRQ Enable Register
ALARM0_IRQ_STA_REG	0x0030	Alarm 0 IRQ Status Register
ALARM_CONFIG_REG	0x0050	Alarm Configuration Register
32K_FOUT_CTRL_GATING_REG	0x0060	32K Fanout Control Gating Register
GP_DATA_REG	0x0100 + N*0x04	General Purpose Register (N=0 to 7)
FBOOT_INFO_REG0	0x0120	Fast Boot Information Register0
FBOOT_INFO_REG1	0x0124	Fast Boot Information Register1
DCXO_CTRL_REG	0x0160	DCXO Control Register
RTC_VIO_REG	0x0190	RTC_VIO Regulation Register
IC_CHARA_REG	0x01F0	IC Characteristic Register
VDD_OFF_GATING_CTRL_REG	0x01F4	VDD Off Gating Control Register
EFUSE_HV_PWRSWT_CTRL_REG	0x0204	Efuse High Voltage Power Switch Control Register
RTC_SPI_CLK_CTRL_REG	0x0310	RTC SPI Clock Control Register

NOTE

The offset addresses less than 0x0300 are in VDD_RTC power domain, and the offset addresses large than or equal to 0x300 are in VDD_SYS power domain.

3.14.6 Register Description

3.14.6.1 0x0000 LOSC Control Register (Default Value: 0x0000_4010)

Offset:0x0000			Register Name: LOSC_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	W	0x0	KEY_FIELD Key Field This field should be filled with 0x16AA, and then the bit0 and bit1 can be written with the new value.
15	R/W	0x0	LOSC_AUTO_SWT_FUNCTION LOSC auto switch function disable 0: Enable 1: Disable
14	R/W	0x1	LOSC_AUTO_SWT_32K_SEL_EN LOSC auto switch 32K clk source select enable 0: Disable. When the losc losts, the 32k clk source will not change to RC 1: Enable. When the losc losts, the 32k clk source will change to RC (LOSC_SRC_SEL will be changed from 1 to 0)
13:9	/	/	/
8	R/W	0x0	RTC_HHMMSS_ACCE RTC Hour Minute Second access After writing the RTC HH-MM-SS Register, this bit is set and it will be cleared until the real writing operation is finished. After writing the RTC HH-MM-SS Register, the RTC HH-MM-SS Register will be refreshed for at most one second. **Note: Make sure that the bit is 0 for time configuration.**
7	R/W	0x0	RTC_DAY_ACCE RTC DAY access After writing the RTC DAY register, this bit is set and it will be cleared until the real writing operation is finished. After writing the RTC DAY register, the DAY register will be refreshed for at most one second. **Note: Make sure that the bit is 0 for time configuration.**
6:5	/	/	/
4	R/W	0x1	EXT_LOSC_EN External 32.768 kHz Crystal Enable 0: Disable 1: Enable

Offset:0x0000			Register Name: LOSC_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
3:2	R/W	0x0	EXT_LOSC_GSM External 32.768 kHz Crystal GSM 00: Low 01: / 10: / 11: High When GSM is changed, the 32K oscillation circuit will arise transient instability. If the autoswitch function (bit 15) is enabled, 32K changes to RC16M with certain probability. The GSM can influence the time of 32K starting oscillation, the more the GSM, the shorter the time of starting oscillation. So modifying GSM is not recommended. If you need to modify the GSM, firstly disable the auto switch function (bit 15), with a delay of 50 us, then change the GSM, the 32K clock source is changed to external clock.
1	R/W	0x0	RTC_SRC_SEL RTC_TIMER Clock Source Select 0: LOSC_SRC 1: 24MDIV32K Before switching the bit, make sure that the 24MDIV32K function is enabled, that is, the bit16 of the 32K Fanout Control Register is 1.
0	R/W	0x0	LOSC_SRC_SEL LOSC Clock Source Select 0: Low frequency clock from 16M RC 1: External 32.768 kHz OSC

NOTE

If the bit[8:7] of LOSC_CTRL_REG is set, the RTC HH-MM-SS, DD and ALARM DD-HH-MM-SS register cannot be written.

3.14.6.2 0x0004 LOSC Auto Switch Status Register (Default Value: 0x0000_0000)

Offset:0x0004			Register Name: LOSC_AUTO_SWT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R	0x0	EXT_LOSC_STA Work only when the auto switch function is enabled. 0: External 32.768 kHz OSC work normally 1: External 32.768 kHz OSC work abnormally
1	R/W1C	0x0	LOSC_AUTO_SWT_PEND LOSC auto switch pending 0: No effect 1: Auto switch pending, it means LOSC_SRC_SEL is changed from 1 to 0. Setting 1 to this bit will clear it.
0	R	0x0	LOSC_SRC_SEL_STA Checking LOSC clock source status 0: Low frequency clock from 16M RC 1: External 32.768 kHz OSC

3.14.6.3 0x0008 Internal OSC Clock Prescalar Register (Default Value: 0x0000_000F)

Offset:0x0008			Register Name: INTOSC_CLK_PRESCAL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4:0	R/W	0xF	INTOSC_32K_CLK_PRESCAL Internal OSC 32K Clock Prescalar value N. The clock output = Internal RC/32/N. 00000: 1 00001: 2 00002: 3 ..... 11111: 32

3.14.6.4 0x0010 RTC Year-Month-DAY Register (Default Value: UDF)

Offset:0x0010			Register Name: RTC_DAY_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	UDF	DAY Set Day Range from 0 to 65535.

3.14.6.5 0x0014 RTC Hour-Minute-Second Register (Default Value: UDF)

Offset:0x0014			Register Name: RTC_HH_MM_SS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	UDF	HOUR Set hour Range from 0 to 23.
15:14	/	/	/
13:8	R/W	UDF	MINUTE Set minute Range from 0 to 59.
7:6	/	/	/
5:0	R/W	UDF	SECOND Set second Range from 0 to 59.

3.14.6.6 0x0020 Alarm 0 Day Setting Register (Default Value: 0x0000_0000)

Offset:0x0020			Register Name: ALARM0_DAY_SET_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0	ALARM0_COUNTER Alarm 0 Counter is based on Day.

3.14.6.7 0x0024 Alarm 0 Counter Current Value Register (Default Value: UDF)

Offset:0x0024			Register Name: ALARM0_CUR_VLU_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	UDF	HOUR Current hour Range from 0 to 23.
15:14	/	/	/
13:8	R/W	UDF	MINUTE Current minute Range from 0 to 59.
7:6	/	/	/
5:0	R/W	UDF	SECOND Current second Range from 0 to 59.

3.14.6.8 0x0028 Alarm 0 Enable Register (Default Value: 0x0000_0000)

Offset:0x0028			Register Name: ALARM0_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ALM_0_EN Alarm 0 Enable 0: Disable 1: Enable

3.14.6.9 0x002C Alarm 0 IRQ Enable Register (Default Value: 0x0000_0000)

Offset:0x002C			Register Name: ALARM0_IRQ_EN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ALARM0_IRQ_EN Alarm 0 IRQ Enable 0: Disable 1: Enable

3.14.6.10 0x0030 Alarm 0 IRQ Status Register (Default Value: 0x0000_0000)

Offset:0x0030			Register Name: ALARM0_IRQ_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W1C	0x0	ALARM0_IRQ_PEND Alarm 0 IRQ Pending bit 0: No effect 1: Pending, alarm 0 counter value is reached If alarm 0 irq enable is set to 1, the pending bit will be sent to the interrupt controller.

3.14.6.11 0x0050 Alarm Configuration Register (Default Value: 0x0000_0000)

Offset:0x0050			Register Name: ALARM_CONFIG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ALARM_WAKEUP Configuration of alarm wake up output. 0: Disable alarm wake up output 1: Enable alarm wake up output

3.14.6.12 0x0060 32K Fanout Control Gating Register (Default Value: 0x0000_0000)

Offset:0x0060			Register Name: 32K_FOUT_CTRL_GATING_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	HOSC_TO_32K_DIVIDER_ENABLE HOSC to 32k divider enable 0: Disable the hosc 24M to 32K divider circuit 1: Enable the hosc 24M to 32K divider circuit
15:3	/	/	/
2:1	R/W	0x0	LOSC_OUT_SRC_SEL LOSC output source select 00: RTC_32K (select by RC_CLK_SRC_SEL & LOSC_SRC_SEL) 01: LOSC 10: HOSC divided 32K

Offset:0x0060			Register Name: 32K_FOUT_CTRL_GATING_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	32K_FANOUT_GATING LOSC out gating enable Configuration of LOSC output, and there is no LOSC output by default. 0: Mask LOSC output gating 1: Enable LOSC output gating

3.14.6.13 0x0100+N*0x0004 General Purpose Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0004 (N=0 to 7)			Register Name: GP_DATA_REGN
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	GP_DATA Data [31:0]

NOTE

General purpose register 0 to 7 value can be stored if the RTC-VIO is larger than 0.7 V.

3.14.6.14 0x0120 Fast Boot Information Register0 (Default Value: 0x0000_0000)

Offset:0x0120			Register Name: FBOOT_INFO_REG0
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	FBOOT_INFO0 Fast Boot info Fast Boot Information 0, refer to BROM spec.

3.14.6.15 0x0124 Fast Boot Information Register1 (Default Value: 0x0000_0000)

Offset:0x0124			Register Name: FBOOT_INFO_REG1
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	FBOOT_INFO1 Fast Boot info Fast Boot Information 1, refer to BROM spec.

3.14.6.16 0x0160 DCXO Control Register (Default Value: 0x883F_10F7)

Offset:0x0160			Register Name: DCXO_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	CLK_REQ_ENB Clock REQ enable 0: Enable DCXO wake up function 1: Disable DCXO wake up function
30:28	/	/	/
27:24	R/W	0x8	DCXO_ICTRL DCXO current control value
23	/	/	/
22:16	R/W	0x3F	DCXO_TRIM DCXO cap array value The capacity cell is 55 fF.
15:13	/	/	/
12:8	R/W	0x10	DCXO_BG DCXO bandgap output voltage
7	R/W	0x1	DCXO_LDO_INRUSHB DCXO LDO driving capacity signal, active high
6	R/W	0x1	XTAL_MODE Xtal mode enable signal, active high 0: For external clk input mode 1: For normal mode
5:4	R/W	0x3	DCXO_RFCLK_ENHANCE DCXO rfclk enhance Enhance driving capacity of output OUT_RF_REFCLK, 0x0 for 5 pF, 0x1 for 10 pF, 0x2 for 15 pF, 0x3 for 20 pF.
3	/	/	/
2	R/W	0x1	RSTO_DLY_SEL For Debug Use Only. It cannot configure to 0 in normal state.
1	R/W	0x1	DCXO_EN DCXO enable 1: Enable 0: Disable

Offset:0x0160			Register Name: DCXO_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
0	R/W	0x1	CLK16M_RC_EN 1: Enable 0: Disable The related register configuration is necessary to ensure the reset debounce circuit has a stable clock source. The first time SoC starts up, by default, the reset debounce circuit of SoC uses 32K divided by RC16M. In power-off, software reads the related bit to ensure whether EXT32K is working normally, if it is normal, first switch the clock source of debounce circuit to EXT32K, then close RC16M. Without EXT32K scenario or external RTC scenario, software confirms firstly whether EXT32K is working normally before switching, or software does not close RC16M.

3.14.6.17 0x0190 RTC_VIO Regulation Register (Default Value: 0x0000_0004)

Offset:0x0190			Register Name:RTC_VIO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R/W	0x0	V_SEL VDD Select 0: Resistance divider 1: Band gap
3	/	/	/
2:0	R/W	0x4	RTC_VIO_REGU RTC_VIO Voltage Select The RTC-VIO is provided power for RTC digital part. These bits are useful for regulating the RTC_VIO from 0.65 V to 1.3 V. 000: 1.0 V 001: 0.65 V (the configuration can cause RTC reset) 010: 0.7 V 011: 0.8 V 100: 0.9 V 101: 1.1 V 110: 1.2 V 111: 1.3 V

3.14.6.18 0x01F0 IC Characteristic Register (Default Value: 0x0000_0000)

Offset:0x01F0			Register Name: IC_CHARA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	KEY_FIELD Key Field The field should be written as 0x16AA. Writing any other value in this field aborts the write-operation.
15:0	R/W	0x0	ID_DATA Return 0x16AA only if the KEY_FIELD is set as 0x16AA when read those bits, otherwise return 0x0.

3.14.6.19 0x01F4 VDD Off Gating Control Register (Default Value: 0x0000_0021)

Offset:0x01F4			Register Name: VDD_OFF_GATING_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	W	0x0	KEY_FIELD Key Field This field should be filled with 0x16AA, and then the bit 15 can be configured.
15	WAC	0x0	PWROFF_GAT_RTC_CFG (For Debug Use Only) Power off gating control signal When use vdd_sys to RTC isolation software control, write this bit to 1. It will only be cleared by resetb release.
14:12	/	/	/
11:4	R/W	0x2	VCCIO_DET_SPARE Bit[7:5]: Reserved, default=0 Bit[4]: Bypass debounce circuit, defaule=0 Bit[3]: Enable control, defaule=0 0: Disable VCC-IO detection 1: Force the detection output Bit[2:0]: Gear adjustment 000: Detection threshold is 2.5 V 001: Detection threshold is 2.6 V 010: Detection threshold is 2.7 V (default) 011: Detection threshold is 2.8 V

Offset:0x01F4			Register Name: VDD_OFF_GATING_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			100: Detection threshold is 2.9 V 101: Detection threshold is 3 V 110: N/A 111: N/A
3:1	/	/	/
0	R/W	0x1	VCCIO_DET_BYPASS_EN 0: not bypass 1: bypass

3.14.6.20 0x0204 Efuse High Voltage Power Switch Control Register (Default Value: 0x0000_0000)

Offset:0x0204			Register Name: EFUSE_HV_PWRSWT_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	EFUSE_1.8V_POWER_SWITCH_CONTROL 1: Open power switch 0: Close power switch

3.14.6.21 0x0310 RTC SPI Clock Control Register (Default Value: 0x0000_0009)

Offset:0x0310			Register Name: RTC_SPI_CLK_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	RTC Reg CFG SPI Clock Gating 0: Gating 1: Not Gating Before configurating RTC register, the clock divider of SPI needs be configured firstly, then clock gating needs be enabled. **Note: Frequency division and clock gating can not be set at the same time.**
30:5	/	/	/
4:0	R/W	0x9	RTC Reg CFG SPI Clock Divider: M Actual SPI Clock = AHBS1/(M+1), (0 to 15) The default frequency of AHBS1 is 200 MHz, and the default frequency of SPI Clock is 20 MHz.

Offset:0x0310			Register Name: RTC_SPI_CLK_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			Note: The SPI clock can not exceed 50 MHz, or else the RTC register may be abnormal.

Contents

Figures

4 Video and Graphics

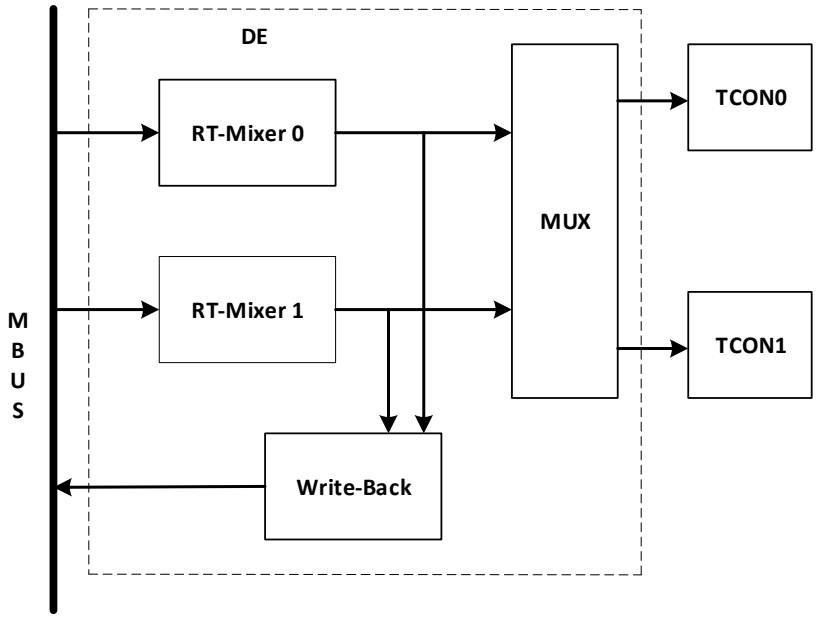
4.1 DE

The Display Engine (DE) is a hardware composer to transfer image layers from a local bus or a video buffer to the LCD interface. The DE supports four overlay windows to blend, and supports image post-processing in the video channel. The block diagram of DE is shown in Figure 4-1.

The DE has the following features:

- Output size up to 2048 x 2048
- Four alpha blending channels for main display, three channels for aux display
- Four overlay layers in each channel, and has a independent scaler
- Potter-duff compatible blending operation
- Supports input format Semi-planar YUV422/YUV420/YUV411 and Planar YUV422/YUV420/YUV411, ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555/RGB565/palette
- Supports SmartColor2.0 for excellent display experience
  - Adaptive detail/edge enhancement
  - Adaptive color enhancement
  - Adaptive contrast enhancement and fresh tone rectify
- Supports write back for aux display

Figure 4-1 DE Block Diagram



4.2 DI

The De-interlacer (DI) converts the interlaced input video frame to progressive video frame.

The DI has the following features:

- Supports YUV420 (Planar/NV12/NV21) and YUV422 (Planar/NV16/NV61) data format
- Supports video resolution from 32 x 32 to 2048 x 1280 pixel
- Supports Inter-field interpolation/motion adaptive de-interlace method
- Performance: module clock 600M for 1080p@60Hz YUV420

4.3 G2D

The Graphic 2D (G2D) engine is hardware accelerator for 2D graphic.

The G2D has the following features:

- Supports layer size up to 2048 x 2048 pixels
- Supports pre-multiply alpha image data
- Supports color key
- Supports two pipes Porter-Duff alpha blending
- Supports multiple video formats 4:2:0, 4:2:2, 4:1:1 and multiple pixel formats (8/16/24/32 bits graphics layer)
- Supports memory scan order option
- Supports any format convert function
- Supports 1/16× to 32× resize ratio
- Supports 32-phase 8-tap horizontal anti-alias filter and 32-phase 4-tap vertical anti-alias filter
- Supports window clip
- Supports FillRectangle, BitBlit, StretchBlit and MaskBlit
- Supports horizontal and vertical flip, clockwise 0/90/180/270 degree rotate for normal buffer
- Supports horizontal flip, clockwise 0/90/270 degree rotate for LBC buffer

4.4 Video Decoding

4.4.1 Overview

The Video Decoding consists of Video Control Firmware (VCF) running on ARM processor and embedded hardware Video Engine (VE). VCF gets the bitstream from topper software, parses bitstream, invokes the Video Engine, and generates the decoding image sequence. The decoder image sequence is transmitted by the video output controller to the display device under the control of the topper software.

The Video Decoding has the following features:

- Supports H.265 MP@L4.1
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 60 Mbit/s, 1080p@60fps
- Supports H.264 BP/MP/HP@L4.2
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 60 Mbit/s, 1080p@60fps
- Supports H.263 BP
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 60 Mbit/s, 1080p@60fps
- Supports MPEG-4 SP/ASP L5
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 60 Mbit/s, 1080p@60fps
- Supports MPEG-2 MP/HL
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 60 Mbit/s, 1080p@60fps
- Supports MPEG-1 MP/HL
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 60 Mbit/s, 1080p@60fps
- Supports Xvid
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 60 Mbit/s, 1080p@60fps
- Supports Sorenson Spark

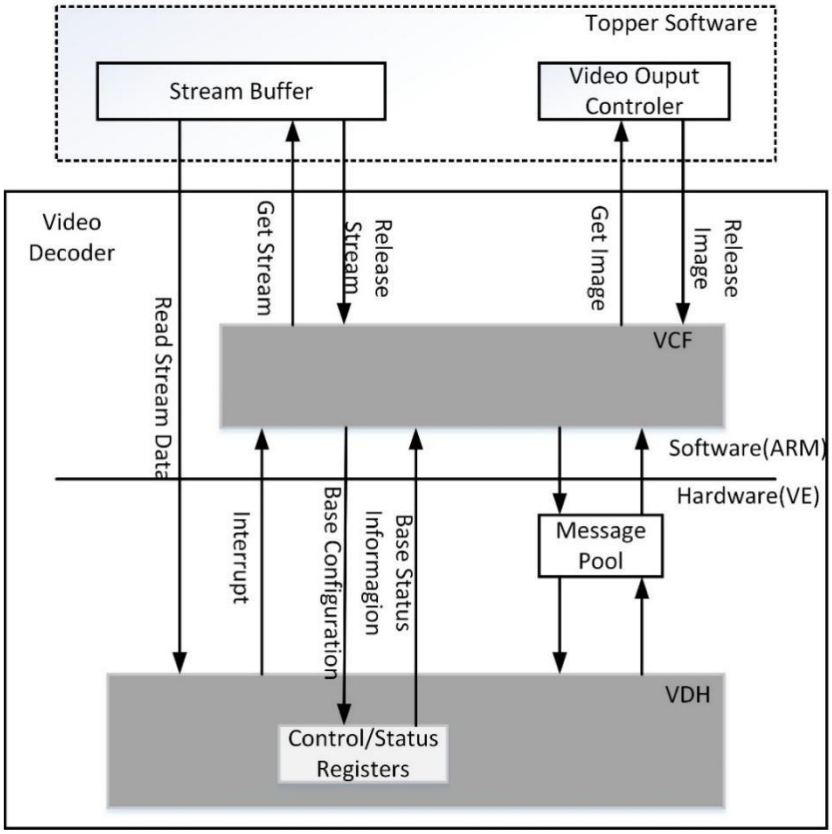
- Maximum video resolution: 1920 x 1080
- Maximum decoding rate: 60 Mbit/s, 1080p@60fps

- Supports WMV9/VC1 SP/MP/AP
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 60 Mbit/s, 1080p@60fps
- Supports MJPEG
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 60 Mbit/s, 1080p@30fps

4.4.2 Block Diagram

The functional block diagram of the Video Decoding is as follows.

Figure 4-2 Video Decoding Block Diagram



4.5 Video Encoding

4.5.1 Overview

The Video Encoding supports JPEG/MJPEG encoding (JPGE).

The JPGE is a high-performance JPEG encoder implemented by using hardware. It supports 64-megapixel snapshot or HD MJPEG encoding.

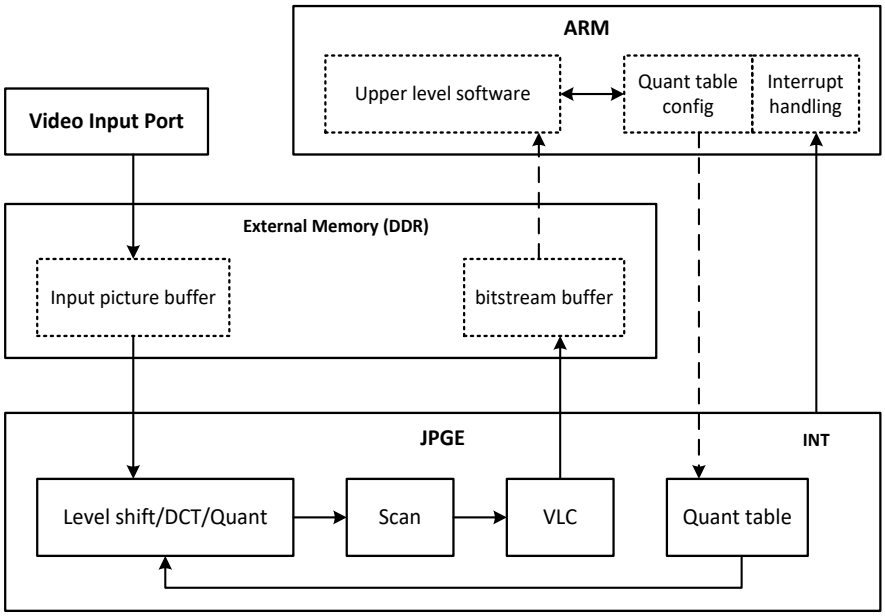
The JPGE has the following features:

- Supports ISO/IEC 10918-1 (CCITT T.81) baseline process (DCT sequential) encoding
- Encodes the pictures in the chrominance sampling format of YCbCr4:2:0 and YCbCr4:2:2
- Supports multiple input picture formats:
  - Semi-planar YCbCr4:2:0
  - Semi-planar YCbCr4:2:2
- Supports JPEG encoding with the performance of 1080p@60fps
- Supports configurable picture resolutions
  - Minimum picture resolution: 192 x 96
  - Maximum picture resolution: 4096 x 4096
- Supports the picture width or height step of 8
- Supports configurable quantization tables for the Y component, Cb component and Cr component respectively
- Supports OSD front-end overlapping
  - OSD overlaying before encoding for a maximum of 16 regions
  - OSD overlaying with any size and at any position (within the size and position range of the picture)
  - 16-level alpha blending
  - OSD overlaying control (enabled or disabled)
- Supports the color-to-gray function
- Supports the MJPEG output bit rate ranging from 2 kbit/s to 60 Mbit/s

4.5.2 Block Diagram

The functional block diagram of the JPGE is as follows.

Figure 4-3 JPGE Block Diagram



The JPGE realizes various protocol processing with large computation such as OSD, level shift, DCT, quantization, scanning, VLC encoding, and stream generation. The ARM software completes the encoding control processing such as quantization table configuration and interrupt processing.

Before the JPGE starts encoding, the software allocates two types of buffers mainly in the external DDR SDRAM:

- **Input picture buffer**

The JPGE reads the source pictures to be encoded from this buffer during encoding. This buffer is generally written by the Video Input Port module.

- **Stream buffer**

This buffer stores encoded streams. The JPGE writes streams to this buffer during encoding. This buffer is read by software.

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Figures

Tables

5 Video Output Interfaces

5.1 TCON LCD

5.1.1 Overview

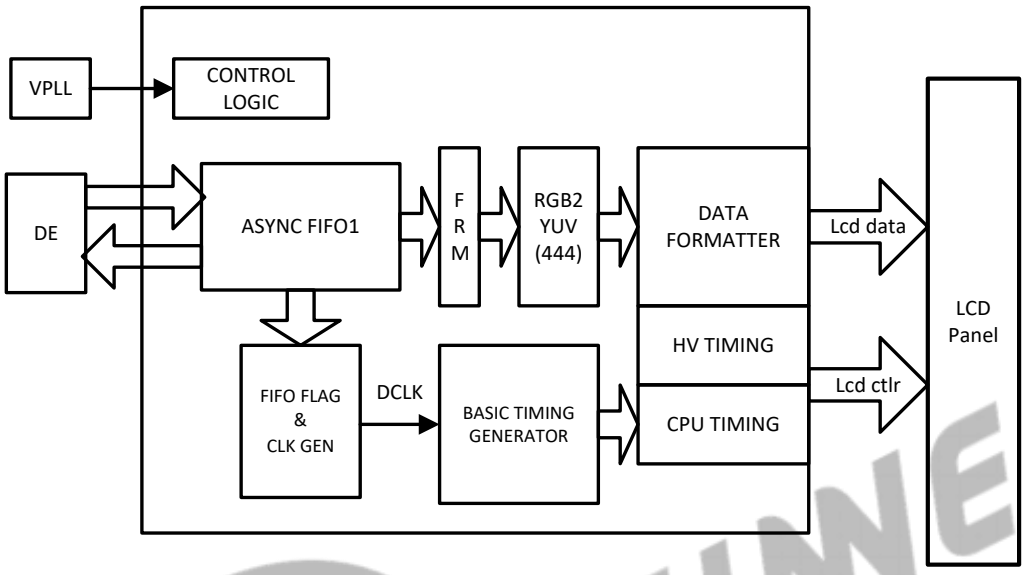
The Timing Controller_LCD (TCON_LCD) is a module that processes video signals received from system through a complicated arithmetic and then generates control signals and transmits them to the LCD panel driver IC.

The TCON_LCD includes the following features:

- Supports RGB interface with DE/SYNC mode, up to 1920 x 1080@60fps
- Supports serial RGB/dummy RGB interface, up to 800 x 480@60fps
- Supports LVDS interface with dual link, up to 1920 x 1080@60fps
- Supports LVDS interface with single link, up to 1366 x 768@60fps
- Supports i8080 interface, up to 800 x 480@60fps
- Supports BT656 interface for NTSC and PAL
- Supports RGB666 and RGB565 with dither function
- Supports Gamma correction with R/G/B channel independence

5.1.2 Block Diagram

Figure 5-1 TCON_LCD Block Diagram



5.1.3 Functional Description

5.1.3.1 External Signals

The LCD external signals are used to connect to panel interface. The panel interface has various types.

Table 5-1 LCD External Signals

Signal Name	Description	Type
LCD0-D[23:0]	LCD Data Output	O
LCD0-CLK	LCD Clock The pixel data are synchronized by this clock	O
LCD0-VSYNC	LCD Vertical Sync It indicates one new frame	O
LCD0-HSYNC	LCD Horizontal Sync It indicates one new scan line	O
LCD0-DE	LCD Data Output Enable	O
TCON-TRIG	LCD Sync (TCON outputs to LCD for sync)	O
LVDS0-CKP	LVDS0 Positive Port of Clock	O
LVDS0-CKN	LVDS0 Negative Port of Clock	O
LVDS0-V[3:0]P	LVDS0 Positive Port of Data Channel [3:0]	O

Signal Name	Description	Type
LVDS0-V[3:0]N	LVDS0 Negative Port of Data Channel [3:0]	O
LVDS1-CKP	LVDS1 Positive Port of Clock	O
LVDS1-CKN	LVDS1 Negative Port of Clock	O
LVDS1-V[3:0]P	LVDS1 Positive Port of Data Channel [3:0]	O
LVDS1-V[3:0]N	LVDS1 Negative Port of Data Channel [3:0]	O

For parallel RGB, the data of LCD is high-aligned. The correspondence is as follows.

Table 5-2 The Correspondence between LCD and RGB

LCD I/O	Parallel RGB I/O		
	RGB565	RGB666	RGB888
LCD0-D23	R4	R5	R7
LCD0-D22	R3	R4	R6
LCD0-D21	R2	R3	R5
LCD0-D20	R1	R2	R4
LCD0-D19	R0	R1	R3
LCD0-D18	-	R0	R2
LCD0-D17	-	-	R1
LCD0-D16	-	-	R0
LCD0-D15	G5	G5	G7
LCD0-D14	G4	G4	G6
LCD0-D13	G3	G3	G5
LCD0-D12	G2	G2	G4
LCD0-D11	G1	G1	G3
LCD0-D10	G0	G0	G2
LCD0-D9	-	-	G1
LCD0-D8	-	-	G0
LCD0-D7	B4	B5	B7
LCD0-D6	B3	B4	B6
LCD0-D5	B2	B3	B5
LCD0-D4	B1	B2	B4
LCD0-D3	B0	B1	B3
LCD0-D2	-	B0	B2
LCD0-D1	-	-	B1
LCD0-D0	-	-	B0

The multiplex relationship between LCD and LVDS is shown as follows.

Table 5-3 The Correspondence between LCD and LVDS

LCD I/O	LVDS I/O
LCD0-D2	LVDS0-V0P
LCD0-D3	LVDS0-V0N
LCD0-D4	LVDS0-V1P
LCD0-D5	LVDS0-V1N
LCD0-D6	LVDS0-V2P
LCD0-D7	LVDS0-V2N
LCD0-D10	LVDS0-CKP
LCD0-D11	LVDS0-CKN
LCD0-D12	LVDS0-V3P
LCD0-D13	LVDS0-V3N
LCD0-D14	LVDS1-V0P
LCD0-D15	LVDS1-V0N
LCD0-D18	LVDS1-V1P
LCD0-D19	LVDS1-V1N
LCD0-D20	LVDS1-V2P
LCD0-D21	LVDS1-V2N
LCD0-D22	LVDS1-CKP
LCD0-D23	LVDS1-CKN
LCD0-CLK	LVDS1-V3P
LCD0-DE	LVDS1-V3N

5.1.3.2 Control Signal and Data Port Mapping

		SYNC RGB				CPU Cmd	CPU 18-bit	CPU 16bit								CPU 8bit					CPU 9bit		LVDS		
External I/O	Internal pin	Para RGB	Serial RGB			CCIR 656		256K							65K	256K				65K	256K		Single Link		Dual Link
			1st	2nd	3rd			1st	2nd	3rd	1st	2nd	1st	2nd		1st	2nd	3rd	1st	2n	1st	2n	1	2	
LCD0_VSYN	IO0	VSYNC				CS																			
LCD0_HSYN	IO1	HSYNC				RD																			

LCD0_CLK	IO2	DCLK					WR																	D3P2	D3P2
LCD0_DE	IO3	DE					RS																	D3N2	D3N2
LCD0_D23	D23	R7					D23	R5	R5	B5	G5	R5		R5	B5	R4								CKN2	CKN2
LCD0_D22	D22	R6					D22	R4	R4	B4	G4	R4		R4	B4	R3								CKP2	CKP2
LCD0_D21	D21	R5					D21	R3	R3	B3	G3	R3		R3	B3	R2								D2N2	D2N2
LCD0_D20	D20	R4					D20	R2	R2	B2	G2	R2		R2	B2	R1								D2P2	D2P2
LCD0_D19	D19	R3					D19	R1	R1	B1	G1	R1		R1	B1	R0								D1N2	D1N2
LCD0_D18	D18	R2					D18	R0	R0	B0	G0	R0		R0	B0	G5								D1P2	D1P2
LCD0_D17	D17	R1					D17																		
LCD0_D16	D16	R0					D16																		
LCD0_D15	D15	G7					D15	G5								G4								D0N2	D0N2
LCD0_D14	D14	G6					D14	G4								G3								D0P2	D0P2
LCD0_D13	D13	G5					D13	G3															D3N1		D3N1
LCD0_D12	D12	G4	D71	D72	D73	D7	D12	G2	G5	R5	B5	G5	B5	G5		G2	R5	G5	B5	R4	G2	R5	G2	D3P1		D3P1
LCD0_D11	D11	G3	D61	D62	D63	D6	D11	G1	G4	R4	B4	G4	B4	G4		G1	R4	G4	B4	R3	G1	R4	G1	CKN1		CKN1
LCD0_D10	D10	G2	D51	D52	D53	D5	D10	G0	G3	R3	B3	G3	B3	G3		G0	R3	G3	B3	R2	G0	R3	G0	CKP1		CKP1
LCD0_D9	D9	G1					D9																		
LCD0_D8	D8	G0					D8																		
LCD0_D7	D7	B7	D41	D42	D43	D4	D7	B5	G2	R2	B2	G2	B2	G2		B4	R2	G2	B2	R1	B4	R2	B5	D2N1		D2N1
LCD0_D6	D6	B6	D31	D32	D33	D3	D6	B4	G1	R1	B1	G1	B1	G1		B3	R1	G1	B1	R0	B3	R1	B4	D2P1		D2P1
LCD0_D5	D5	B5	D21	D22	D23	D2	D5	B3	G0	R0	B0	G0	B0	G0		B2	R0	G0	B0	G5	B2	R0	B3	D1N1		D1N1
LCD0_D4	D4	B4	D11	D12	D13	D1	D4	B2								B1				G4	B1	G5	B2	D1P1		D1P1
LCD0_D3	D3	B3	D01	D02	D03	D0	D3	B1								B0				G3	B0	G4	B1	D0N1		D0N1
LCD0_D2	D2	B2					D2	B0														G3	B0	D0P1		D0P1
LCD0_D1	D1	B1					D1																			
LCD0_D0	D0	B0					D0																			

5.1.3.3 HV interface (Sync+DE mode)

HV I/F is also known as Sync + DE mode, which is widely used in TFT LCD module for PMP/MP4 applications.

Its signals are define as:

Table 5-4 HV Panel Signals

Signal Name	Description	Type
Vsync	Vertical sync, indicates one new frame	O
Hsync	Horizontal sync, indicates one new scan line	O
DCLK	Dot clock, pixel data are sync by this clock	O
DE	LCD data enable	O
D[23..0]	24-bit RGB output from input FIFO for panel	O

The timing diagram of HV interface is as follows.

Figure 5-2 HV Interface Vertical Timing

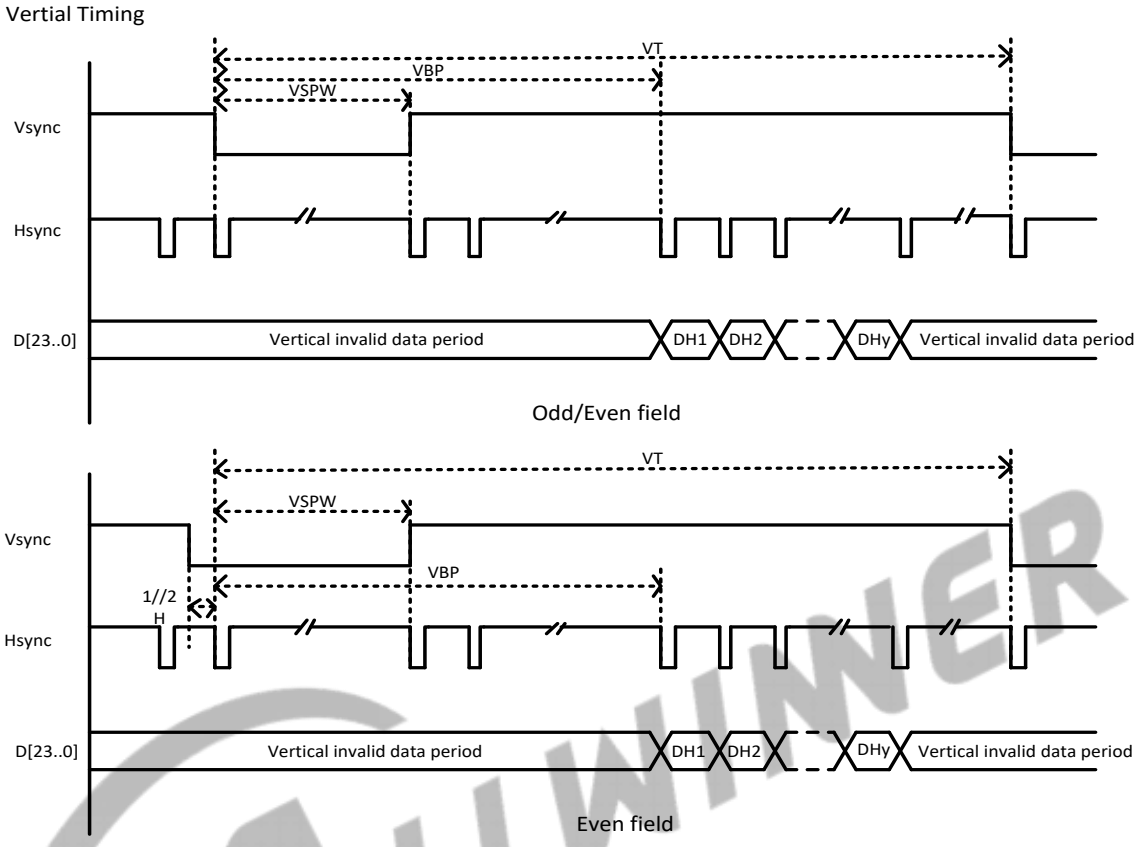
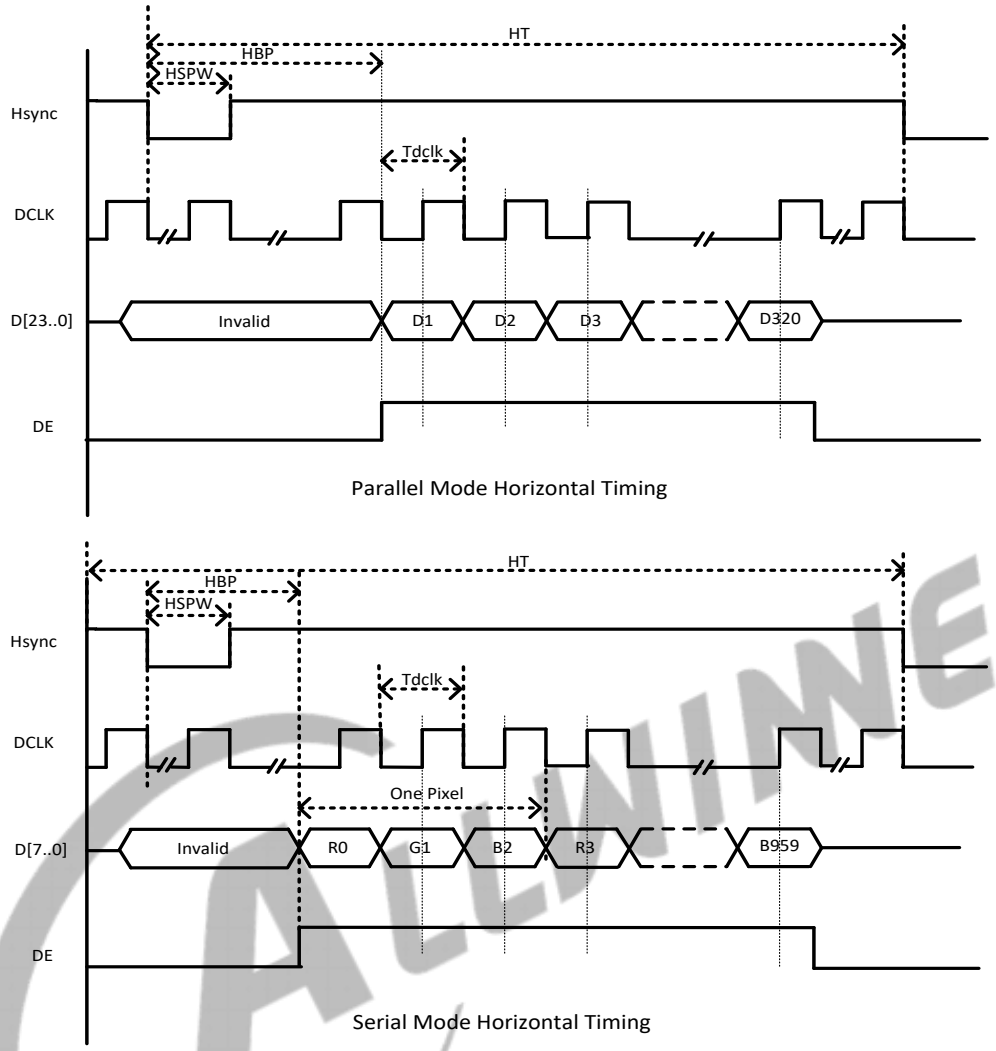


Figure 5-3 HV Interface Horizontal Timing



5.1.3.4 BT656 Interface

In HV serial YUV output mode, its timing is BT656 compatible. SAV adds right before active area every line; EAV adds right after active area every line.

Table 5-5 BT656 Panel Signals

Signal Name	Description	Type
DCLK	Clock signal	O
DATA[7:0]	Data signal	O

Its logic is:

F = “0” for Field 1 F = “1” for Field 2

V = “1” during vertical blanking

H = “0” at SAV H = “1” at EAV

P3-P0 = protection bits

P3 = V ⊕ H

P2 = F ⊕ H

P1 = F ⊕ V

P0 = F ⊕ V ⊕ H

Where ⊕ represents the exclusive-OR function.

The 4 byte SAV/EAV sequence is as follows.

Table 5-6 EAV and SAV Sequence

	8-bit Data								10-bit Data	
	D9 (MSB)	D8	D7	D6	D5	D4	D3	D2	D1	D0
Preamble	1	1	1	1	1	1	1	1	1	1
	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0
Status word	1	F	V	H	P3	P2	P1	P0	0	0

5.1.3.5 i8080 Interface

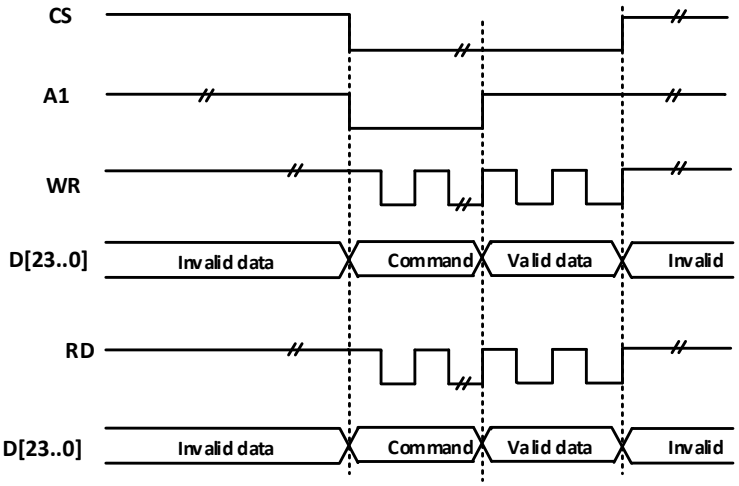
The i8080 I/F LCD panel is most common interface for small size, low resolution LCD panels. The CPU control signals are active low.

Table 5-7 CPU Panel Signals

Signal Name	Description	Type
CS	Chip select, active low	O
WR	Write strobe, active low	O
RD	Read strobe, active low	O
A1	Address bit, controlled by "LCD_CPUI/F" BIT26/25	O
D[23..0]	Digital RGB output signal	I/O

The following figure relationship between basic timing and CPU timing. WR is 180^{o} delay of DCLK; CS is active when pixel data is valid; RD is always set to 1; A1 is set by “LCD_CPUI/F”.

Figure 5-4 i8080 Interface Timing



When CPU I/F is in IDLE state, it can generate WR/RD timing by setting "**Lcd_CPUI/F**". The CS strobe is one DCLK width, and the WR/RD strobe is half DCLK width.

5.1.3.6 LVDS Interface

Table 5-8 LVDS Panel Signals

Signal Name	Description	Type
CKP	The positive port of clock	O
CKN	The negative port of clock	O
D0P	The positive port of data channel 0	O
D0N	The negative port of data channel 0	O
D1P	The positive port of data channel 1	O
D1N	The negative port of data channel 1	O
D2P	The positive port of data channel 2	O
D2N	The negative port of data channel 2	O
D3P	The positive port of data channel 3	O
D3N	The negative port of data channel 3	O

The following figures show the timing of LVDS interface.

Figure 5-5 LVDS Single Link JEDIA Mode Interface Timing

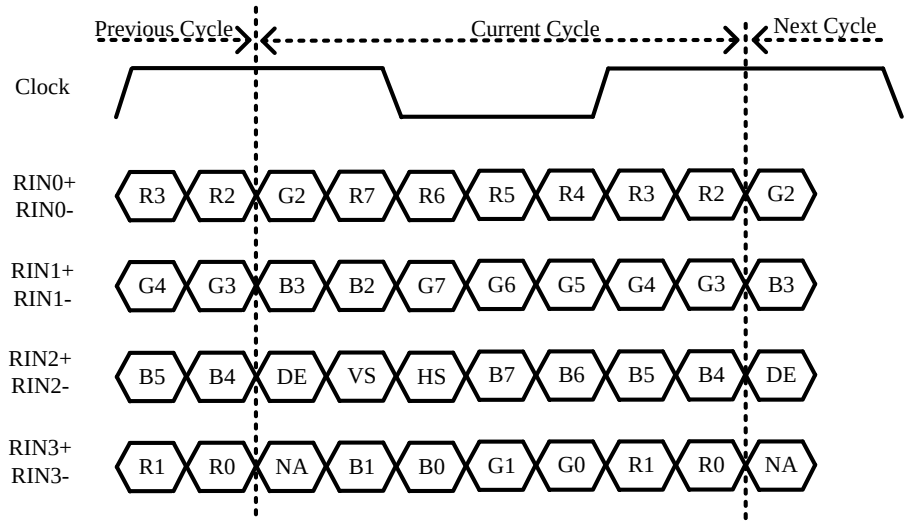


Figure 5-6 LVDS Single Link NS Mode Interface Timing

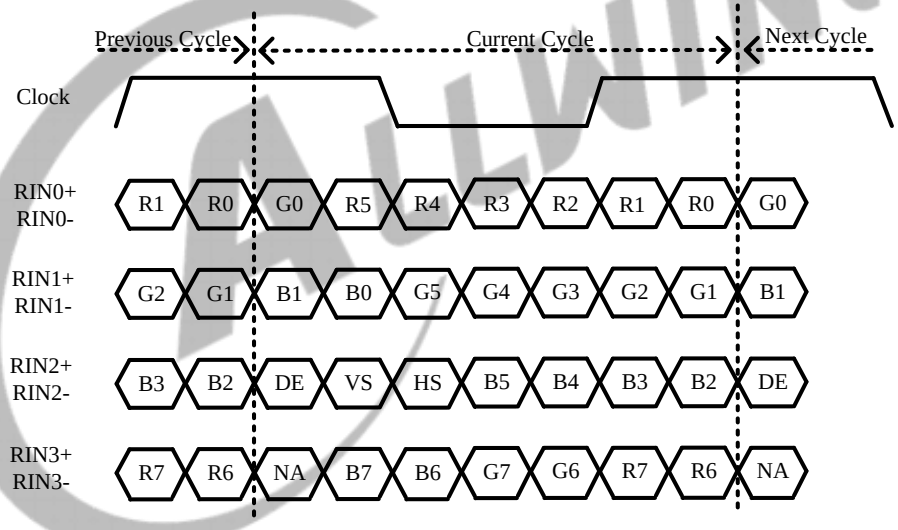
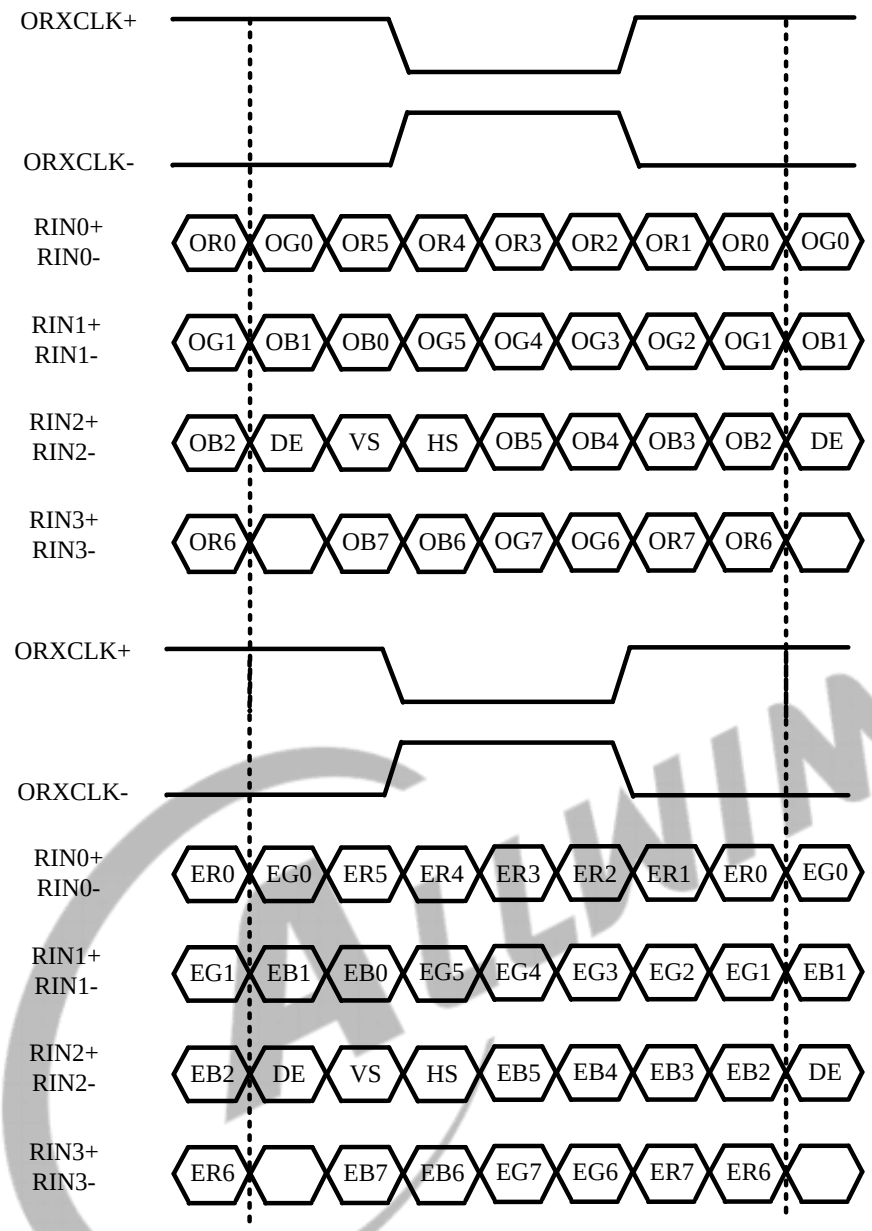


Figure 5-7 LVDS Dual Link NS Mode Interface Timing



5.1.3.7 Clock Sources

The following table describes the clock sources of TCON_LCD. Table 5-9 describes the clock sources of TCON_LCD.

Table 5-9 TCON_LCD Clock Sources

Clock Sources	Description
PLL_VIDEO0(1X)	By default, PLL_VIDEO0(4X) is 1188 MHz, PLL_VIDEO0(1X) is 297 MHz
PLL_VIDEO0(4X)	

Clock Sources	Description
PLL_VIDEO1(1X)	By default, PLL_VIDEO1(4X) is 1188 MHz, PLL_VIDEO1(1X) is 297 MHz
PLL_VIDEO1(4X)	
PLL_PERI(2X)	By default, PLL_PERI(2X) is 1.2 GHz
PLL_AUDIO1(DIV2)	By default, PLL_AUDIO1 is 3072 MHz, PLL_AUDIO1(DIV2) is 1536 MHz

5.1.3.8 RGB Gamma Correction

Function: This module correct the RGB input data of DE.

A 256*8*3 Byte register file is used to store the gamma table.

Table 5-10 RGB Gamma Correction Table

Offset	Value
0x400	{ B0[7:0], G0[7:0], R0[7:0] }
0x404	{ B1[7:0], G1[7:0], R1[7:0] }
.....	.....
0x7FC	{ B255[7:0], G255[7:0], R255[7:0] }

5.1.3.9 CEU Module

This module enhances color data from DE .

R' = Rr*R + Rg*G + Rb*B + Rc

G' = Gr*R + Gg*G + Gb*B + Gc

B' = Br*R + Bg*G + Bb*B + Bc

NOTE

Rr, Rg, Rb, Gr, Gg, Gb, Br, Bg, Bb s13 (-16, 16)

Rc, Gc, Bc s19 (-16384, 16384)

R, G, B u8 [0-255]

R' has the range of [Rmin ,Rmax]

G' has the range of [Rmin ,Rmax]

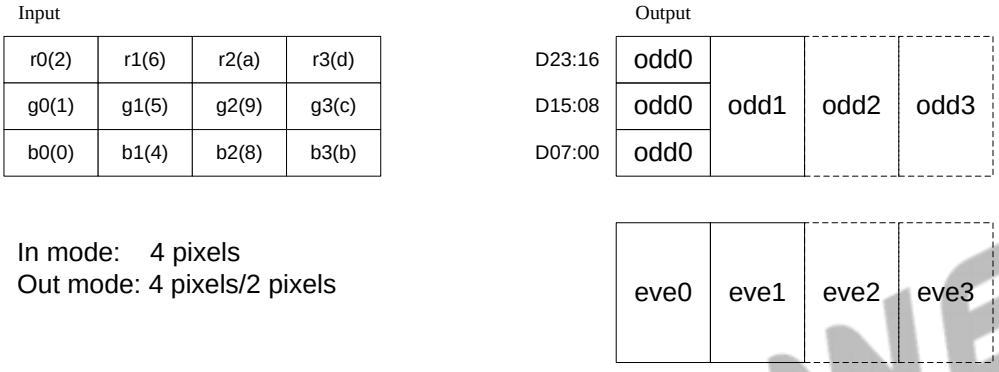
B' has the range of [Rmin ,Rmax]

5.1.3.10 CMAP Module

Function: This module map color data from DE.

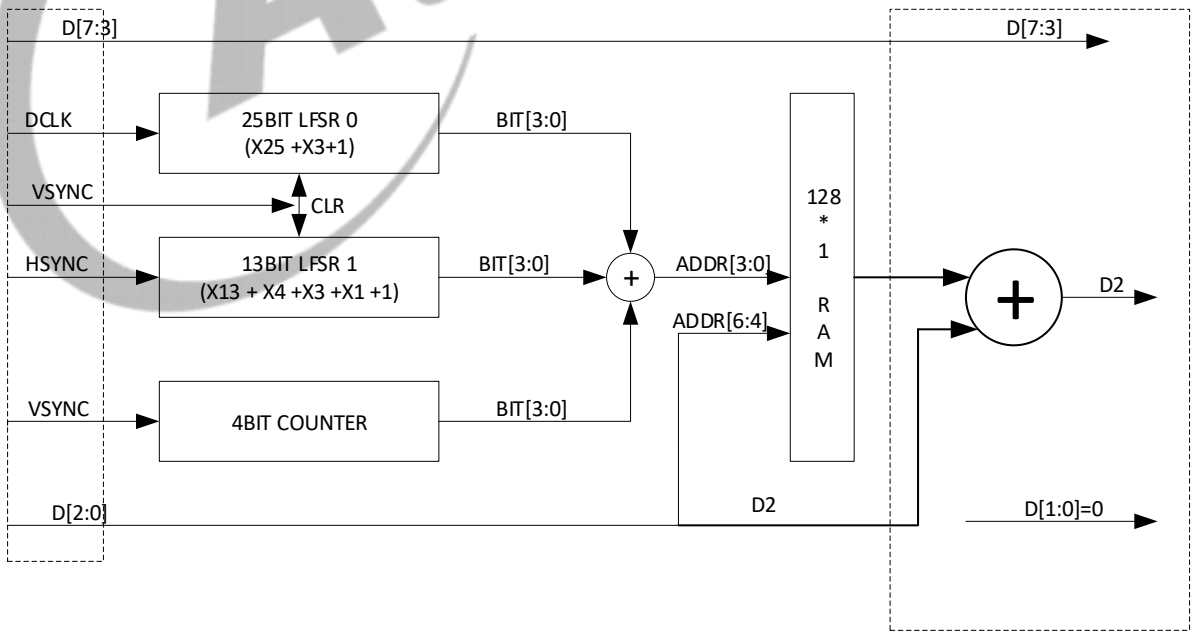
Every 4 input pixels are as a unit. A unit is divided into 12 bytes. Output byte can select one of those 12 bytes. Note that even line and odd line can be different, and output can be 12 bytes (4 pixels) or reduce to 6 bytes (2 pixels).

Figure 5-8 CMAP Module



5.1.3.11 FRM Module

Figure 5-9 FRM Module



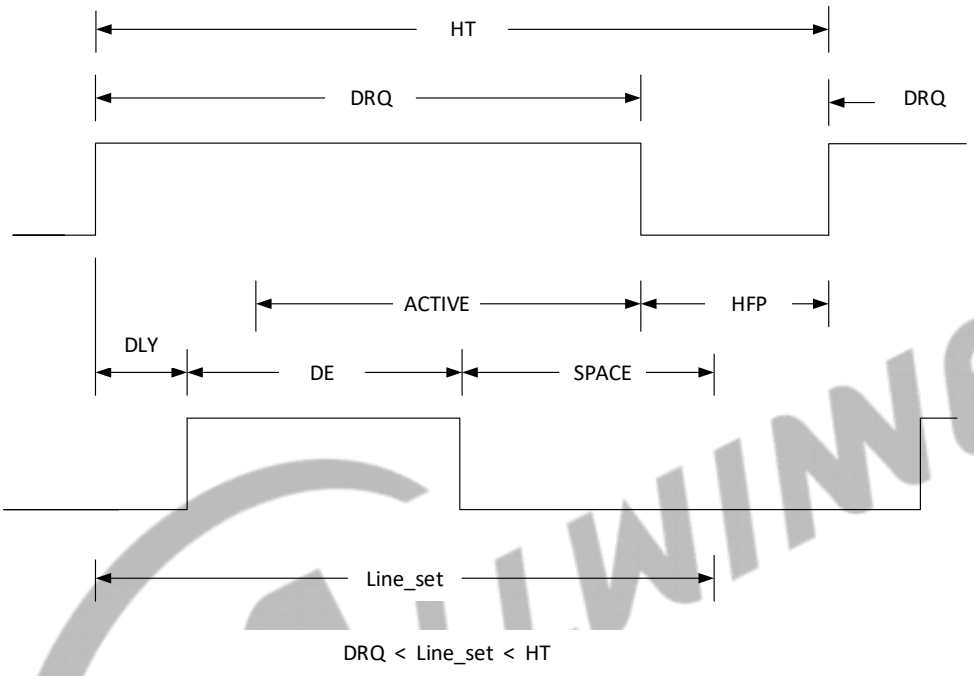
5.1.3.12 MIPI DSI

The requirements on MIPI DSI mode are as follows.

(1). When using MIPI DSI as display interface, the data clk of TCON needs be started firstly.

(2). When it is used with DSI video mode, the setting of block space needs to meet the following relationship.

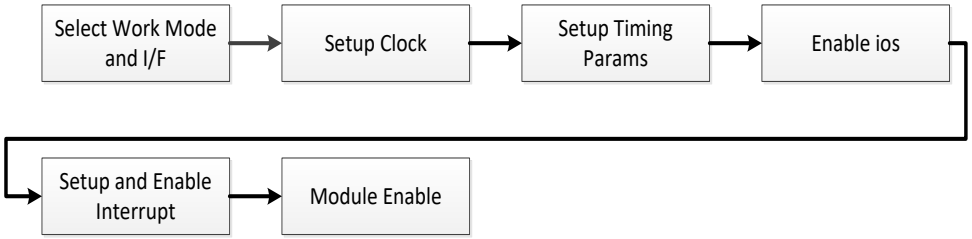
Figure 5-10 The Data Timing of MIPI DSI Video Mode



5.1.4 Programming Guidelines

5.1.4.1 HV Mode Configuration Process

Figure 5-11 HV Mode Initial Process



(1) Parallel RGB

Step 1 Select HV interface type

Configure LCD_CTL_REG[LCD_IF] (reg0x40) to 0 to select HV (Sync+DE) mode, and configure LCD_HV_IF_REG[HV_MODE] (reg0x58) to 0 to select 24bit/1cycle parallel mode.

lcd_dev[sel]->lcd_ctl.lcd_if = HV(Sync+DE);

lcd_dev[sel]->lcd_ctl.src_sel = src; //src = DE/color/grayscale/...

lcd_dev[sel]->lcd_hv_ctl.hv_mode = 24bit/1cycle parallel mode;

Step 2 Clock configuration

NOTE

- In parallel RGB mode, the displayed pixel clock (pixel_CLK) is required to be consistent with the DCLK, the pixel_clk(pixel_clk=Ht*Vt*frame rate) is decided by external LCD.
- When using phase adjustment function, the LCD_IO_POL_REG.DCLK_SEL (reg0x88) selects dclk0–2 of different phase, and LCD_IO_POL_REG.IO2_INV can achieve 180°phase delay.

Configure corresponding frequency by setting PLL_VIDEO0/1 register, and configure TCON LCD0 Clock register.

Configure internal frequency division of TCON_LCD. Based on clock source of TCON and DCLK clock ratio, configure LCD_DCLK_REG[LCD_DCLK_DIV]. If using phase adjustment function, LCD_DCLK_REG[LCD_DCLK_EN] needs be set, usually is 0xf. When the dclk1 and dclk2 in LCD_DCLK_REG[LCD_DCLK_EN] are used, the value of LCD_DCLK_REG[LCD_DCLK_DIV] needs no less than 6.

lcd_dev[sel]->lcd_dclk.dclk_en = en;

lcd_dev[sel]->lcd_dclk.dclk_div = div;

Step 3 Set sequence parameters

The sequence parameters include x,ht,hbp,hspw,y,vt,vbp,vspw, and correspond to LCD_BASE_REG from reg0x48 to reg 0x54. Note that hbp includes hspw, and vbp includes vspw. And LCD_BASE2_REG.VT needs be set to the twice of the actual value.

lcd_dev[sel]->lcd_basic0.x = x-1;

lcd_dev[sel]->lcd_basic0.y = y-1;

lcd_dev[sel]->lcd_basic1.ht = ht-1;

lcd_dev[sel]->lcd_basic1.hbp = hbp-1;

lcd_dev[sel]->lcd_basic2.vt = vt*2;

lcd_dev[sel]->lcd_basic2.vbp = vbp-1;

lcd_dev[sel]->lcd_basic3.hspw = hspw-1;

lcd_dev[sel]->lcd_basic3.vspw = vspw-1;

Step 4 Open IO output

Set the corresponding data IO enable and control signal IO enable of LCD_IO_TRI_REG (reg0x8C) to 0 to start enable. Note that except the internal IO of TCON_LCD, the external GPIO mapping needs to be set to LCD mode.

When some control signals require polarity reversal, it can realize by setting LCD_IO_POL_REG.IO0~3_INV (reg0x88).

Step 5 Set and open interrupt function

The LCD_GINT0_REG (reg0x4) controls interrupt mode and flag, and the LCD_GINT1_REG (reg0x8) sets the interrupt line position of Line interrupt mode.

V interrupt:

lcd_dev[sel]->lcd_gint0.vb_en = 1;

Line interrupt:

lcd_dev[sel]->lcd_gint1.lcd_line_int_num = line;

lcd_dev[sel]->lcd_gint0.line_en = 1;

Step 6 Open module enable

Enable LCD_CTL_REG.LCD_EN (reg0x40) and LCD_GCTL_REG.LCD_EN (reg0x00).

lcd_dev[sel]->lcd_ctl.lcd_en = 1;

lcd_dev[sel]->lcd_gctl.lcd_en = 1;

(2) Serial RGB

The serial RGB mode is consistent with parallel RGB mode, the main difference is the definition of clock and the sequence of serial data. The difference is as follows.

Step 1 Select HV interface type

Set LCD_CTL_REG.LCD_IF (reg0x40) to 0 to select HV(Sync+DE) mode; set LCD_HV_IF_REG.HV_MODE (reg0x58) to select 8bit/3cycle RGB serial mode (RGB888), 8bit/4cycle Dummy RGB mode (DRGB) or 8bit/4cycle RGB Dummy mode (RGBD).

lcd_dev[sel]->lcd_ctl.lcd_if = HV(Sync+DE);

lcd_dev[sel]->lcd_ctl.src_sel = src; //src = DE/color/grayscale/...

lcd_dev[sel]->lcd_hv_ctl.hv_mode = Serial mode;

Step2、Step3: Set clock and sequence parameters

In serial RGB mode, DCLK is the transfer clock of each byte data. In the same resolution, pixel_clk of serial RGB is three times of its clock in parallel RGB, and ht,hbp,hspw own the same conversion relation. When display is split into odd field and even field, LCD_BASE2_REG.VT needs not to be set to the twice of the actual value.

lcd_dev[sel]->lcd_basic2.vt = vt;

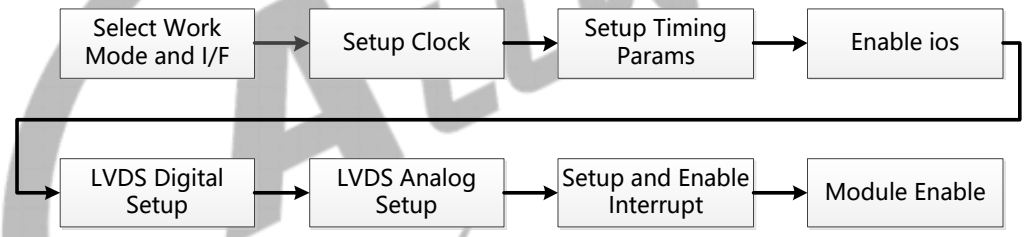
Set LCD_HV_IF_REG.RGB888_ODD_ORDER/LCD_HV_IF_REG.RGB888_ODD_EVEN to select RGB output sequence of the selected odd and even lines.

lcd_dev[lcd_sel]->lcd_hv_ctl.srgb_seq_even = seq_even;

lcd_dev[lcd_sel]->lcd_hv_ctl.srgb_seq_odd = seq_odd;

5.1.4.2 LVDS Mode Configuration Process

Figure 5-12 LVDS Mode Configuration Process



The LVDS interface configuration process is similar to the parallel mode of HV mode, and adds the digital/analog configuration of LVDS interface.

Step 1 Same as in step1 of parallel mode

Step 2 Clock configuration

NOTE

In parallel mode, the displayed pixel clock (pixel_CLK) is required to be consistent with the DCLK, pixel_clk=Ht*Vt*frame rate.

- Configure LCD_DCLK_REG.LCD_DCLK_DIV (reg0x44) to 7 after DCLK is determined;
- Configure the PLL clock in CCU based on proportional relationship;

- Release the LVDS reset of TCON LCD BUS GATING RESET register;
- Other configurations remain unchanged.

```
lcd_dev[sel]->lcd_dclk.dclk_en = en;
lcd_dev[sel]->lcd_dclk.dclk_div = 7;
```

Step 3 **Same as in step3 of parallel mode**

Step 4 **Same as in step4 of parallel mode**

Step 5 **LVDS digital logic configuration**

Includes clock source select of module, LVDS link number, data mode and bit width configuration.

- Configure LCD_LVDS_IF_REG.LCD_LVDS_CLK_SEL (reg0x84) to set LCD CLK;
- Configure LCD_LVDS_IF_REG.LCD_LVDS_LINK to set the required LVDS port number;
- Configure LCD_LVDS_IF_REG.LCD_LVDS_MODE to set JEDIA and NS mode;
- Configure LCD_LVDS_IF_REG.LCD_LVDS_BITWIDTH to select 24-bit or 18-bit width;
- Lastly configure LCD_LVDS_IF_REG.LCD_LVDS_EN to start LVDS mode.

```
lcd_dev[sel]->lcd_lvds_ctl.lvds_link = link_num-1;
lcd_dev[sel]->lcd_lvds_ctl.lvds_mode = mode;
lcd_dev[sel]->lcd_lvds_ctl.lvds_bitwidth = bitwidth;
lcd_dev[sel]->lcd_lvds_ctl.lvds_clk_sel = clk_src;
lcd_dev[sel]->lcd_lvds_ctl.lvds_en = 1;
```

NOTE

If configuring the same source data output mode of dual link, except the reg0x84 register of TCON_LCD0 needs be configured, the LCD_LVDS_IF_REG.LCD_LVDS_CLK_SEL, LCD_LVDS_IF_REG.LCD_LVDS_LINK, LCD_LVDS_IF_REG.LCD_LVDS_MODE, and LCD_LVDS_IF_REG.LCD_LVDS_BITWIDTH of the reg0x244 register need be configured.

Step 6 **LVDS controller configuration**

NOTE

The TCON LCD0 PHY0 is controlled by COMBO_PHY_REG (reg0x1110, reg0x1114). The TCON LCD0 PHY1 is controlled by LCD_LVDS0_ANA_REG (reg0x220).

For PHY0:

- Configure the reg_verf1p6 (differential mode voltage) in reg0x1114 to 4;
- Configure the reg_vref0p8 reg0x1114 (common mode voltage) in reg0x1114 to 3;
- Start en_cp, en_mipi, en_lvds, and en_comboldo in reg0x1110, in turn.

For PHY1:

The LVDS analog configuration process is to start clock and data channel, and set the common mode and differential mode voltage, and start module power.

- Configure LVDS_HPREN_DRVC and LVDS_HPREN_DRV. When LVDS signal is 18-bit, LVDS_HPREN_DRV=0x7; when LVDS signal is 24-bit, LVDS_HPREN_DRV=0xF;
- Configure LVDS0_REG_C (differential mode voltage) to 4;
- Configure LVDS0_REG_V (common mode voltage) to 3;
- Lastly, start module voltage, and enable EN_LVDS and EN_24M.

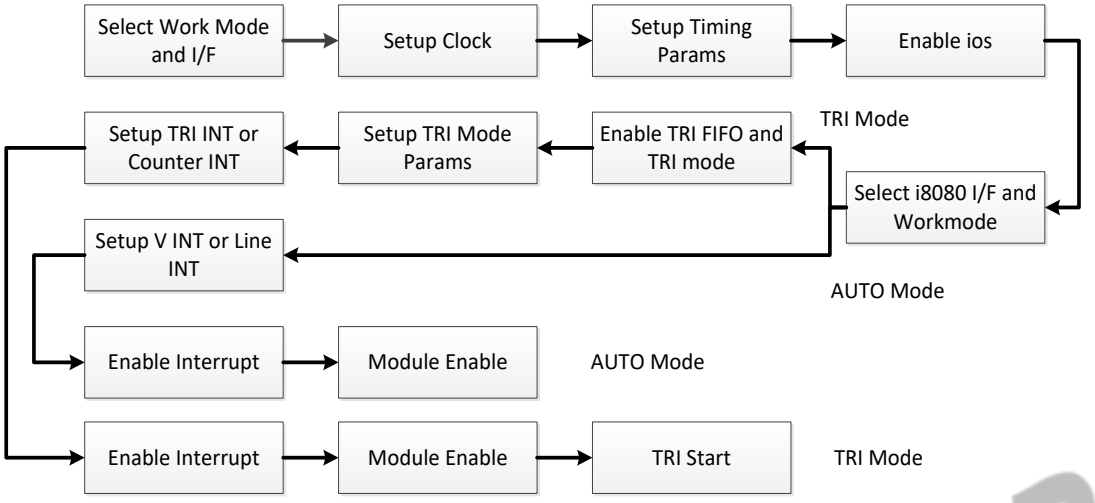
```
lcd_dev[sel]->lcd_lvds_ana_ctl[lvds_num].bits.en_drvd = 0x7; //18-bit=0x7, 24-bit=0xf
lcd_dev[sel]->lcd_lvds_ana_ctl[lvds_num].bits.en_drvc = 1;
lcd_dev[sel]->lcd_lvds_ana_ctl[lvds_num].bits.diff_level = diff;
lcd_dev[sel]->lcd_lvds_ana_ctl[lvds_num].bits.com_level = com;
lcd_dev[sel]->lcd_lvds_ana_ctl[lvds_num].bits.dual_src = link_src;
lcd_dev[sel]->lcd_lvds_ana_ctl[lvds_num].bits.en_24M = 1;
lcd_dev[sel]->lcd_lvds_ana_ctl[lvds_num].bits.en_lvds = 1;
lcd_dev[sel]->lcd_lvds_ana_ctl[lvds_num].bits.en_mb = 1;
```

Step 7 **Same as in step5 of parallel mode**

Step 8 **Same as in step6 of parallel mode**

5.1.4.3 i8080 Mode Configuration Process

Figure 5-13 i8080 Mode Initial Process



Step 1 Select i8080 interface type.

Step 2 The step is the same as HV mode, but pulse adjustment function is invalid.

Step 3 The step is the same as HV mode. When using TRI mode, it is best to configure LCD timing parameters in HV mode , or a handful of functions such as CMAP will not be able to apply.

Step 4 The step is the same as HV mode.

Step 5 Select type and operating mode of i8080, the operating mode includes TRI mode and AUTO mode, and the two operating modes are different.

----------**For TRI mode**----------

Step 6 Open TRI FIFO switch, and TRI mode function.

Step 7 Set parameters of TRI mode, including block size, block space and block number.

NOTE

When output interface is parallel mode, then the setting value of block space parameter is not less than 20.

When output interface is 2 cycle serial mode, then the setting value of block space parameter is not less than 40.

When output interface is 3 cycle serial mode, then the setting value of block space parameter is not less than 60.

When output interface is 4 cycle serial mode, then the setting value of block space parameter is not less than 80.

Step 8 Set the tri interrupt or counter interrupt. When using the two interrupts, mainly in the interrupt service function the tri start operation need be operated (the bit1 of LCD_CPU_IF_REG is set to"1"). If using TE trigger interrupt, you select the external input pin as a trigger signal, the 24-bit for offset 0x8C register is set to "1", to open up input of pad.

Step 9 Open the total switch of interrupt.

Step 10 Open the total enable of interrupt.

Step 11 Operate “tri start” operation (the bit1 of LCD_CPU_IF_REG is set to "1").

----------**For Auto mode**----------

Step 6 Set and open V interrupt or Line interrupt, the step is the same as HV mode.

Step 7 Open module total enable.

5.1.5 Register List

Module Name	Base Address
TCON_LCD0	0x05461000

Register Name	Offset	Description
LCD_GCTL_REG	0x0000	LCD Global Control Register
LCD_GINT0_REG	0x0004	LCD Global Interrupt Register0
LCD_GINT1_REG	0x0008	LCD Global Interrupt Register1
LCD_FRM_CTL_REG	0x0010	LCD FRM Control Register
LCD_FRM_SEED_REG	0x0014+N*0x04	LCD FRM Seed Register (N=0,1,2,3,4,5)
LCD_FRM_TAB_REG	0x002C+N*0x04	LCD FRM Table Register (N=0,1,2,3)
LCD_3D_FIFO_REG	0x003C	LCD 3D FIFO Register
LCD_CTL_REG	0x0040	LCD Control Register
LCD_DCLK_REG	0x0044	LCD Data Clock Register
LCD_BASIC0_REG	0x0048	LCD Basic Timing Register0
LCD_BASIC1_REG	0x004C	LCD Basic Timing Register1
LCD_BASIC2_REG	0x0050	LCD Basic Timing Register2
LCD_BASIC3_REG	0x0054	LCD Basic Timing Register3
LCD_HV_IF_REG	0x0058	LCD HV Panel Interface Register
LCD_CPU_IF_REG	0x0060	LCD CPU Panel Interface Register
LCD_CPU_WR_REG	0x0064	LCD CPU Panel Write Data Register
LCD_CPU_RD0_REG	0x0068	LCD CPU Panel Read Data Register0
LCD_CPU_RD1_REG	0x006C	LCD CPU Panel Read Data Register1

Register Name	Offset	Description
LCD_LVDS_IF_REG	0x0084	LCD LVDS Configure Register
LCD_IO_POL_REG	0x0088	LCD IO Polarity Register
LCD_IO_TRI_REG	0x008C	LCD IO Control Register
LCD_DEBUG_REG	0x00FC	LCD Debug Register
LCD_CEU_CTL_REG	0x0100	LCD CEU Control Register
LCD_CEU_COEF_MUL_REG	0x0110+N*0x04	LCD CEU Coefficient Register0 (N=0–10)
LCD_CEU_COEF_ADD_REG	0x011C+N*0x10	LCD CEU Coefficient Register1 (N=0,1,2)
LCD_CEU_COEF_RANG_REG	0x0140+N*0x04	LCD CEU Coefficient Register2 (N=0,1,2)
LCD_CPU_TRI0_REG	0x0160	LCD CPU Panel Trigger Register0
LCD_CPU_TRI1_REG	0x0164	LCD CPU Panel Trigger Register1
LCD_CPU_TRI2_REG	0x0168	LCD CPU Panel Trigger Register2
LCD_CPU_TRI3_REG	0x016C	LCD CPU Panel Trigger Register3
LCD_CPU_TRI4_REG	0x0170	LCD CPU Panel Trigger Register4
LCD_CPU_TRI5_REG	0x0174	LCD CPU Panel Trigger Register5
LCD_CMAP_CTL_REG	0x0180	LCD Color Map Control Register
LCD_CMAP_ODD0_REG	0x0190	LCD Color Map Odd Line Register0
LCD_CMAP_ODD1_REG	0x0194	LCD Color Map Odd Line Register1
LCD_CMAP_EVEN0_REG	0x0198	LCD Color Map Even Line Register0
LCD_CMAP_EVEN1_REG	0x019C	LCD Color Map Even Line Register1
LCD_SAFE_PERIOD_REG	0x01F0	LCD Safe Period Register
LCD_LVDS0_ANA_REG	0x0220	LCD LVDS Analog Register 0
LCD_LVDS1_ANA_REG	0x0224	LCD LVDS Analog Register 1
LCD_SYNC_CTL_REG	0x0230	LCD Sync Control Register
LCD_SYNC_POS_REG	0x0234	LCD Sync Position Register
LCD_SLAVE_STOP_POS_REG	0x0238	LCD Slave Stop Position Register
LCD_GAMMA_TABLE_REG	0x0400-0x07FF	LCD Gamma Table Register

5.1.6 Register Description

5.1.6.1 0x0000 LCD Global Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: LCD_GCTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	LCD_EN When it is disabled, the module will be reset to idle state. 0: Disable 1: Enable
30	R/W	0x0	LCD_GAMMA_EN Enable the Gamma correction function. 0: Disable 1: Enable
29:0	/	/	/

5.1.6.2 0x0004 LCD Global Interrupt Register0 (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: LCD_GINT0_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	LCD_VB_INT_EN Enable the Vb interrupt 0: Disable 1: Enable
30	/	/	/
29	R/W	0x0	LCD_LINE_INT_EN Enable the line interrupt 0: Disable 1: Enable
28	/	/	/
27	R/W	0x0	LCD_TRI_FINISH_INT_EN Enable the trigger finish interrupt 0: Disable 1: Enable
26	R/W	0x0	LCD_TRI_COUNTER_INT_EN Enable the trigger counter interrupt 0: Disable 1: Enable
25:16	/	/	/

Offset: 0x0004			Register Name: LCD_GINT0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
15	R/W0C	0x0	LCD_VB_INT_FLAG Asserted during vertical no-display period every frame Write 0 to clear it.
14	/	/	/
13	R/W0C	0x0	LCD_LINE_INT_FLAG Trigger when SY0 match the current LCD scan line Write 0 to clear it.
12	/	/	/
11	R/W0C	0x0	LCD_TRI_FINISH_INT_FLAG Trigger when cpu trigger mode finished Write 0 to clear it.
10	R/W0C	0x0	LCD_TRI_COUNTER_INT_FLAG Trigger when tri counter reaches this value Write 0 to clear it.
9	R/W0C	0x0	LCD_TRI_UNDERFLOW_FLAG Only used in dsi video mode, tri when sync by dsi but not finish Write 0 to clear it.
8:3	/	/	/
2	R/W0C	0x0	FSYNC_INT_INV Enable the fsync interrupt to set signal inverse polarity. When FSYNC is positive, this bit must be 1. And vice versa.
1	R/W0C	0x0	DE_INT_FLAG Asserted at the first valid line in every frame Write 0 to clear it.
0	R/W0C	0x0	FSYNC_INT_FLAG Asserted at the fsync signal in every frame Write 0 to clear it.

5.1.6.3 0x0008 LCD Global Interrupt Register1 (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: LCD_GINT1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	LCD_LINE_INT_NUM Scan line for LCD line trigger (including inactive lines). Setting it for the specified line for trigger0. **Note: SY0 is writable only when LINE_TRG0 is disabled.**
15:0	/	/	/

5.1.6.4 0x0010 LCD FRM Control Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: LCD_FRM_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	LCD_FRM_EN Enable the dither function 0: Disable 1: Enable
30:7	/	/	/
6	R/W	0x0	LCD_FRM_MODE_R The R component output bits in dither function 0: 6-bit frm output 1: 5-bit frm output
5	R/W	0x0	LCD_FRM_MODE_G The G component output bits in dither function 0: 6-bit frm output 1: 5-bit frm output
4	R/W	0x0	LCD_Frm_MODE_B The B component output bits in dither function 0: 6-bit frm output 1: 5-bit frm output
3:2	/	/	/
1:0	R/W	0x0	LCD_FRM_TEST Set the test mode of dither function 00: FRM 01: Half 5-/6-bit, half FRM 10: Half 8-bit, half FRM 11: Half 8-bit, half 5-/6-bit

5.1.6.5 0x0014+ N*0x04 (N=0–5) LCD FRM Seed Register (Default Value: 0x0000_0000)

Offset: 0x0014+N*0x04 (N=0–5)			Register Name:
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/

Offset: 0x0014+N*0x04 (N=0–5)			Register Name:
Bit	**Read/Write**	**Default/Hex**	**Description**
24:0	R/W	0x0	SEED_VALUE Set the seed used in dither function N=0: Pixel_Seed_R N=1: Pixel_Seed_G N=2: Pixel_Seed_B N=3: Line_Seed_R N=4: Line_Seed_G N=5: Line_Seed_B **Note: Avoid setting it to 0.**

5.1.6.6 0x002C+ N*0x04 (N=0–3) LCD FRM Table Register (Default Value: 0x0000_0000)

Offset: 0x002C+N*0x04 (N=0–3)			Register Name: LCD_FRM_TAB_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	FRM_TABLE_VALUE Set the data used in dither function Usually set as follows: Table0 = 0x01010000 Table1 = 0x15151111 Table2 = 0x57575555 Table3 = 0x7f7f7777

5.1.6.7 0x003C LCD 3D FIFO Register (Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: LCD_3D_FIFO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	3D_FIFO_BIST_EN Enable the 3D fifo bist test function 0: Disable 1: Enable
30:14	/	/	/
13:4	R/W	0x0	3D_FIFO_HALF_LINE_SIZE The number of data in half line=3D_FIFO_HALF_LINE_SIZE+1, only valid when 3D_FIFO_SETTING is set as 2.
3:2	/	/	/

Offset: 0x003C			Register Name: LCD_3D_FIFO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
1:0	R/W	0x0	3D_FIFO_SETTING Set the work mode of 3D FIFO 00: Bypass 01: Used as normal FIFO 10: Used as 3D interlace FIFO 11: Reserved

5.1.6.8 0x0040 LCD Control Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: LCD_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	LCD_EN It executes at the beginning of the first blank line of LCD timing. 0: Disable 1: Enable
30:26	/	/	/
25:24	R/W	0x0	LCD_IF Set the interface type of LCD controller. 00: HV(Sync+DE) 01: 8080 I/F 1x: Reserved
23	R/W	0x0	LCD_RB_SWAP Enable the function to swap red data and blue data in fifo1. 0: Default 1: Swap RED and BLUE data at FIFO1
22	/	/	/
21	R/W	0x0	LCD_FIFO1_RST Writing 1 and then 0 to this bit will reset FIFO 1 Note: 1 holding time must more than 1 DCLK
20	R/W	0x0	LCD_INTERLACE_EN This flag is valid only when LCD_EN == 1 0: Disable 1: Enable
19:9	/	/	/
8:4	R/W	0x0	LCD_START_DLY The unit of delay is T_{line}. Note: Valid only when LCD_EN == 1
3	/	/	/

Offset: 0x0040			Register Name: LCD_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
2:0	R/W	0x0	LCD_SRC_SEL LCD Source Select 000: DE 001: Color Check 010: Grayscale Check 011: Black by White Check 100: Test Data all 0 101: Test Data all 1 110: Reversed 111: Gridding Check

5.1.6.9 0x0044 LCD Data Clock Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: LCD_DCLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	LCD_DCLK_EN LCD clock enable 0000: dclk_en = 0; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 0; 0001: dclk_en = 1; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 0; 0010: dclk_en = 1; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 1; 0011: dclk_en = 1; dclk1_en = 1; dclk2_en = 0; dclkm2_en = 0; 0101: dclk_en = 1; dclk1_en = 0; dclk2_en = 1; dclkm2_en = 0; 1111: dclk_en = 1; dclk1_en = 1; dclk2_en = 1; dclkm2_en = 1; Others:Reversed
27:7	/	/	/
6:0	R/W	0x0	LCD_DCLK_DIV Tdclk = Tsclk/DCLKDIV Note: 1.If dclk1&dclk2 are used, DCLKDIV >=6 2.If only dclk is used, DCLKDIV >=1

5.1.6.10 0x0048 LCD Basic Timing Register0 (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: LCD_BASIC0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	WIDTH_X Panel width is X+1

Offset: 0x0048			Register Name: LCD_BASIC0_REG
Bit	Read/Write	Default/Hex	Description
15:12	/	/	/
11:0	R/W	0x0	HEIGHT_Y Panel height is Y+1

5.1.6.11 0x004C LCD Basic Timing Register1 (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: LCD_BASIC1_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	HT Thcycle = (HT+1) * Tdclk Computation: 1) parallel: HT = X + BLANK Limitation: 1) parallel: HT >= (HBP +1) + (X+1) +2 2) serial 1: HT >= (HBP +1) + (X+1) *3+2 3) serial 2: HT >= (HBP +1) + (X+1) *3/2+2
15:12	/	/	/
11:0	R/W	0x0	HBP Horizontal back porch (in dclk) Thbp = (HBP +1) * Tdclk

5.1.6.12 0x0050 LCD Basic Timing Register2 (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: LCD_BASIC2_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	VT TVT = (VT)/2 * Thsync VT/2 >= (VBP+1) + (Y+1) +2
15:12	/	/	/
11:0	R/W	0x0	VBP Tvbp = (VBP +1) * Thsync

5.1.6.13 0x0054 LCD Basic Timing Register3 (Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: LCD_BASIC3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0x0	HSPW Thspw = (HSPW+1) * Tdclk HT > (HSPW+1)
15:10	/	/	/
9:0	R/W	0x0	VSPW Tvspw = (VSPW+1) * Thsync VT/2 > (VSPW+1)

5.1.6.14 0x0058 LCD HV Panel Interface Register (Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: LCD_HV_IF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	HV_MODE Set the HV mode of LCD controller 0000: 24-bit/1-cycle parallel mode 1000: 8-bit/3-cycle RGB serial mode (RGB888) 1010: 8-bit/4-cycle Dummy RGB (DRGB) 1011: 8-bit/4-cycle RGB Dummy (RGBD) 1100: 8-bit/2-cycle YUV serial mode (CCIR656)
27:26	R/W	0x0	RGB888_ODD_ORDER Serial RGB888 mode Output sequence at odd lines of the panel (line 1, 3, 5, 7…). 00: R→G→B 01: B→R→G 10: G→B→R 11: R→G→B
25:24	R/W	0x0	RGB888_EVEN_ORDER Serial RGB888 mode Output sequence at even lines of the panel (line 2, 4, 6, 8…). 00: R→G→B 01: B→R→G 10: G→B→R 11: R→G→B

Offset: 0x0058			Register Name: LCD_HV_IF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
23:22	R/W	0x0	YUV_SM Serial YUV mode Output sequence 2-pixel-pair of every scan line. 00: YUYV 01: YVYU 10: UYVY 11: VYUY
21:20	R/W	0x0	YUV_EAV_SAV_F_LINE_DLY Set the delay line mode. 00: F toggle right after active video line 01: delay 2 line (CCIR PAL) 10: delay 3 line (CCIR NTSC) 11: reserved
19	R/W	0x0	CCIR_CSC_DIS LCD convert source from RGB to YUV. 0: Enable 1: Disable Only valid when HV mode is “1100”.
18:0	/	/	/

5.1.6.15 0x0060 LCD CPU Panel Interface Register (Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: LCD_CPU_IF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	CPU_MODE Set the cpu interface work mode 0000: 18-bit/256K mode 0010: 16-bit mode0 0100: 16-bit mode1 0110: 16-bit mode2 1000: 16-bit mode3 1010: 9-bit mode 1100: 8-bit 256K mode 1110: 8-bit 65K mode xxx1: 24-bit for DSI
27	/	/	/
26	R/W	0x0	DA Pin A1 value in 8080 mode auto/flash states
25	R/W	0x0	CA Pin A1 value in 8080 mode WR/RD execute

Offset: 0x0060			Register Name: LCD_CPU_IF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
24	/	/	/
23	R	0x0	WR_FLAG The status of write operation. 0: Write operation is finishing 1: Write operation is pending
22	R	0x0	RD_FLAG The status of read operation. 0: Read operation is finishing 1: Read operation is pending
21:18	/	/	/
17	R/W	0x0	AUTO Auto transfer mode If it is 1, all the valid data during this frame are written to panel. **Note: This bit is sampled by Vsync.**
16	R/W	0x0	FLUSH Direct transfer mode If it is enabled, FIFO1 is regardless of the HV timing, the pixels data keep being transferred unless the input FIFO was empty. Data output rate is controlled by DCLK.
15:4	/	/	/
3	R/W	0x0	TRI_FIFO_BIST_EN Entry address is 0xFF8 0: Disable 1: Enable
2	R/W	0x0	TRI_FIFO_EN Enable the trigger FIFO 0: Disable 1: Enable
1	R/W1S	0x0	TRI_START Software must make sure that write ‘1’ only when this flag is ‘0’. Writing ‘1’ starts a frame flush and writing ’0’ has no effect. This flag indicates the frame flush is running.
0	R/W	0x0	TRI_EN Enable trigger mode 0: Trigger mode disable 1: Trigger mode enable

5.1.6.16 0x0064 LCD CPU Panel Write Data Register (Default Value: 0x0000_0000)

Offset: 0x0064			Register Name: LCD_CPU_WR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	W	0x0	DATA_WR Data write on 8080 bus, launch a write operation on 8080 bus.

5.1.6.17 0x0068 LCD CPU Panel Read Data Register0 (Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: LCD_CPU_RD0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R	0x0	DATA_RD0 Data read on 8080 bus, launch a new read operation on 8080 bus.

5.1.6.18 0x006C LCD CPU Panel Read Data Register1 (Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: LCD_CPU_RD1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R	0x0	DATA_RD1 Data read on 8080 bus, without a new read operation on 8080 bus.

5.1.6.19 0x0084 LCD LVDS Interface Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: LCD_LVDS_IF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0	LCD_LVDS_EN Enable LVDS interface 0: Disable 1: Enable

Offset: 0x0084			Register Name: LCD_LVDS_IF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
30	R/W	0	LCD_LVDS_LINK Select work in single link mode or dual link mode 0: Single link 1: Dual link
29	R/W	0	LCD_LVDS_EVEN_ODD_DIR Set the order of even field and odd field 0: normal 1: reverse
28	R/W	0	LCD_LVDS_DIR Set the LVDS direction 0: Normal 1: Reverse
27	R/W	0	LCD_LVDS_MODE Set the LVDS data mode 0: NS mode 1: JEIDA mode
26	R/W	0	LCD_LVDS_BITWIDTH Set the bit width of data 0: 24-bit 1: 18-bit
25	R/W	0	LCD_LVDS_DEBUG_EN Enable LVDS debug function 0: Disable 1: Enable
24	R/W	0	LCD_LVDS_DEBUG_MODE Set the output signal in debug mode 0: Mode0—Random data 1: Mode1—Output CLK period=7/2 LVDS CLK period
23	R/W	0	LCD_LVDS_CORRECT_MODE Set the LVDS correct mode 0: Mode0 1: Mode1
22:21	/	/	/
20	R/W	0	LCD_LVDS_CLK_SEL Select the clock source of LVDS 0: Reserved 1: LCD CLK
19:5	/	/	/
4	R/W	0	LCD_LVDS_CLK_POL Set the clock polarity of LVDS 0: Reverse 1: Normal

Offset: 0x0084			Register Name: LCD_LVDS_IF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
3:0	R/W	0	LCD_LVDS_DATA_POL Set the data polarity of LVDS 0: Reverse 1: Normal

5.1.6.20 0x0088 LCD IO Polarity Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: LCD_IO_POL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	IO_OUTPUT_SEL When it is set as '1', the d[23:0], io0, io1, io3 are sync to dclk. 0: Normal output 1: Register output
30:28	R/W	0x0	DCLK_SEL Set the phase offset of clock and data in hv mode. 000: Used DCLK0 (normal phase offset) 001: Used DCLK1 (1/3 phase offset) 010: Used DCLK2 (2/3 phase offset) 100: DCLK0/2 phase 0 101: DCLK0/2 phase 90 Others: Reserved
27	R/W	0x0	IO3_INV Enable invert function of IO3 0: Not invert 1: Invert
26	R/W	0x0	IO2_INV Enable invert function of IO2 0: Not invert 1: Invert
25	R/W	0x0	IO1_INV Enable invert function of IO1 0: Not invert 1: Invert
24	R/W	0x0	IO0_INV Enable invert function of IO0 0: Not invert 1: Invert

Offset: 0x0088			Register Name: LCD_IO_POL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
23:0	R/W	0x0	Data_INV LCD output port D[23:0] polarity control, with independent bit control. 0: Normal polarity 1: Invert the specify output

5.1.6.21 0x008C LCD IO Control Register (Default Value: 0x0FFF_FFFF)

Offset: 0x008C			Register Name: LCD_IO_TRI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x0	RGB_ENDIAN Set the endian of data bits 0: Normal 1: Bits_invert
27	R/W	0x1	IO3_OUTPUT_TRI_EN Enable the output of IO3 1: Disable 0: Enable
26	R/W	0x1	IO2_OUTPUT_TRI_EN Enable the output of IO2 1: Disable 0: Enable
25	R/W	0x1	IO1_OUTPUR_TRI_EN Enable the output of IO1 1: Disable 0: Enable
24	R/W	0x1	IO0_OUTPUT_TRI_EN Enable the output of IO0 1: Disable 0: Enable
23:0	R/W	0xFFFFFF	DATA_OUTPUT_TRI_EN LCD output port D[23:0] output enable, with independent bit control. 1: Disable 0: Enable

5.1.6.22 0x00FC LCD Debug Register (Default Value: 0x0000_0000)

Offset: 0x00FC			Register Name: LCD_DEBUG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	LCD_FIFO_UNDERFLOW The flag shows whether the fifos in underflow status 0: Not underflow 1: Underflow
30	/	/	/
29	R	0x0	LCD_FIELD_POL The flag indicates the current field polarity 0: Second field 1: First field
28	/	/	/
27:16	R	0x0	LCD_CURRENT_LINE The current scan line
15:0	/	/	/

5.1.6.23 0x0100 LCD CEU Control Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: LCD_CEU_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CEU_EN Enable CEU function 0: Bypass 1: Enable
30	R/W	0x0	BT656_F_MASK BT656 F Mask 0: Disable 1: Enable
29	R/W	0x0	BT656_F_MASK_VALUE BT656 F Mask Value
28:0	/	/	/

5.1.6.24 0x0110+N*0x04 (N=0–10) LCD CEU Coefficient Register0 (Default Value: 0x0000_0000)

Offset: 0x0110+N*0x04 (N=0–10)			Register Name: LCD_CEU_COEF_MUL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/

Offset: 0x0110+N*0x04 (N=0–10)			Register Name: LCD_CEU_COEF_MUL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
12:0	R/W	0x0	CEU_COEF_MUL_VALUE Signed 13-bit value, range of (-16,16). N=0: Rr N=1: Rg N=2: Rb N=4: Gr N=5: Gg N=6: Gb N=8: Br N=9: Bg N=10: Bb

5.1.6.25 0x011C+N*0x10 (N=0–2) LCD CEU Coefficient Register1 (Default Value: 0x0000_0000)

Offset: 0x011C+N*0x10 (N=0–2)			Register Name: LCD_CEU_COEF_ADD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18:0	R/W	0x0	CEU_COEF_ADD_VALUE Signed 19-bit value, range of (-16384, 16384). N=0: Rc N=1: Gc N=2: Bc

5.1.6.26 0x0140+N*0x04 (N=0–2) LCD CEU Coefficient Register2 (Default Value: 0x0000_0000)

Offset: 0x0140+N*0x04 (N=0–2)			Register Name: LCD_CEU_COEF_RANG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	CEU_COEF_RANGE_MIN Unsigned 8-bit value, range of [0, 255].
15:8	/	/	/
7:0	R/W	0x0	CEU_COEF_RANGE_MAX Unsigned 8-bit value, range of [0, 255].

5.1.6.27 0x0160 LCD CPU Panel Trigger Register0 (Default Value: 0x0000_0000)

Offset: 0x0160			Register Name: LCD_CPU_TRI0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	BLOCK_SPACE The spaces between data blocks. It should be set >20*pixel.
15:12	/	/	/
11:0	R/W	0x0	BLOCK_SIZE The size of data block. It is usually set as X.

5.1.6.28 0x0164 LCD CPU Panel Trigger Register1 (Default Value: 0x0000_0000)

Offset: 0x0164			Register Name: LCD_CPU_TRI1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R	0x0	BLOCK_CURRENT_NUM Shows the current data block transmitting to panel.
15:0	R/W	0x0	BLOCK_NUM The number of data blocks. It is usually set as Y.

5.1.6.29 0x0168 LCD CPU Panel Trigger Register2 (Default Value: 0x0020_0000)

Offset: 0x0168			Register Name: LCD_CPU_TRI2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x20	START_DLY T_{dly} = (Start_Delay +1) * be_clk*8.
15	R/W	0x0	TRANS_START_MODE Select the FIFOs used in CPU mode. 0: ECC_FIFO+TRI_FIFO 1: TRI_FIFO
14:13	R/W	0x0	SYNC_MODE Set the sync mode in CPU interface. 0x: Auto 10: 0 11: 1
12:0	R/W	0x0	TRANS_START_SET Usual set as the length of a line.

5.1.6.30 0x016C LCD CPU Panel Trigger Register3 (Default Value: 0x0000_0000)

Offset: 0x016C			Register Name: LCD_CPU_TRI3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:28	R/W	0x0	TRI_INT_MODE When set as 01, the Tri_Counter_Int occurs in cycle of (Count_N+1)×(Count_M+1)×4 dclk. When set as 10 or 11, the io0 is map as TE input. 00: Disable 01: Counter mode 10: Te rising mode 11: Te falling mode
27:24	/	/	/
23:8	R/W	0x0	COUNTER_N The value of counter factor
7:0	R/W	0x0	COUNTER_M The value of counter factor

5.1.6.31 0x0170 LCD CPU Panel Trigger Register4 (Default Value: 0x0000_0000)

Offset: 0x0170			Register Name: LCD_CPU_TRI4_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x0	PLUG_MODE_EN Enable the plug mode used in dsi command mode. 0: Disable 1: Enable
27:25	/	/	/
24	R/W	0x0	A1_First_Valid Valid in first Block.
23:0	R/W	0x0	D23_TO_D0_First_Valid Valid in first Block.

5.1.6.32 0x0174 LCD CPU Panel Trigger Register5 (Default Value: 0x0000_0000)

Offset: 0x0174			Register Name: LCD_CPU_TRI5_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/

Offset: 0x0174			Register Name: LCD_CPU_TRI5_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
24	R/W	0x0	A1_NON_First_Valid Valid in Block except first.
23:0	R/W	0x0	D23_TO_D0_NON_First_Valid Valid in Block except first.

5.1.6.33 0x0180 LCD Color Map Control Register (Default Value: 0x0000_0000)

Offset: 0x0180			Register Name: LCD_CMAP_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	COLOR_MAP_EN Enable the color map function. This module only works when X is divided by 4. 0: Bypass 1: Enable
30:1	/	/	/
0	R/W	0x0	OUT_FORMAT Set the pixel output format in color map function. 0: 4 pixel output mode: Out0 -> Out1 -> Out2 -> Out3 1: 2 pixel output mode: Out0 -> Out1

5.1.6.34 0x0190 LCD Color Map Odd Line Register0 (Default Value: 0x0000_0000)

Offset: 0x0190			Register Name: LCD_CMAP_ODD0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	OUT_ODD1 Indicates the output order of components. bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved

Offset: 0x0190			Register Name: LCD_CMAP_ODD0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0x0	OUT_ODD0 Indicates the output order of components. bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved

5.1.6.35 0x0194 LCD Color Map Odd Line Register1 (Default Value: 0x0000_0000)

Offset: 0x0194			Register Name: LCD_CMAP_ODD1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	OUT_ODD3 Indicates the output order of components. bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved

Offset: 0x0194			Register Name: LCD_CMAP_ODD1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0x0	OUT_ODD2 Indicates the output order of components. bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved

5.1.6.36 0x0198 LCD Color Map Even Line Register0 (Default Value: 0x0000_0000)

Offset: 0x0198			Register Name: LCD_CMAP_EVEN0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	OUT_EVEN1 Indicates the output order of components. bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved

Offset: 0x0198			Register Name: LCD_CMAP_EVEN0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0x0	OUT_EVEN0 Indicates the output order of components. bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved

5.1.6.37 0x019C LCD Color Map Even Line Register1 (Default Value: 0x0000_0000)

Offset: 0x019C			Register Name: LCD_CMAP_EVEN1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	OUT_EVEN3 Indicates the output order of components. bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved

Offset: 0x019C			Register Name: LCD_CMAP_EVEN1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0x0	OUT_EVEN2 Indicates the output order of components. bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111: Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved

5.1.6.38 0x01F0 LCD Safe Period Register (Default Value: 0x0000_0000)

Offset: 0x01F0			Register Name: LCD_SAFE_PERIOD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	SAFE_PERIOD_FIFO_NUM When the data length in line buffer is more than SAFE_PERIOD_FIFO_NUM, the LCD controller will allow dram controller to stop working to change frequency.
15:4	R/W	0x0	SAFE_PERIOD_LINE Set a fixed line and during the line time, the LCD controller allow dram controller to change frequency. The fixed line should be set in the blanking area.
3	/	/	/

Offset: 0x01F0			Register Name: LCD_SAFE_PERIOD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
2:0	R/W	0x0	SAFE_PERIOD_MODE Select the save mode 000: unsafe 001: safe 010: safe at FIFO_CURR_NUM > SAFE_PERIOD_FIFO_NUM 011: safe at 2 and safe at sync active 100: safe at line

5.1.6.39 0x0220 LCD LVDS Analog Register0 (Default Value: 0x0000_0000)

Offset: 0x0220			Register Name: LCD_LVDS_ANA0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	LVDS_EN_MB Enable the bias circuit of the LVDS_Ana module. 0: Disable 1: Enable
30	R/W	0x0	Reserved
29	R/W	0x0	EN_LVDS Enable LVDS
28	R/W	0x0	EN_24M Enable the 24M clock
27:25	/	/	/
24	R/W	0x0	LVDS_HPREN_DRVC Enable clock channel drive 0: Disable 1: Enable
23:20	R/W	0x0	LVDS_HPREN_DRV Enable data channel[3:0] drive 0: Disable 1: Enable

Offset: 0x0220			Register Name: LCD_LVDS_ANA0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
19:17	R/W	0x0	LVDS_REG_C Adjust current flowing through Rload of Rx to change the differential signals amplitude. 000: 216 mV 001: 252 mV 010: 276 mV 011: 312 mV 100: 336 mV 101: 372 mV 110: 395 mV 111: 432 mV
16	R/W	0x0	LVDS_REG_DENC Choose data output or PLL test clock output in LVDS_tx.
15:12	R/W	0x0	LVDS_REG_DEN Choose data output or PLL test clock output in LVDS_tx.
11	/	/	/
10:8	R/W	0x0	LVDS_REG_R Adjust current flowing through R_{load} of R_x to change the common signals amplitude. 000: 0.925 V 001: 0.950 V 010: 0.975 V 011: 1.000 V 100: 1.025 V 101: 1.050 V 110: 1.075 V 111: 1.100 V
7:5	/	/	/
4	R/W	0x0	LVDS_REG_PLRC LVDS clock channel direction. 0: Normal 1: Reverse
3:0	R/W	0x0	LVDS_REG_PLR LVDS data channel [3:0] direction. 0: Normal 1: Reverse

5.1.6.40 0x0228 LCD FSYNC Generate Control Register (Default Value: 0x0000_0000)

Offset: 0x0228			Register Name: FSYNC_GEN_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18:8	R/W	0x0	SENSOR_DIS_TIME Delay 0–2047 Hsync Period When hsync_pol_sel is 0, the actual delay is sensor_dis_time-1. When hsync_pol_sel is 1, the actual delay is sensor_dis_time.
7	/	/	/
6	R/W	0x0	SENSOR_ACT1_VALUE Sensor Active1 Value 0: Fsync active_1 period output 0 1: Fsync active_1 period output 1
5	R/W	0x0	SENSOR_ACT0_VALUE Sensor Active0 Value 0: Fsync active_0 period output 0 1: Fsync active_0 period output 1
4	R/W	0x0	SENSOR_DIS_VALUE Sensor Disable Value 0: Fsync disable period output 0 1: Fsync disable period output 1
3	/	/	/
2	R/W	0x0	HSYNC_POL_SEL Hsync Polarity Select 0: Normal 1: Opposite hsync to hysnc counter
1	R/W	0x0	SEL_VSYNC_EN Select Vsync Enable 0: Select vsync falling edge to start state machine 1: Select vsync rising edge to start state machine
0	R/W	0x0	FSYNC_GEN_EN Fsync Generate Enable 0: Disable 1: Enable

5.1.6.41 0x022C LCD FSYNC Generate Delay Register (Default Value: 0x0000_0000)

Offset: 0x022C			Register Name: FSYNC_GEN_DLY_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/

Offset: 0x022C			Register Name: FSYNC_GEN_DLY_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
27:16	R/W	0x0	SENSOR_ACT0_TIME Delay 0–4095 Pixel clk Period The actual delay is sensor_act0_time+1.
15:12	/	/	/
11:0	R/W	0x0	SENSOR_ACT1_TIME Delay 0–4095 Pixel clk Period The actual delay is sensor_act1_time+1.

5.1.6.42 0x0230 LCD Sync Control Register (Default Value: 0x0000_0000)

Offset: 0x0230			Register Name: LCD_SYNC_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	LCD_CTRL_WORK_MODE LCD Controller Work mode 0: Single DSI mode 1: Dual DSI mode
7:5	/	/	/
4	R/W	0x0	LCD_CYRL_SYNC_MASTER_SLAVE LCD Controller Sync Master Slave 0: Master 1: Slave **Note: Only use in Single DSI mode.**
3:1	/	/	/
0	R/W	0x0	LCD_CTRL_SYNC_MODE LCD Controller Sync Mode 0: Sync in the first time 1: Sync every frame **Note: Only use in Single DSI mode.**

5.1.6.43 0x0234 LCD Sync Position Register (Default Value: 0x0000_0000)

Offset: 0x0234			Register Name: LCD_SYNC_POS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/

Offset: 0x0234			Register Name: LCD_SYNC_POS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
27:16	R/W	0x0	LCD_Sync_Pixel_Num Set the pixel number of master LCD controller which is used to trigger the slave LCD controller to start working.This value is the number of pixels between the trigger point and the end of the line. Tri pos = Tline*LCD_Sync_Line_Num+Tpixel*(HT-LCD_Sync_Pixel_Num) **Note: Only use in Single DSI mode.**
15:12	/	/	/
11:0	R/W	0x0	LCD_Sync_Line_Num Set the line number of master LCD controller which is used to trigger the slave LCD controller to start working. Note:It is only set in master LCD controller.It is not necessarily to set in slave LCD controller. Tri pos = Tline*LCD_Sync_Line_Num+Tpixel*(HT-LCD_Sync_Pixel_Num) **Note: Only use in Single DSI mode.**

5.1.6.44 0x0238 LCD Slave Stop Position Register (Default Value: 0x0000_0000)

Offset: 0x0238			Register Name: LCD_SLAVE_STOP_POS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	STOP_VAL Set the stop position of the slave LCD. This value is the number of pixels between the stop position and the end of the HFP. Stop_pos = HFP - Stop_val. 0<Stop_pos<HFP-2 **Note: Only use in Single DSI mode.**

5.1.6.45 0x0400-0x07FF LCD Gamma Table Registers (Default Value: 0x0000_0000)

Offset: 0x0400–0x07FF			Register Name: LCD_GAMMA_TABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	RED_COMP Red Component

Offset: 0x0400–0x07FF			Register Name: LCD_GAMMA_TABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
15:8	R/W	0x0	GREEN_COMP Green Component
7:0	R/W	0x0	BLUE_COMP Blue Component

5.2 TCON TV

5.2.1 Overview

The Timing Controller_TV (TCON_TV) is a module that processes video signals received from systems using a complicated arithmetic and then generates control signals and transmits them to the TV panel driver IC.

The TCON_TV includes the following features:

- Supports 10-bit pixel depth YUV444, and HV format output up to 4K@60Hz
- Supports 8-bit pixel depth YUV444, and HV format output up to 4K@60Hz

5.2.2 Functional Description

5.2.2.1 CEU Module

Function: This module enhance color data from DE .

R' = Rr*R + Rg*G + Rb*B

G' = Gr*R + Gg*G + Gb*B

B' = Br*R + Bg*G + Bb*B

Rr, Rg, Rb, ,Gr, Gg, Gb, Br, Bg, Bb bool 0,1

R, G, B u10 [0-1023]

R' have the range of [Rmin ,Rmax]

G' have the range of [Rmin ,Rmax]

B' have the range of [Rmin ,Rmax]

5.2.3 Register List

Module Name	Base Address
TCON_TV0	0x05470000

Register Name	Offset	Description
TV_GCTL_REG	0x0000	TV Global Control Register
TV_GINT0_REG	0x0004	TV Global Interrupt Register0
TV_GINT1_REG	0x0008	TV Global Interrupt Register1
TV_SRC_CTL_REG	0x0040	TV Source Control Register

Register Name	Offset	Description
TV_CTL_REG	0x0090	TV Control Register
TV_BASIC0_REG	0x0094	TV Basic Timing Register0
TV_BASIC1_REG	0x0098	TV Basic Timing Register1
TV_BASIC2_REG	0x009C	TV Basic Timing Register2
TV_BASIC3_REG	0x00A0	TV Basic Timing Register3
TV_BASIC4_REG	0x00A4	TV Basic Timing Register4
TV_BASIC5_REG	0x00A8	TV Basic Timing Register5
TV_IO_POL_REG	0x0088	TV SYNC Signal Polarity Register
TV_IO_TRI_REG	0x008C	TV SYNC Signal IO Control Register
TV_DEBUG_REG	0x00FC	TV Debug Register
TV_CEU_CTL_REG	0x0100	TV CEU Control Register
TV_CEU_COEF_MUL_REG	0x0110+N*0x04(N=0–10)	TV CEU Coefficient Register0
TV_CEU_COEF_RANG_REG	0x0140+N*0x04(N=0–2)	TV CEU Coefficient Register2
TV_SAFE_PERIOD_REG	0x01F0	TV Safe Period Register
TV_FILL_CTL_REG	0x0300	TV Fill Data Control Register
TV_FILL_BEGIN_REG	0x0304+N*0x0C(N=0–2)	TV Fill Data Begin Register
TV_FILL_END_REG	0x0308+N*0x0C(N=0–2)	TV Fill Data End Register
TV_FILL_DATA_REG	0x030C+N*0x0C(N=0–2)	TV Fill Data Value Register
TV_DATA_IO_POL0_REG	0x0330	TCON Data IO Polarity Control0
TV_DATA_IO_POL1_REG	0x0334	TCON Data IO Polarity Control1
TV_DATA_IO_TRI0_REG	0x0338	TCON Data IO Enable Control0
TV_DATA_IO_TRI1_REG	0x033C	TCON Data IO Enable Control1
TV_PIXELDEPTH_MODE_REG	0x0340	TV Pixeldepth Mode Control Register

5.2.4 Register Description

5.2.4.1 0x0000 TV Global Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: TV_GCTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TV_EN When it is disabled, the module will be reset to idle state. 0: Disable 1: Enable
30:2	/	/	/
1	R/W	0x0	CEC_DDC_PAD_SEL CEC DDC PAD Select 1: TCON_TV internal pad for cec scl sal 0: GPIO pad for cec scl sal
0	/	/	/

5.2.4.2 0x0004 TV Global Interrupt Register0 (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: TV_GINT0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x0	TV_VB_INT_EN TV Vb Interrupt Enable 0: Disable 1: Enable
29	/	/	/
28	R/W	0x0	TV_Line_Int_En TV Line Interrupt Enable 0: Disable 1: Enable
27:15	/	/	/
14	R/W	0x0	TV_VB_INT_FLAG TV Vb Interrupt Flag Asserted during vertical no-display period every frame. Write 0 to clear it.
13	/	/	/
12	R/W	0x0	TV_Line_Int_Flag TV Line Interrupt Flag Trigger when SY1 match the current TV scan line Write 0 to clear it.
11:0	/	/	/

5.2.4.3 0x0008 TV Global Interrupt Register1 (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: TV_GINT1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R/W	0	TV_Line_Int_Num Scan line for TV line trigger(including inactive lines) Setting it for the specified line for trigger 1. Note: SY1 is writable only when LINE_TRG1 is disabled.

5.2.4.4 0x0040 TV Source Control Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: TV_SRC_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0	TV_SRC_SEL TV Source Select 000: DE 001: Color Check 010: Grayscale Check 011: Black by White Check 100: Reserved 101: Reserved 111: Gridding Check

5.2.4.5 0x0090 TV Control Register (Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: TV_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TV_EN When enable TCON_TV, this bit and the 0x0000[bit31] need to be enabled. 0: Disable 1: Enable
30:9	/	/	/
8:4	R/W	0x0	START_DELAY This is for DE0 and DE1.
3:2	/	/	/
1	R/W	0x0	TV_SRC_SEL TV Source Select 0: Reserved 1: BLUE data **Note: The priority of this bit is higher than TV_SRC_SEL(bit[2:0]) in TV_SRC_CTL_REG.**
0	/	/	/

5.2.4.6 0x0094 TV Basic Timing Register0 (Default Value: 0x0000_0000)

Offset: 0x0094			Register Name: TV_BASIC0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	WIDTH_XI Source Width Is X+1
15:12	/	/	/
11:0	R/W	0x0	HEIGHT_YI Source Height Is Y+1

5.2.4.7 0x0098 TV Basic Timing Register1 (Default Value: 0x0000_0000)

Offset: 0x0098			Register Name: TV_BASIC1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	LS_XO Width Is LS_XO+1
15:12	/	/	/
11:0	R/W	0x0	LS_YO Width Is LS_YO+1 **Note: This version LS_YO = TV_YI**

5.2.4.8 0x009C TV Basic Timing Register2 (Default Value: 0x0000_0000)

Offset: 0x009C			Register Name: TV_BASIC2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	TV_XO Width is TV_XO+1
15:12	/	/	/
11:0	R/W	0x0	TV_YO Height is TV_YO+1

5.2.4.9 0x00A0 TV Basic Timing Register3 (Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name: TV_BASIC3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	H_T Horizontal total time Thcycle = (HT+1) * Thdclk
15:12	/	/	/
11:0	R/W	0x0	H_BP Horizontal back porch Thbp = (HBP +1) * Thdclk

5.2.4.10 0x00A4 TV Basic Timing Register4 (Default Value: 0x0000_0000)

Offset: 0x00A4			Register Name: TV_BASIC4_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	V_T horizontal total time (in HD line) Tvt = VT/2 * Th
15:12	/	/	/
11:0	R/W	0x0	V_BP horizontal back porch (in HD line) Tvbp = (VBP +1) * Th

5.2.4.11 0x00A8 TV Basic Timing Register5 (Default Value: 0x0000_0000)

Offset: 0x00A8			Register Name: TV_BASIC5_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0x0	H_SPW Horizontal Sync Pulse Width (in dclk) Thspw = (HSPW+1) * Tdclk **Note: HT> (HSPW+1)**
15:10	/	/	/

Offset: 0x00A8			Register Name: TV_BASIC5_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
9:0	R/W	0x0	V_SPW Vertical Sync Pulse Width (in lines) Tvspw = (VSPW+1) * Th **Note: VT/2 > (VSPW+1)**

5.2.4.12 0x0088 TV SYNC Signal Polarity Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: TV_IO_POL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27	R/W	0x0	IO3_INV IO3 Invert 0: Not invert 1: Invert
26	R/W	0x0	IO2_INV IO2 Invert 0: Not invert 1: Invert
25	R/W	0x0	IO1_INV IO1 Invert 0: Not invert 1: Invert
24	R/W	0x0	IO0_INV IO0 Invert 0: Not invert 1: Invert
23:0	/	/	/

5.2.4.13 0x008C TV SYNC Signal IO Control Register (Default Value: 0x0F00_0000)

Offset: 0x008C			Register Name: TV_IO_TRI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27	R/W	0x1	IO3_OUTPUT_TRI_EN IO3 Output Trigger Enable 1: Disable 0: Enable

Offset: 0x008C			Register Name: TV_IO_TRI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
26	R/W	0x1	IO2_OUTPUT_TRI_EN IO2 Output Trigger Enable 1: Disable 0: Enable
25	R/W	0x1	IO1_OUTPUT_TRI_EN IO1 Output Trigger Enable 1: Disable 0: Enable
24	R/W	0x1	IO0_OUTPUT_TRI_EN IO0 Output Trigger Enable 1: Disable 0: Enable
23:0	/	/	/

5.2.4.14 0x00FC TV Debug Register (Default Value: 0x0000_0000)

Offset: 0x00FC			Register Name: TV_DEBUG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x0	TV_FIFO_U TV FIFO Underflow
29	/	/	/
28	R	0x0	TV_FIELD_POL TV Field Polarity 0: Second field 1: First field
27:12	/	/	/
13	R/W	0x0	LINE_BUF_BYPASS Line Buffer Bypass 0: Used 1: Bypass
12	/	/	/
11:0	R	0x0	TV_CURRENT_LINE TV Current Line

5.2.4.15 0x0100 TV CEU Control Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: TV_CEU_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CEU_EN CEU Enable 0: Bypass 1: Enable
30:0	/	/	/

5.2.4.16 0x0110+N*0x04 (N=0–10) TV CEU Coefficient Register0 (Default Value: 0x0000_0000)

Offset: 0x110+N*0x04 (N=0–10)			Register Name: TV_CEU_COEF_MUL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	CEU_COEF_MUL_VALUE Note: 1. CEU_Coef_Mul_Value only can be 0 or 1. 2. REG Map: N=0: Rr N=1: Rg N=2: Rb N=4: Gr N=5: Gg N=6: Gb N=8: Br N=9: Bg N=10: Bb
7:0	/	/	/

5.2.4.17 0x0140+N*0x04 (N=0–2) TV CEU Coefficient Register2 (Default Value: 0x0000_0000)

Offset: 0x0140+N*0x04 (N=0–2)			Register Name: TV_CEU_COEF_RANG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0	CEU_COEF_RANGE_MIN Unsigned 10-bit Value, range of [0, 1023]
15:10	/	/	/
9:0	R/W	0	CEU_COEF_RANGE_MAX Unsigned 10-bit Value, range of [0, 1023]

5.2.4.18 0x01F0 TV Safe Period Register (Default Value: 0x0000_0000)

Offset: 0x01F0			Register Name: TV_SAFE_PERIOD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	SAFE_PERIOD_FIFO_NUM Safe Period FIFO Number
15:4	R/W	0x0	Safe_Period_Line Safe Period Line
3	/	/	/
2:0	R/W	0x0	Safe_Period_Mode Safe Period Mode 000: unsafe 001: safe 010: safe at line_buf_curr_num > safe_period_fifo_num 011: safe at 2 and safe at sync active 100: safe at line

5.2.4.19 0x0300 TV Fill Data Control Register (Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: TV_FILL_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TV_Fill_En TV Fill Enable 0: Bypass 1: Enable
30:0	/	/	/

5.2.4.20 0x0304+N*0x0C (N=0–2) TV Fill Data Begin Register (Default Value: 0x0000_0000)

Offset: 0x0304+N*0x0C (N=0–2)			Register Name: TV_FILL_BEGIN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0	FILL_BEGIN Fill Begin

5.2.4.21 0x0308+N*0x0C (N=0–2) TV Fill Data End Register (Default Value: 0x0000_0000)

Offset: 0x0308+N*0x0C (N=0–2)			Register Name: TV_FILL_END_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	FILL_END Fill End

5.2.4.22 0x030C+N*0x0C (N=0–2) TV Fill Data Value Register (Default Value: 0x0000_0000)

Offset: 0x030C+N*0x0C (N=0–2)			Register Name: TV_FILL_DATA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:0	R/W	0x0	FILL_VALUE Fill Value

5.2.4.23 0x0330 TCON Data IO Polarity Control0 (Default Value: 0x0000_0000)

Offset: 0x0330			Register Name: TV_DATA_IO_POL0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0x0	R_CB_CH_DATA_INV R CB Channel Data Inv 0: normal polarity 1: invert the specify output
15:10	/	/	/
9:0	R/W	0x0	G_Y_CH_DATA_INV G Y Channel Data Inv 0: normal polarity 1: invert the specify output

5.2.4.24 0x0334 TCON Data IO Polarity Control1 (Default Value: 0x0000_0000)

Offset: 0x0334			Register Name: TV_DATA_IO_POL1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/

Offset: 0x0334			Register Name: TV_DATA_IO_POL1_REG
Bit	Read/Write	Default/Hex	Description
25:16	R/W	0x0	B_CR_CH_DATA_INV B CR CHANNE DATA INV 0: Normal polarity 1: Invert the specify output
15:0	/	/	/

5.2.4.25 0x0338 TCON Data IO Enable Control0 (Default Value: 0x03FF_03FF)

Offset: 0x0338			Register Name: TV_DATA_IO_TRI0_REG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:16	R/W	0x3ff	R_CB_CH_DATA_OUT_TRI_EN R CB Channel Data Output Trigger Enable 1: Disable 0: Enable
15:10	/	/	/
9:0	R/W	0x3ff	G_Y_CH_DATA_OUT_TRI_EN G Y Channel Data Output Trigger Enable 1: Disable 0: Enable

5.2.4.26 0x033C TCON Data IO Enable Control1 (Default Value: 0x03FF_0000)

Offset: 0x033C			Register Name: TV_DATA_IO_TRI1_REG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:16	R/W	0x3ff	B_CR_CH_DATA_OUT_TRI_EN B CR Channel Data Output Trigger Enable 1: Disable 0: Enable
15:0	/	/	/

5.2.4.27 0x0340 TV Pixeldepth Mode Control Register (Default Value: 0x0000_0000)

Offset: 0x0340			Register Name: TV_PIXELDEPTH_MODE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	COLORBAR_PD_MODE Colorbar Pixeldepth mode 0: 8-bit mode When data source is the embedded colorbar, the 8-bit colorbar pattern is transmitted. 1: 10-bit mode When data source is the embedded colorbar, the 10-bit colorbar pattern is transmitted.

5.3 TV Encoder

5.3.1 Overview

The TV Encoder (TVE) module is a highly programmable digital video encoder supporting worldwide video standards Composite Video Broadcast Signal (CVBS).

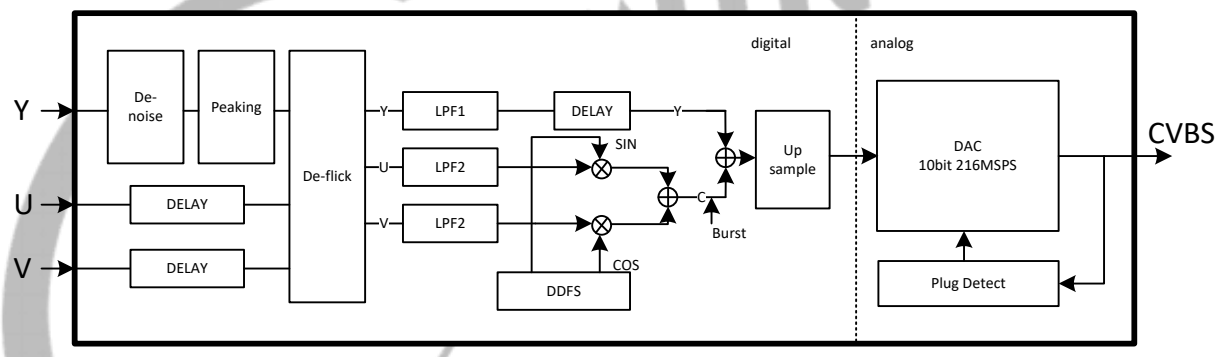
The TVE includes the following features:

- 1-channel CVBS output, supporting PAL-D and NTSC-M
- Plug status auto detecting
- 10 bits DAC output

5.3.2 Block Diagram

Figure 5-14 shows a block diagram of the TVE.

Figure 5-14 TVE Block Diagram



5.3.3 Functional Description

5.3.3.1 External Signals

Table 5-11 describes the external signals of TVE.

Table 5-11 TVE External Signals

Port Name	Description	Type
TVOUT0	TV CVBS output	AO
VCC-TVOUT	TV DAC power	P

5.3.3.2 Clock Sources

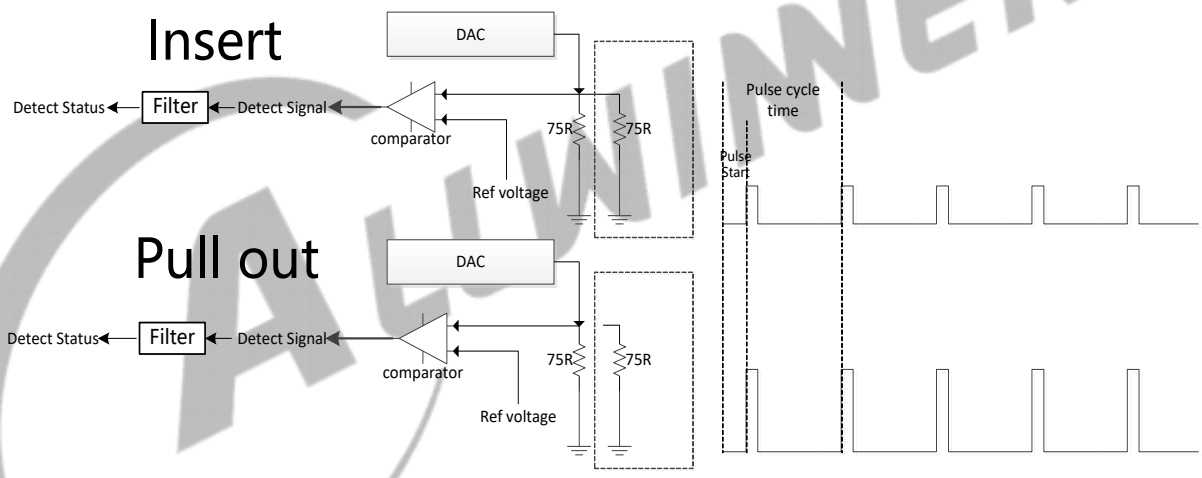
The TVE module requires one clock with 50% duty. Digital circuit and Analog circuit work by this clock. Mode and Clock frequency is shown below.

Table 5-12 TVE Clock Sources

Mode	TVE Clock Frequency
NTSC	216 MHz
PAL	216 MHz

5.3.3.3 Auto Detection Function

Figure 5-15 Auto Detection Function



DAC outputs constant current, when insert, external load is 37.5Ω; when pull out, external load is 75Ω. The method that comparator judges pin level can detect plug action.

Because plug action may exist jitter, then there need be a filter to filter jitter, the debounce time of filter is set through the bit[3:0] of TV Encoder Auto Detection de-bounce Setting Register.

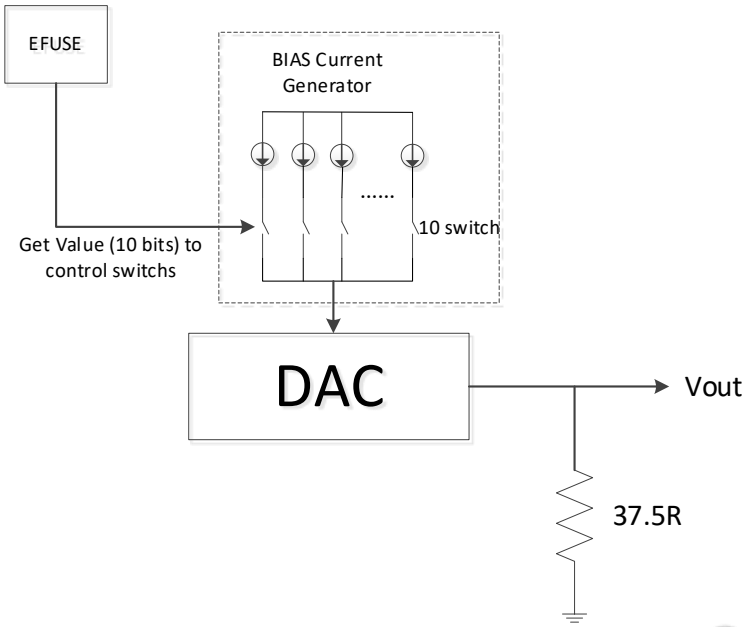
The pulse cycle time can be set through the bit[30:16] of TV Encoder Auto Detect Configuration Register1, the pulse start time can be set through the bit[14:0] of TV Encoder Auto Detect Configuration Register1. The clock sources of the two time are 32KHz clock.

Pulse width is cycle time of 4 clock sources.

Pulse amplitude can be set through the bit[9:0] of TV Encoder Auto Detect Configuration Register0.

5.3.3.4 DAC Calibration Function

Figure 5-16 DAC Calibration Function



After FT, 10-bit calibration value is burned into efuse. Every time software can read the 10-bit calibration value from efuse, to control BIAS current and BIAS current switch, then a specific BIAS current is generated to calibrate maximum output voltage of DAC.

5.3.4 Programming Guidelines

5.3.4.1 Operating TVE Module

Operate TVE module by the following steps, Figure 5-17 shows the process diagram.

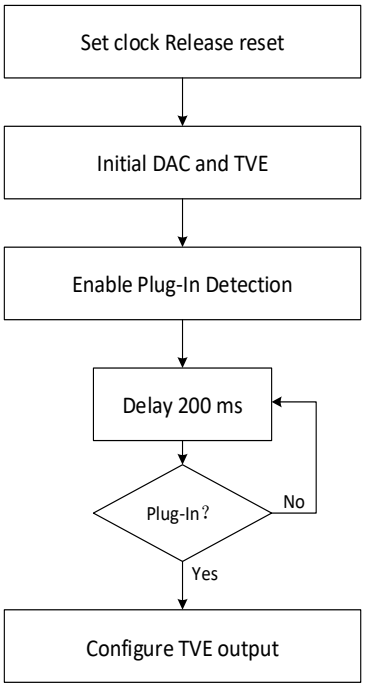
Step 1 Set CCU clock source for TVE, and release AHB bus, and module reset.

Step 2 Initial DAC amplitude value from efuse calibration value which has burned.

Step 3 Enable the plug-in detect function, and detect plug-in status every 200 ms.

Step 4 When the plug-in has detected, configure TVE module to output mode setting by application.

Figure 5-17 Operating TVE Module



5.3.5 Register List

Module Name	Base Address
TVE_TOP	0x05600000
TVE	0x05604000

Register Name	Offset	Description
TVE_TOP		
TVE_DAC_MAP	0x0020	TV Encoder DAC MAP Register
TVE_DAC_STATUS	0x0024	TV Encoder DAC STAUTS Register
TVE_DAC_CFG0	0x0028	TV Encoder DAC CFG0 Register
TVE_DAC_CFG1	0x002C	TV Encoder DAC CFG1 Register
TVE_DAC_CFG2	0x0030	TV Encoder DAC CFG2 Register
TVE_DAC_CFG3	0x0034	TV Encoder DAC CFG2 Register
TVE_DAC_TEST	0x00F0	TV Encoder DAC TEST Register
TVE		
TVE_000_REG	0x0000	TV Encoder Clock Gating Register
TVE_004_REG	0x0004	TV Encoder Configuration Register
TVE_008_REG	0x0008	TV Encoder DAC Register1

Register Name	Offset	Description
TVE_00C_REG	0x000C	TV Encoder Notch and DAC Delay Register
TVE_010_REG	0x0010	TV Encoder Chroma Frequency Register
TVE_014_REG	0x0014	TV Encoder Front/Back Porch Register
TVE_018_REG	0x0018	TV Encoder HD Mode VSYNC Register
TVE_01C_REG	0x001C	TV Encoder Line Number Register
TVE_020_REG	0x0020	TV Encoder Level Register
TVE_024_REG	0x0024	TV Encoder DAC Register2
TVE_030_REG	0x0030	TV Encoder Auto Detection Enable Register
TVE_034_REG	0x0034	TV Encoder Auto Detection Interrupt Status Register
TVE_038_REG	0x0038	TV Encoder Auto Detection Status Register
TVE_03C_REG	0x003C	TV Encoder Auto Detection De-bounce Setting Register
TVE_0F8_REG	0x00F8	TV Encoder Auto Detect Configuration Register0
TVE_0FC_REG	0x00FC	TV Encoder Auto Detect Configuration Register1
TVE_100_REG	0x0100	TV Encoder Color Burst Phase Reset Configuration Register
TVE_104_REG	0x0104	TV Encoder VSYNC Number Register
TVE_108_REG	0x0108	TV Encoder Notch Filter Frequency Register
TVE_10C_REG	0x010C	TV Encoder Cb/Cr Level/Gain Register
TVE_110_REG	0x0110	TV Encoder Tint and Color Burst Phase Register
TVE_114_REG	0x0114	TV Encoder Burst Width Register
TVE_118_REG	0x0118	TV Encoder Cb/Cr Gain Register
TVE_11C_REG	0x011C	TV Encoder Sync and VBI Level Register
TVE_120_REG	0x0120	TV Encoder White Level Register
TVE_124_REG	0x0124	TV Encoder Video Active Line Register
TVE_128_REG	0x0128	TV Encoder Video Chroma BW and CompGain Register
TVE_12C_REG	0x012C	TV Encoder Register
TVE_130_REG	0x0130	TV Encoder Re-sync Parameters Register
TVE_134_REG	0x0134	TV Encoder Slave Parameter Register
TVE_138_REG	0x0138	TV Encoder Configuration Register0
TVE_13C_REG	0x013C	TV Encoder Configuration Register1
TVE_380_REG	0x0380	TV Encoder Low Pass Control Register
TVE_384_REG	0x0384	TV Encoder Low Pass Filter Control Register

Register Name	Offset	Description
TVE_388_REG	0x0388	TV Encoder Low Pass Gain Register
TVE_38C_REG	0x038C	TV Encoder Low Pass Gain Control Register
TVE_390_REG	0x0390	TV Encoder Low Pass Shoot Control Register
TVE_394_REG	0x0394	TV Encoder Low Pass Coring Register
TVE_3A0_REG	0x03A0	TV Encoder Noise Reduction Register

5.3.6 TVE_TOP Register Description

5.3.6.1 0x0020 TV Encoder DAC MAP Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: TVE_DAC_MAP
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DAC_MAP 000: OUT0 Others: Reserved
3:2	/	/	/
1:0	R/W	0x0	DAC_SEL 00: Reserved 01: TVE0 10: Reserved 11: Reserved

5.3.6.2 0x0024 TV Encoder DAC Status Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: TVE_DAC_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R	0x0	DAC_Status 00: Unconnected 01: Connected 11: Short to ground 10: Reserved

5.3.6.3 0x0028 TV Encoder DAC Configuration0 Register (Default Value: 0x8000_4200)

Offset: 0x0028			Register Name: TVE_DAC_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	DAC_CLOCK_INVERT 0: Not invert 1: Invert
30:26	/	/	/
25:16	R/W	0x0	CALI_IN
15:12	R/W	0x4	LOW_BIAS 500 uA to 4 mA
11:10	/	/	/
9	R/W	0x1	BIAS_EXT_SEL 0: Disable 1: Enable (A_SEL_BIAS_ADDA)
8	R/W	0x0	BIAS_INT_SEL 0: Disable 1: Enable (A_SEL_BIAS_RES)
7:5	/	/	/
4	R/W	0x0	BIAS_REF_INT_EN 0: Disable 1: Enable (A_EN_RESREF)
3:1	/	/	/
0	R/W	0x0	DAC_EN 0: Disable 1: Enable

5.3.6.4 0x002C TV Encoder DAC Configuration1 Register (Default Value: 0x0000_023A)

Offset: 0x002C			Register Name: TVE_DAC_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R/W	0x1	REF_EXT_SEL 0: Disable

Offset: 0x002C			Register Name: TVE_DAC_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
			1: Enable (A_SEL_DETREF_LDO)
8	R/W	0x0	REF_INT_SEL 0: Disable 1: Enable (A_SEL_DETREF_RES)
7:6	/	/	/
5:4	R/W	0x3	REF2_SEL 00: 0.25 V 01: 0.30 V 10: 0.35 V 11: 0.40 V (a_refslct2<1:0>)
3:0	R/W	0xA	REF1_SEL 0000: 0.50 V 0001: 0.55 V 0010: 0.60 V 0011: 0.65 V 0100: 0.70 V 0101: 0.75 V 0110: 0.80 V 0111: 0.85 V 1000: 0.90 V 1001: 0.95 V 1010: 1.00 V 1011: 1.05 V 1100: 1.10 V 1101: 1.15 V 1110: 1.20 V 1111: 1.25 V (a_refslct1<3:0>) The reference voltage is used for hot plug detect function.

5.3.6.5 0x0030 TV Encoder DAC Configuration2 Register (Default Value: 0x0000_0010)

Offset: 0x0030			Register Name: TVE_DAC_CFG2
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:8	R/W	0x0	AB (I config output current for different peak voltage)
7:6	R/W	0x0	S2S1
5:0	R/W	0x10	R_SET

5.3.6.6 0x0034 TV Encoder DAC Configuration3 Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: TVE_DAC_CFG3
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:16	R/W	0x0	FORCE_DATA_SET Force DAC input data
15:1	/	/	/
0	R/W	0x0	FORCE_DATA_EN 0: DAC input data from TVE 1: DAC input data from FORCE_DATA_SET

5.3.6.7 0x00F0 TV Encoder DAC Test Register (Default Value: 0x0000_0000)

Offset: 0x00F0			Register Name: TVE_DAC_TEST
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:16	R/W	0x0	DAC_TEST_LENGTH DAC TEST DATA LENGTH
15:6	/	/	/
5:4	R/W	0x0	DAC_TEST_SEL 00: DAC0 Others: Reserved
3:1	/	/	/
0	R/W	0x0	DAC_TEST_ENABLE 0: Reserved

Offset: 0x00F0			Register Name: TVE_DAC_TEST
Bit	Read/Write	Default/Hex	Description
			1: Repeat DAC data from DAC sram

5.3.7 TVE Register Description

5.3.7.1 0x0000 TV Encoder Clock Gating Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: TVE_000_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CLOCK_GATE_DIS 0: Enable 1: Disable
30:29	/	/	/
28	R/W	0x0	BIST_EN 0: Normal mode 1: Bist mode
27:23	/	/	/
22	R/W	0x0	UPSAMPLE_FOR_YPBPR 0: 1x 1: 2x
21:20	R/W	0x0	UPSAMPLE_FOR_CVBS Out up sample 00: 27 MHz 01: 54 MHz 10: 108 MHz 11: 216 MHz
19:1	/	/	/
0	R/W	0x0	TVE_EN 0: Disable 1: Enable Video Encoder enable, default disable, write 1 to take it out of the reset state

5.3.7.2 0x0004 TV Encoder Configuration Register (Default Value: 0x0001_0000)

Offset: 0x0004			Register Name: TVE_004_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	BYPASS_TV 0: Disable 1: Enable
28:27	R/W	0x0	DAC_Src_Sel 00: TV Encoder 01: LCD controller, override all other TV encoder setting, the DAC clock can from LCD controller. 10: DAC test mode, DAC using DAC clock 11: DAC test mode, DAC using AHB clock
26	R/W	0x0	DAC_Control_Logic_Clock_Sel 0: Using 27 MHz clock or 74.25 MHz clock depend on CCU setting 1: Using 54 MHz clock or 148.5 MHz clock depend on CCU setting
25	R/W	0x0	Core_Datapath_Logic_Clock_Sel 0: Using 27 MHz clock or 74.25 MHz clock depend on CCU setting 1: Using 54 MHz clock or 148.5 MHz clock depend on CCU setting
24	R/W	0x0	Core_Control_Logic_Clock_Sel 0: Using 27 MHz clock or 74.25 MHz clock depend on CCU setting 1: Using 54 MHz clock or 148.5 MHz clock depend on CCU setting
23:21	/	/	/
20	R/W	0x0	Cb_Cr_Seq_For_422_Mode 0: Cb first 1: Cr first
19	R/W	0x0	Input_Chroma_Data_Sampling_Rate_Sel 0: 4:4:4 1: 4:2:2
18	R/W	0x0	YUV_RGB_Output_En 0: CVBS 1: Reserved

Offset: 0x0004			Register Name: TVE_004_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
17	R/W	0x0	YC_EN S-port Video enable Selection. 0: Y/C is disable 1: Reserved This bit selects whether the S-port(Y/C) video output is enabled or disabled.
16	R/W	0x1	CVBS_EN Composite video enables selection 0: Composite video is disabled, Only Y/C is enabled 1: Composite video is enabled., CVBS and Y/C are enabled This bit selects whether the composite video output (CVBS) is enabled or disabled.
15:10	/	/	/
9	R/W	0x0	Color_BAR_TYPE 0: 75/7.5/75/7.5 (NTSC), 100/0/75/0(PAL) 1: 100/7.5/100/7.5(NTSC), 100/0/100/0(PAL)
8	R/W	0x0	Color_BAR_MODE Standard Color bar input selection 0: The Video Encoder input is coming from the Display Engineer 1: The Video Encoder input is coming from an internal standard color bar generator. This bit selects whether the Video Encoder video data input is replaced by an internal standard color bar generator or not.
7:5	/	/	/
4	R/W	0x0	Mode_1080i_1250Line_Sel 0: 1125 Line mode 1: 1250 Line mode
3:0	R/W	0x0	TVMode_Select 0000: NTSC 0001: PAL 0010: Reserved 0011: Reserved 01xx: Reserved 100x: Reserved 101x: Reserved 110x: Reserved

Offset: 0x0004			Register Name: TVE_004_REG
Bit	Read/Write	Default/Hex	Description
			111x: Reserved Note: Changing this register value will cause some relative register setting to relative value.

5.3.7.3 0x0008 TV Encoder DAC Register1 (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: TVE_008_REG
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	DAC0_Src_Sel 000: Composite Others: Reserved
3:0	/	/	/

5.3.7.4 0x000C TV Encoder Notch and DAC Delay Register (Default Value: 0x0201_4924)

Offset: 0x000C			Register Name: TVE_00C_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	Chroma_Filter_Active_Valid 0: Disable 1: Enable
30	R/W	0x0	Luma_filter_lti_enable 0: Disable Luma filter lti 1: Enable Luma filter lti
27:25	R/W	0x1	Y_DELAY_BEFORE_DITHER
24	R/W	0x0	HD_Mode_CB_Filter_Bypass 0: Bypass Enable 1: Bypass Disable
23	R/W	0x0	HD_Mode_CR_Filter_Bypass 0: Bypass Enable 1: Bypass Disable
22	R/W	0x0	Chroma_Filter_1_444_En 0: Chroma Filter 1 444 Disable 1: Chroma Filter 1 444 Enable
21	R/W	0x0	Chroma_HD_Mode_Filter_En

Offset: 0x000C			Register Name: TVE_00C_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: Chroma HD Filter Disable 1: Chroma HD Filter Enable
20	R/W	0x0	Chroma_Filter_Stage_1_Bypass 0: Chroma Filter Stage 1 Enable 1: Chroma Filter Stage 1 bypass
19	R/W	0x0	Chroma_Filter_Stage_2_Bypass 0: Chroma Filter Stage 2 Enable 1: Chroma Filter Stage 2 bypass
18	R/W	0x0	Chroma_Filter_Stage_3_Bypass 0: Chroma Filter Stage 3 Enable 1: Chroma Filter Stage 3 bypass
17	R/W	0x0	Luma_Filter_Bypass 0: Luma Filter Enable 1: Luma Filter bypass
16	R/W	0x1	Notch_En 0: The luma notch filter is bypassed 1: The luma notch filter is operating Luma notch filter on/off selection Note: This bit selects if the luma notch filter is operating or bypassed.
15:12	R/W	0x4	C_DELAY_BEFORE_DITHER
11:0	R/W	0x924	Reserved

5.3.7.5 0x0010 TV Encoder Chroma Frequency Register (Default Value: 0x21F0_7C1F)

Offset: 0x0010			Register Name: TVE_010_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x21f07c1f	Chroma_Freq Specify the ratio between the color burst frequency. 32 bits unsigned fraction. The default value is h21f07c1f, which is compatible with NTSC spec. 3.5795455 MHz (X'21F07C1F'): NTSC-M, NTSC-J 4.43361875 MHz(X'2A098ACB'): PAL-B, D, G, H,I, N 3.582056 MHz (X'21F69446'): PAL-N(Argentina) 3.579611 MHz (X'21E6EFE3'): PAL-M

5.3.7.6 0x0014 TV Encoder Front/Back Porch Register (Default Value: 0x0076_0020)

Offset: 0x0014			Register Name: TVE_014_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24:16	R/W	0x76	Back_Porch Specify the width of the back porch in encoder clock cycles. Min value is (burst_width+breeze_way+17). 8 bits unsigned integer. The default value is 118. For 720p mode, the value is 260. For 1080i/p mode, the value is 192.
15:12	/	/	/
11:0	R/W	0x20	Front_Porch Must be even Specify the width of the front porch in encoder clock cycles. 6 bits unsigned even integer. Allowed range is form 10 to 62. The default value is 32. For 1080i mode, the value is 44.

5.3.7.7 0x0018 TV Encoder HD Mode VSYNC Register (Default Value: 0x0000_0016)

Offset: 0x0018			Register Name: TVE_018_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	Broad_Plus_Cycle_Number_In_HD_Mode_VSYNC
15:12	/	/	/
11:0	R/W	0x16	Front_Porch_Like_In_HD_Mode_VSYNC

5.3.7.8 0x001C TV Encoder Line Number Register (Default Value: 0x0016_020D)

Offset: 0x001C			Register Name: TVE_01C_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x16	First_Video_Line Specify the index of the first line in a field/frame to have active video. 8 bits unsigned integer.

Offset: 0x001C			Register Name: TVE_01C_REG
Bit	Read/Write	Default/Hex	Description
			For interlaced video: When VSync5=B'0', FirstVideoLine is restricted to be greater than 7. When VSync5=B'1', FirstVideoLine is restricted to be greater than 9.
15:11	/	/	/
10:0	R/W	0x20D	Num_Lines Specify the total number of lines in a video frame. 11 bits unsigned integer. Allowed range is 0 to 2048. For interlaced video: When NTSC, and FirstVideoLine is greater than 20, then NumLines is restricted to be greater than 2*(FirstVideoLine+18). When NTSC, and FirstVideoLine is not greater than 20, then NumLines is restricted to be greater than 77. When PAL, and FirstVideoLine is greater than 22, then NumLines is restricted to be greater than 2*(FirstVideoLine+18). When PAL, and FirstVideoLine is not greater than 22, then NumLines is restricted to be greater than 81. If NumLines is even, then it is restricted to be divisible by 4. If NumLines is odd, then it is restricted to be divisible by 4 with a remainder of 1.

5.3.7.9 0x0020 TV Encoder Level Register (Default Value: 0x00F0_011A)

Offset: 0x0020			Register Name: TVE_020_REG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:16	R/W	0xf0	Blank_Level Specify the blank level setting for active lines. This is 10 bits unsigned integer. Allowed range is from 0 to 1023.
15:10	/	/	/
9:0	R/W	0x11a	Black_Level Specify the black level setting. This is 10 bits unsigned integer. Allowed range is from 240 to 1023.

5.3.7.10 0x0030 TV Encoder Auto Detection Enable Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: TVE_030_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	DAC_AUTO_DETECT_MODE_SEL 0: Old Mode 1: New Mode
30:17	/	/	/
16	R/W	0x0	DAC0_Auto_Detect_Interrupt_En
15:1	/	/	/
0	R/W	0x0	DAC0_Auto_Detect_Enable

5.3.7.11 0x0034 TV Encoder Auto Detection Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: TVE_034_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W1C	0x0	DAC0_Auto_Detect_Interrupt_Active_Flag Write 1 to inactive DAC0 auto detection interrupt

5.3.7.12 0x0038 TV Encoder Auto Detection Status Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: TVE_038_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R	0x0	DAC0_Status 00: Unconnected 01: Connected 11: Short to ground 10: Reserved

5.3.7.13 0x003C TV Encoder Auto Detection Debounce Setting Register (Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: TVE_03C_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/

Offset: 0x003C			Register Name: TVE_03C_REG
Bit	Read/Write	Default/Hex	Description
25:16	R/W	0x0	DAC_TEST_REGISTER DAC test register.
15:4	/	/	/
3:0	R/W	0x0	DAC0_De_Bounce_Times The de_bounce time for hot plug detect function.

5.3.7.14 0x00F8 TV Encoder Auto Detection Configuration Register0 (Default Value: 0x0000_0000)

Offset: 0x00F8			Register Name: TVE_0F8_REG
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9:0	R/W	0x0	DETECT_Pulse_Value Use for DAC data input at auto detect pluse. Set the pulse amplitude.

5.3.7.15 0x00FC TV Encoder Auto Detection Configuration Register1 (Default Value: 0x0000_0000)

Offset: 0x00FC			Register Name: TVE_0FC_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:16	R/W	0x0	DETECT_Pulse_Periods Use 32K clock
15	/	/	/
14:0	R/W	0x0	DETECT_Pulse_Start Detect signal start time

5.3.7.16 0x0100 TV Encoder Color Burst Phase Reset Configuration Register (Default Value: 0x0000_0001)

Offset: 0x0100			Register Name: TVE_100_REG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x1	Color_Phase_Reset Color burst phase period selection

Offset: 0x0100			Register Name: TVE_100_REG
Bit	Read/Write	Default/Hex	Description
			These bits select the number of fields or lines after which the color burst phase is reset to its initial value as specified by the ChromaPhase parameter, This parameter is application only for interlaced video. 00: 8 field 01: 4 field 10: 2 lines 11: only once

5.3.7.17 0x0104 TV Encoder VSYNC Number Register (Default Value: 0x0000_0000)

Offset: 0x0104			Register Name: TVE_104_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	VSync5 Number of equalization pulse selection This bit selects whether the number of equalization pulses is 5 or 6. This parameter is applicable only for interlaced video. 0: 5 equalization pulse(default) 1: 6 equalization pulses

5.3.7.18 0x0108 TV Encoder Notch Filter Frequency Register (Default Value: 0x0000_0002)

Offset: 0x0108			Register Name: TVE_108_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2:0	R/W	0x2	Notch_Freq Luma notch filter center frequency selection These bits select the luma notch filter (which is a band-reject filter) center frequency. In two of the selections, the filter width affects also the selection of the center frequency. 000: 1.1875 001: 1.1406 010: 1.0938. When notch_wide value is B‘1’ (this selection is proper for CCIR-NTSC), or 1.0000 when notch_wide value is B‘0’.

Offset: 0x0108			Register Name: TVE_108_REG
Bit	Read/Write	Default/Hex	Description
			011: 0.9922. This selection is proper for NTSC with square pixels. 100: 0.9531. This selection is proper for PAL with square pixel. 101: 0.8359 when notch_wide value is B'1' (this selection is proper for CCIR-PAL), or 0.7734 when notch_wide value is B'0'. 110: 0.7813 111: 0.7188

5.3.7.19 0x010C TV Encoder Cb/Cr Level/Gain Register (Default Value: 0x0000_004F)

Offset: 0x010C			Register Name: TVE_10C_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:8	R/W	0x0	Cr_Burst_Level Specify the amplitude of the Cr burst. 8 bit 2's complement integer. Allowed range is from (-127) to 127.
7:0	R/W	0x4f	Cb_Burst_Level Specify the amplitude of the Cb burst. 8 bit 2's complement integer. Allowed range is from (-127) to 127.

5.3.7.20 0x0110 TV Encoder Tint and Color Burst Phase Register (Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: TVE_110_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	Tint Specify the tint adjustment of the chroma signal for CVBS and Y/C outputs. The adjustment is effected by setting the sub-carrier phase to the value of this parameter. 8.8 bit unsigned fraction. Units are cycles of the color burst frequency.
15:8	/	/	/
7:0	R/W	0x0	Chroma_Phase

Offset: 0x0110			Register Name: TVE_110_REG
Bit	Read/Write	Default/Hex	Description
			Specify the color burst initial phase (ChromaPhase). 8.8 bit unsigned fraction. Units are cycles of the color burst frequency. The color burst is set to this phase at the first HSYNC and then reset to the same value at further HSYNCs as specified by the CPhaseRset bits of the EncConfig5 parameter (see above)

5.3.7.21 0x0114 TV Encoder Burst Width Register (Default Value: 0x0016_447E)

Offset: 0x0114			Register Name: TVE_114_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	Back_Porch Breezeway like in HD mode VSync For 720p mode, the value is 220 For 2080i/p mode, the value is 88 (default)
23	/	/	/
22:16	R/W	0x16	Breezeway Must be even Specify the width of the breezeway in encoder clock cycles. 5 bit unsigned integer. Allowed range is 0 to 31. For 1080i mode, the value is 44. For 1080p mode, the value is 44. For 720p mode, the value is 40.
15	/	/	/
14:8	R/W	0x44	Burst_Width Specify the width of the color frequency burst in encoder clock cycles. 7 bit unsigned integer. Allowed range is 0 to 127. In hd mode, it is ignored.
7:0	R/W	0x7e	HSync_Width Specify the width of the horizontal sync pulse in encoder clock cycles. Min value is 16. Max value is (FrontPorch + ActiveLine - BackPorch). Default value is 126. The sum of HSyncSize and BackPorch is restricted to be divisible by 4. For 720p mode, the value is 40. For 1080i/p mode, the value is 44.

5.3.7.22 0x0118 TV Encoder Cb/Cr Gain Register (Default Value: 0x0000_A0A0)

Offset: 0x0118			Register Name: TVE_118_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:8	R/W	0xa0	Cr_Gain Specify the Cr color gain. 8-bit unsigned fraction.
7:0	R/W	0xa0	Cb_Gain Specify the Cb color gain. 8-bit unsigned fraction.

5.3.7.23 0x011C TV Encoder Sync and VBI Level Register (Default Value: 0x0010_00F0)

Offset: 0x011C			Register Name: TVE_11C_REG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:16	R/W	0x10	Sync_Level Specify the sync pulse level setting. 8-bit unsigned integer. Allowed range is from 0 to ABlankLevel-1 or VBlankLevel-1 (whichever is smaller).
15:10	/	/	/
9:0	R/W	0xf0	VBlank_Level Specify the blank level setting for non active lines. 10-bit unsigned integer. Allow range is from 0 to 1023.

5.3.7.24 0x0120 TV Encoder White Level Register (Default Value: 0x01E8_0320)

Offset: 0x0120			Register Name: TVE_120_REG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:16	R/W	0x1e8	HD_Sync_Breezeway_Level Specify the breezeway level setting. 10-bit unsigned integer. Allowed range is from 0 to 1023.
15:10	/	/	/
9:0	R/W	0x320	White_Level Specify the white level setting. 10-bit unsigned integer. Allowed range is from black_level+1 or vbi_blank_level +1 (whichever is greater) to 1023.

5.3.7.25 0x0124 TV Encoder Video Active Line Register (Default Value: 0x0000_05A0)

Offset: 0x0124			Register Name: TVE_124_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R/W	0x5A0	Active_Line Specify the width of the video line in encoder clock cycles. 12-bit unsigned multiple of 4 integer. Allowed range is from 0 to 4092.

5.3.7.26 0x0128 TV Encoder Video Chroma BW and CompGain Register (Default Value: 0x0000_0000)

Offset: 0x0128			Register Name: TVE_128_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17:16	R/W	0x0	Chroma_BW Chroma filter bandwidth selection This bit specifies whether the bandwidth of the chroma filter is: 00: Narrow width 0.6 MHz 01: Wide width 1.2 MHz 10: Extra width 1.8 MHz 11: Ultra width 2.5 MHz
15:2	/	/	/
1:0	R/W	0x0	Comp_Ch_Gain Chroma gain selection for the composite video signal. These bits specify the gain of the chroma signal for composing with the luma signal to generate the composite video signal: 00: 100% 01: 25% 10: 50% 11: 75%

5.3.7.27 0x012C TV Encoder Register (Default Value: 0x0000_0101)

Offset: 0x012C			Register Name: TVE_12C_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x1	Notch_Width Luma notch filter width selection This bit selects the luma notch filter (which is a band-reject filter) width. 0: Narrow 1: Wide
7:1	/	/	/
0	R/W	0x1	Comp_YUV_EN This bit selects if the components video output are the RGB components or the YUV components. 0: The three component outputs are the RGB components. 1: The three component outputs are the YUV components, (i.e. the color conversion unit is bypassed)

5.3.7.28 0x0130 TV Encoder Re-sync Parameters Register (Default Value: 0x0010_0001)

Offset: 0x0130			Register Name: TVE_130_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	Re_Sync_Field Re-sync field
30	R/W	0x0	Re_Sync_Dis 0: Re-Sync Enable 1: Re-Sync Disable
29:27	/	/	/
26:16	R/W	0x10	Re_Sync_Line_Num Re-sync line number from TCON
15:11	/	/	/
10:0	R/W	0x1	Re_Sync_Pixel_Num Re-sync line pixel from TCON

5.3.7.29 0x0134 TV Encoder Slave Parameter Register (Default Value: 0x0000_0000)

Offset: 0x0134			Register Name: TVE_134_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	Slave_Thresh Horizontal line adjustment threshold selection This bit selects whether the number of lines after which the Video Encoder starts the horizontal line length adjustment is slave mode is 0 or 30. 0: Number of lines is 0 1: Number of lines is 30
7:1	/	/	/
0	R/W	0x0	Slave_Mode Slave mode selection This bit selects whether the Video Encoder is sync slave, partial slave or sync master. It should be set to B'0'. 0: The Video Encoder is not a full sync slave (i.e. it is a partial sync slave or a sync master) 1: Reserved

5.3.7.30 0x0138 TV Encoder Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0138			Register Name: TVE_138_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	Invert_Top Field parity input signal (top_field) polarity selection. This bit selects whether the top field is indicated by a high level of the field parity signal or by the low level. The bit is applicable both when the Video Encoder is the sync master and when the Video Encoder is the sync slave. 0: Top field is indicated by low level 1: Top field is indicated by high level
7:1	/	/	/
0	R/W	0x0	UV_Order This bit selects if the sample order at the chroma input to the Video Encoder is Cb first (i.e. Cb 0 Cr 0 Cb 1 Cr 1) or Cr first (i.e. Cr 0 Cb 0 Cr 1 Cb 1).

Offset: 0x0138			Register Name: TVE_138_REG
Bit	Read/Write	Default/Hex	Description
			0: The chroma sample input order is Cb first 1: The chroma sample input order is Cr first

5.3.7.31 0x013C TV Encoder Configuration Register (Default Value: 0x0000_0001)

Offset: 0x013C			Register Name: TVE_13C_REG
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:24	R/W	0x0	RGB_Sync R, G and B signals sync embedding selection. These bits specify whether the sync signal is added to each of the R, G and B components (b‘1’) or not (b‘0’). The bit[26] specify if the R signal has embedded syncs, the bit[25] specify if the G signal has embedded syncs and the bit[24] specify if the B signal has embedded syncs. When comp_yuv is equal to b‘1’, these bits are N.A. and should be set to b‘000’. When the value is different from b‘000’, RGB_Setup should be set to b‘1’.
23:17	/	/	/
16	R/W	0x0	RGB_Setup “Set-up” enable for RGB outputs. This bit specifies if the “set-up” implied value (black_level – blank_level) specified for the CVBS signal is used also for the RGB signals. 0: The “set-up” is not used, or i.e. comp_yuv is equal to b‘1’. 1: The implied “set-up” is used for the RGB signals
15:1	/	/	/
0	R/W	0x1	Bypass_YClamp Y input clamping selection This bit selects whether the Video Encoder Y input is clamped to 64 to 940 or not. When not clamped the expected range is 0 to 1023. The U and V inputs are always clamped to the range 64 to 960. 0: The Video Encoder Y input is clamped 1: The Video Encoder Y input is not clamped

5.3.7.32 0x0380 TV Encoder Low Pass Control Register (Default Value: 0x0000_0000)

Offset: 0x0380			Register Name: TVE_380_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:10	R/W	0x0	User_deflicker_coef up: coef/32 Center: 1-coef/16 Down: coef/32
9	R/W	0x0	Fix_coef_deflicker 0: Auto deflicker 1: User deflicker
8	R/W	0x0	Enable_deflicker 0: Disable deflicker 1: Enable deflicker
7:1	/	/	/
0	R/W	0x0	EN LP function enable 0: Disable 1: Enable

5.3.7.33 0x0384 TV Encoder Low Pass Filter Control Register (Default Value: 0x0000_0000)

Offset: 0x0384			Register Name: TVE_384_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:16	R/W	0x0	HP_RATIO Default high-pass filter ratio In two complement, the range is from -31 to 31.
15:14	/	/	/
13:8	R/W	0x0	BP0_RATIO Default band-pass filter0 ratio In two complement, the range is from -31 to 31.
7:6	/	/	/
5:0	R/W	0x0	BP1_RATIO Default band-pass filter1 ratio In two complement, the range is from -31 to 31.

5.3.7.34 0x0388 TV Encoder Low Pass Gain Register (Default Value: 0x0000_0000)

Offset: 0x0388			Register Name: TVE_388_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	GAIN Peaking gain setting.

5.3.7.35 0x038C TV Encoder Low Pass Gain Control Register (Default Value: 0x0000_0000)

Offset: 0x038C			Register Name: TVE_38C_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	DIF_UP Gain control: limitation threshold.
15:8	/	/	/
4:0	R/W	0x0	BETA Gain control: large gain limitation.

5.3.7.36 0x0390 TV Encoder Low Pass Shoot Control Register (Default Value: 0x0000_0000)

Offset: 0x0390			Register Name: TVE_390_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5:0	R/W	0x0	NEG_GAIN Undershoot gain control.

5.3.7.37 0x0394 TV Encoder Low Pass Coring Register (Default Value: 0x0000_0000)

Offset: 0x0394			Register Name: TVE_394_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	CORTHR Coring threshold.

5.3.7.38 0x03A0 TV Encoder Noise Reduction Register (Default Value: 0x0000_0000)

Offset: 0x03A0			Register Name: TVE_3A0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	T_Value
15:1	/	/	/
0	R/W	0x0	EN

5.4 MIPI DSI

5.4.1 Overview

The Display Serial Interface is a high-speed interface between a host processor and peripheral devices that adhere to MIPI Alliance specifications for mobile device interfaces. This DSI module is composed of a DSI controller which is compliance with MIPI DSI specification V1.01 and a D-PHY module which is compliance with MIPI DPHY specification V1.00.

The MIPI DSI includes the following features:

- Compliance with MIPI DSI v1.01
- Up to 4 lanes
- Supports 1280 x 720@60fps and 1920 x 1200@60fps
- Supports non-burst mode with sync pulse/sync event and burst mode
- Supports pixel format: RGB888, RGB666, RGB666 loosely packed and RGB565
- Supports continuous lane clock mode and non-continuous lane clock mode
- Compliance with MIPI DCS v1.01, bidirectional communication in LP through data lane 0
- Supports bidirectional communication of all generic commands in LP through data lane 0
- Supports low power data transmission
- Supports ULPS and Escape modes
- Hardware checksum capabilities

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Tables

6 Video Input Interfaces

6.1 CSIC

6.1.1 Overview

The CMOS Sensor Interface Controller (CSIC) is an image or video data receiver, which can receive image or video data via camera interface and store the data in memory directly.

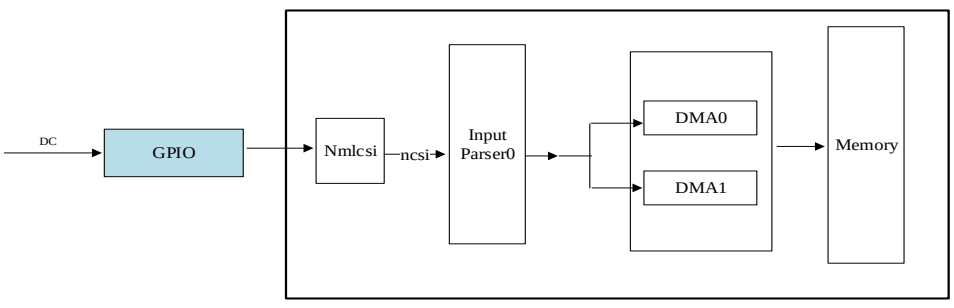
The CSIC includes the following features:

- Supports 8-bit digital camera interface
- Supports BT656 Interface
  - Supports time-multiplexed format
  - Supports dual data rate sample mode with pixel clock up to 148.5 MHz
- Supports BT601 Interface
- Supports crop function
- Supports frame rate down
- Supports 2 DMA for 2 video stream storage
  - Supports de-interlacing for interlace video input
  - Supports conversion from YUV422 to YUV420, YUV422 to YUV400, YUV420 to YUV400
  - Supports horizontal and vertical flip

6.1.2 Block Diagram

Figure 6-1 shows block diagram of the CSIC.

Figure 6-1 CSIC Block Diagram



6.1.3 Functional Description

6.1.3.1 External Signals

Table 6-1 CSIC External Signals

Port Name	Description	Type
NCSI0-PCLK	Parallel CSI Pixel Clock	I
NCSI0-MCLK	Parallel CSI Master Clock	O
NCSI0-HSYNC	Parallel CSI Horizontal Sync	I
NCSI0-VSYNC	Parallel CSI Vertical Sync	I
NCSI0-D[7:0]	Parallel CSI Data Bit	I
NCSI0-FIELD	Parallel CSI Field Index	I

6.1.3.2 CSIC FIFO Distribution

Table 6-2 CSIC FIFO Distribution

Interface	MIPI Interface		
Input format	YUV422		Raw
Output format	Planar	UV combined	Raw/RGB/PRGB
CH0_FIFO0	Y	Y	All pixels data
CH0_FIFO1	Cb (U)	CbCr (UV)	-
CH0_FIFO2	Cr (V)	-	-

6.1.3.3 Pixel Format Arrangement

Figure 6-2 RAW-10 Format

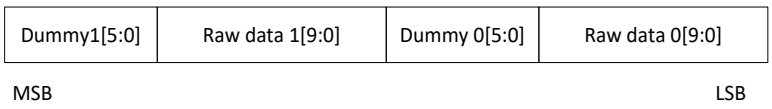


Figure 6-3 RAW-12 Format

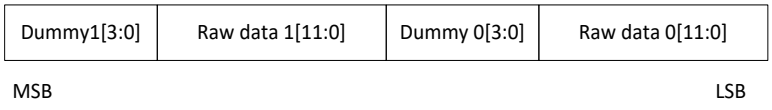


Figure 6-4 YUV-10 Format

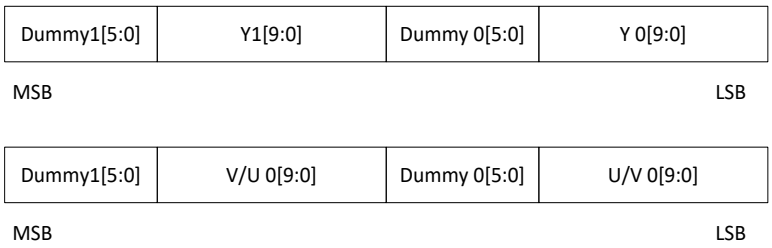


Figure 6-5 RGB888 Format

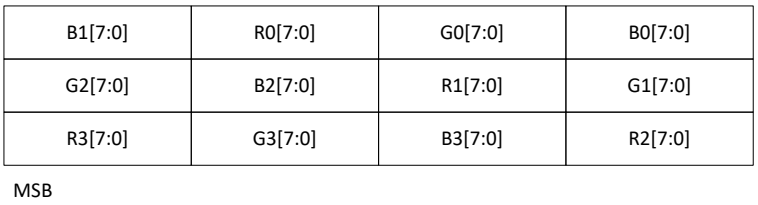


Figure 6-6 PRGB888 Format

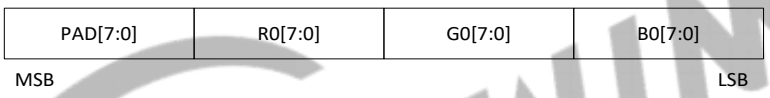
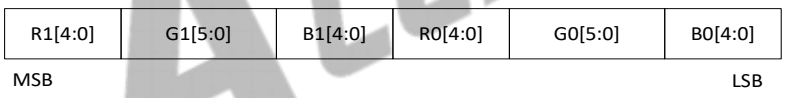


Figure 6-7 RGB565 Format



6.1.3.4 Offset Definition

Offset in horizontal and vertical can be added when receiving image. Unit is pixel.

For YUV422 format, pixel unit is a YU/YV combination.

For YUV420 format, pixel unit is a YU/YV combination in YC line, and only a Y in Y line.

For Bayer and RAW format, pixel unit is a R/G/B single component.

For RGB565, pixel unit is 2 bytes of RGB565 package.

For RGB888, pixel unit is 3 bytes of RGB combination.

6.1.3.5 Flip Definition

Both horizontal and vertical flip are supported at the same time. This function is implemented in the process of each FIFO writing data to memory, only flipping the data of separate FIFO, not changing component to FIFO distribution.

If horizontal flip is enabled, one or more pixels will be took as a unit:

For YUV format, a unit of $Y_0U_0Y_1V_1$ will parser and flip the Y component in one channel, and UV will be treated as a whole. In planar output mode, U and V will be flipped separately. In UV combined output mode, UV will be flipped as a whole. So, a sequence of $Y_1U_0Y_0V_1$ will be.

For Bayer_raw format, situation is much like. A GR/BG sequence will be changed to BG/RG. A unit of square has four pixels.

For RGB565/RGB888, one unit of two/three bytes of component will be flipped with original sequence.

6.1.4 Register List

Module Name	Base Address
CSIC_CCU	0x05800000
CSIC_TOP	0x05800800
CSIC_PARSER0	0x05801000
CSIC_DMA0	0x05809000
CSIC_DMA1	0x05809200

CCU register list:

Register Name	Offset	Register Description
CCU_CLK_MODE_REG	0x0000	CCU Clock Mode Register
CCU_PARSER_CLK_EN_REG	0x0004	CCU Parser Clock Enable Register
CCU_POST0_CLK_EN_REG	0x000C	CCU Post0 Clock Enable Register

CSIC TOP register list:

Register Name	Offset	Register Description
CSIC_TOP_EN_REG	0x0000	CSIC TOP Enable Register
CSIC_PTN_GEN_EN_REG	0x0004	CSIC Pattern Generation Enable Register
CSIC_PTN_CTRL_REG	0x0008	CSIC Pattern Control Register
CSIC_PTN_LEN_REG	0x0020	CSIC Pattern Generation Length Register
CSIC_PTN_ADDR_REG	0x0024	CSIC Pattern Generation Address Register
CSIC_PTN_ISP_SIZE_REG	0x0028	CSIC Pattern ISP Size Register
CSIC_DMA0_INPUT_SEL_REG	0x00A0	CSIC DMA0 Input Select Register
CSIC_DMA1_INPUT_SEL_REG	0x00A4	CSIC DMA1 Input Select Register
CSIC_BIST_CS_REG	0x00DC	CSIC BIST CS Register
CSIC_BIST_CONTROL_REG	0x00E0	CSIC BIST Control Register
CSIC_BIST_START_REG	0x00E4	CSIC BIST Start Register
CSIC_BIST_END_REG	0x00E8	CSIC BIST End Register
CSIC_BIST_DATA_MASK_REG	0x00EC	CSIC BIST Data Mask Register
CSIC_MBUS_REQ_MAX_REG	0x00F0	CSIC MBUS REQ MAX Register
CSIC_MULF_MOD_REG	0x0100	CSIC Multi-Frame Mode Register
CSIC_MULF_INT_REG	0x0104	CSIC Multi-Frame Interrupt Register

PARSER0 register list:

Register Name	Offset	Register Description
PRS_EN_REG	0x0000	Parser Enable Register
PRS_NCSIC_IF_CFG_REG	0x0004	Parser NCSIC Interface Configuration Register
PRS_CAP_REG	0x000C	Parser Capture Register
CSIC_PRS_SIGNAL_STA_REG	0x0010	CSIC Parser Signal Status Register
CSIC_PRS_NCSIC_BT656_HEAD_CFG_REG	0x0014	CSIC Parser NCSIC BT656 Header Configuration Register
PRS_C0_INFMT_REG	0x0024	Parser Channel_0 Input Format Register
PRS_C0_OUTPUT_HSIZE_REG	0x0028	Parser Channel_0 Output Horizontal Size Register
PRS_C0_OUTPUT_VSIZE_REG	0x002C	Parser Channel_0 Output Vertical Size Register
PRS_C0_INPUT_PARA0_REG	0x0030	Parser Channel_0 Input Parameter0 Register
PRS_C0_INPUT_PARA1_REG	0x0034	Parser Channel_0 Input Parameter1 Register
PRS_C0_INPUT_PARA2_REG	0x0038	Parser Channel_0 Input Parameter2 Register
PRS_C0_INPUT_PARA3_REG	0x003C	Parser Channel_0 Input Parameter3 Register
PRS_C0_INT_EN_REG	0x0040	Parser Channel_0 Interrupt Enable Register
PRS_C0_INT_STA_REG	0x0044	Parser Channel_0 Interrupt Status Register
PRS_CH0_LINE_TIME_REG	0x0048	Parser Channel_0 Line Time Register
PRS_C1_INFMT_REG	0x0124	Parser Channel_1 Input Format Register
PRS_C1_OUTPUT_HSIZE_REG	0x0128	Parser Channel_1 Output Horizontal Size Register
PRS_C1_OUTPUT_VSIZE_REG	0x012C	Parser Channel_1 Output Vertical Size Register

Register Name	Offset	Register Description
PRS_C1_INPUT_PARA0_REG	0x0130	Parser Channel_1 Input Parameter0 Register
PRS_C1_INPUT_PARA1_REG	0x0134	Parser Channel_1 Input Parameter1 Register
PRS_C1_INPUT_PARA2_REG	0x0138	Parser Channel_1 Input Parameter2 Register
PRS_C1_INPUT_PARA3_REG	0x013C	Parser Channel_1 Input Parameter3 Register
PRS_C1_INT_EN_REG	0x0140	Parser Channel_1 Interrupt Enable Register
PRS_C1_INT_STA_REG	0x0144	Parser Channel_1 Interrupt Status Register
PRS_CH1_LINE_TIME_REG	0x0148	Parser Channel_1 Line Time Register
PRS_C2_INFMT_REG	0x0224	Parser Channel_2 Input Format Register
PRS_C2_OUTPUT_HSIZE_REG	0x0228	Parser Channel_2 Output Horizontal Size Register
PRS_C2_OUTPUT_VSIZE_REG	0x022C	Parser Channel_2 Output Vertical Size Register
PRS_C2_INPUT_PARA0_REG	0x0230	Parser Channel_2 Input Parameter0 Register
PRS_C2_INPUT_PARA1_REG	0x0234	Parser Channel_2 Input Parameter1 Register
PRS_C2_INPUT_PARA2_REG	0x0238	Parser Channel_2 Input Parameter2 Register
PRS_C2_INPUT_PARA3_REG	0x023C	Parser Channel_2 Input Parameter3 Register
PRS_C2_INT_EN_REG	0x0240	Parser Channel_2 Interrupt Enable Register
PRS_C2_INT_STA_REG	0x0244	Parser Channel_2 Interrupt Status Register
PRS_CH2_LINE_TIME_REG	0x0248	Parser Channel_2 Line Time Register
PRS_C3_INFMT_REG	0x0324	Parser Channel_3 Input Format Register
PRS_C3_OUTPUT_HSIZE_REG	0x0328	Parser Channel_3 Output Horizontal Size Register
PRS_C3_OUTPUT_VSIZE_REG	0x032C	Parser Channel_3 Output Vertical Size Register
PRS_C3_INPUT_PARA0_REG	0x0330	Parser Channel_3 Input Parameter0 Register
PRS_C3_INPUT_PARA1_REG	0x0334	Parser Channel_3 Input Parameter1 Register
PRS_C3_INPUT_PARA2_REG	0x0338	Parser Channel_3 Input Parameter2 Register
PRS_C3_INPUT_PARA3_REG	0x033C	Parser Channel_3 Input Parameter3 Register
PRS_C3_INT_EN_REG	0x0340	Parser Channel_3 Interrupt Enable Register
PRS_C3_INT_STA_REG	0x0344	Parser Channel_3 Interrupt Status Register
PRS_CH3_LINE_TIME_REG	0x0348	Parser Channel_3 Line Time Register
CSIC_PRS_NCSIC_RX_SIGNAL0_DLY_ADJ_REG	0x0500	CSIC Parser NCSIC RX Signal0 Delay Adjust Register
CSIC_PRS_NCSIC_RX_SIGNAL5_DLY_ADJ_REG	0x0514	CSIC Parser NCSIC RX Signal5 Delay Adjust Register
CSIC_PRS_NCSIC_RX_SIGNAL6_DLY_ADJ_REG	0x0518	CSIC Parser NCSIC RX Signal6 Delay Adjust Register

DMA0/1 register list:

Register Name	Offset	Register Description
CSIC_DMA_EN_REG	0x0000	CSIC DMA Enable Register
CSIC_DMA_CFG_REG	0x0004	CSIC DMA Configuration Register
CSIC_DMA_HSIZE_REG	0x0010	CSIC DMA Horizontal Size Register
CSIC_DMA_VSIZE_REG	0x0014	CSIC DMA Vertical Size Register

Register Name	Offset	Register Description
CSIC_DMA_F0_BUFA_REG	0x0020	CSIC DMA FIFO 0 Output Buffer-A Address Register
CSIC_DMA_F0_BUFA_RESULT_REG	0x0024	CSIC DMA FIFO 0 Output Buffer-A Address Result Register
CSIC_DMA_F1_BUFA_REG	0x0028	CSIC DMA FIFO 1 Output Buffer-A Address Register
CSIC_DMA_F1_BUFA_RESULT_REG	0x002C	CSIC DMA FIFO 1 Output Buffer-A Address Result Register
CSIC_DMA_F2_BUFA_REG	0x0030	CSIC DMA FIFO 2 Output Buffer-A Address Register
CSIC_DMA_F1_BUFA_RESULT_REG	0x0034	CSIC DMA FIFO 2 Output Buffer-A Address Result Register
CSIC_DMA_BUF_LEN_REG	0x0038	CSIC DMA Buffer Length Register
CSIC_DMA_FLIP_SIZE_REG	0x003C	CSIC DMA Flip Size Register
CSIC_DMA_VI_TO_TH0_REG	0x0040	CSIC DMA Video Input Timeout Threshold0 Register
CSIC_DMA_VI_TO_TH1_REG	0x0044	CSIC DMA Video Input Timeout Threshold1 Register
CSIC_DMA_VI_TO_CNT_VAL_REG	0x0048	CSIC DMA Video Input Timeout Counter Value Register
CSIC_DMA_CAP_STA_REG	0x004C	CSIC DMA Capture Status Register
CSIC_DMA_INT_EN_REG	0x0050	CSIC DMA Interrupt Enable Register
CSIC_DMA_INT_STA_REG	0x0054	CSIC DMA Interrupt Status Register
CSIC_DMA_LINE_CNT_REG	0x0058	CSIC DMA LINE Counter Register
CSIC_DMA_FRM_CNT_REG	0x005C	CSIC DMA Frame Counter Register
CSIC_DMA_FRM_CLK_CNT_REG	0x0060	CSIC DMA Frame Clock Counter Register
CSIC_DMA_ACC_ITNL_CLK_CNT_REG	0x0064	CSIC DMA Accumulated And Internal Clock Counter Register
CSIC_DMA_FIFO_STAT_REG	0x0068	CSIC DMA FIFO Statistic Register
CSIC_DMA_FIFO_THRS_REG	0x006C	CSIC DMA FIFO Threshold Register
CSIC_DMA_PCLK_STAT_REG	0x0070	CSIC DMA PCLK Statistic Register
CSIC_DMA_BUF_ADDR_FIFO0_ENTRY_REG	0x0080	CSIC DMA BUF Address FIFO0 Entry Register
CSIC_DMA_BUF_ADDR_FIFO1_ENTRY_REG	0x0084	CSIC DMA BUF Address FIFO1 Entry Register
CSIC_DMA_BUF_ADDR_FIFO2_ENTRY_REG	0x0088	CSIC DMA BUF Address FIFO2 Entry Register
CSIC_DMA_BUF_TH_REG	0x008C	CSIC DMA BUF Threshold Register
CSIC_DMA_BUF_ADDR_FIFO_CON_REG	0x0090	CSIC DMA BUF Address FIFO Content Register
CSIC_DMA_STORED_FRM_CNT_REG	0x0094	CSIC DMA Stored Frame Counter Register
CSIC_FEATURE_REG	0x01F4	CSIC DMA Feature List Register

6.1.5 CCU Register Description

6.1.5.1 0x0000 CCU Clock Mode Register(Default Value:0x8000_0000)

Offset: 0x0000			Register Name: CCU_CLK_MODE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	CCU_CLK_GATING_DISABLE 0: CCU Clock Gating Registers(0x0004~0x0010) effect 1: CCU Clock Gating Registers(0x0004~0x0010) not effect
30:0	/	/	/

6.1.5.2 0x0004 CCU Parser Clock Enable Register(Default Value:0x0000_0000)

Offset: 0x0004			Register Name: CCU_PARSER_CLK_EN_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	MCSI_PARSER0_CLK_ENABLE 0: CSI Parser0 clock disable 1: CSI Parser0 clock enable

6.1.5.3 0x000C CCU Post0 Clock Enable Register(Default Value:0x0000_0000)

Offset: 0x000C			Register Name: CCU_POST0_CLK_EN_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	MCSI_POST0_CLK_ENABLE 0: POST0 clock disable 1: POST0 clock enable
15:2	/	/	/
1	R/W	0x0	MCSI_BK1_CLK_ENABLE 0: BK1 clock disable 1: BK1 clock enable,when MCSI_POST0_CLK_ENABLE is 1
0	R/W	0x0	MCSI_BK0_CLK_ENABLE 0: BK0 clock disable 1: BK0 clock enable,when MCSI_POST0_CLK_ENABLE is 1

6.1.6 CSIC Top Register Description

6.1.6.1 0x0000 CSIC TOP Enable Register (Default Value:0x0000_0000)

Offset: 0x0000			Register Name: CSIC_TOP_EN_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	BIST_MODE_EN 0: Closed 1: EN BIST TEST
1	/	/	/
0	R/W	0x0	CSIC_TOP_EN 0: Reset and disable the CSIC module 1: Enable the CSIC module

6.1.6.2 0x0004 CSIC Pattern Generation Enable Register (Default Value:0x0000_0000)

Offset: 0x0004			Register Name: CSIC_PTN_GEN_EN_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	PTN_CYCLE Pattern generating cycle counter. The pattern in dram will be generated in cycles of PTN_CYCLE+1.
15:5	/	/	/
4	R/WAC	0x0	PTN_START CSIC Pattern Generating Start 0: Finish 1: Start Software writes this bit to “1” to start pattern generating from DRAM. When finished, the hardware will clear this bit to “0” automatically. Generating cycles depends on PTN_CYCLE.
3:1	/	/	/
0	R/W	0x0	PTN_GEN_EN Pattern Generation Enable

6.1.6.3 0x0008 CSIC Pattern Control Register (Default Value:0x0000_000F)

Offset: 0x0008			Register Name: CSIC_PTN_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/

Offset: 0x0008			Register Name: CSIC_PTN_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
25:24	R/W	0x0	PTN_PORT_SEL Pattern Generator output port selection 10:NCSIC0 others:reserved
23:22	/	/	/
21:20	R/W	0x0	PTN_GEN_DATA_WIDTH 00:8-bit 01:10-bit 10:12-bit 11:reserved
19:16	R/W	0x0	PTN_MODE Pattern mode selection 0000–0011:reserved 0100:NCSIC YUV 8 bits width 0101:NCSIC YUV 16 bits width 0110:reserved 0111:reserved 1000:BT656 8 bits width 1001:BT656 16 bits width 1010:reserved 1011:reserved 1100:BAYER 12 bits for ISPFE 1101:UYVY422 12 bits for ISPFE 1110:UYVY420 12 bits for ISPFE 1111:reserved
15:10	/	/	/
9:8	R/W	0x0	PTN_GEN_CLK_DIV Packet generator clock divider
7:0	R/W	0xF	PTN_GEN_DLY Clocks delayed before pattern generating start.

6.1.6.4 0x0020 CSIC Pattern Generation Length Register (Default Value:0x0000_0000)

Offset: 0x0020			Register Name: CSIC_PTN_LEN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	PTN_LEN The pattern length in byte when generating pattern.

6.1.6.5 0x0024 CSIC Pattern Generation Address Register (Default Value:0x0000_0000)

Offset: 0x0024			Register Name: CSIC_PTN_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PTN_ADDR The pattern DRAM address when generating pattern.

6.1.6.6 0x0028 CSIC Pattern ISP Size Register (Default Value:0x0000_0000)

Offset: 0x0028			Register Name: CSIC_PTN_ISP_SIZE_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	Height Vertical size, only valid for ISP mode pattern generation.
15:13	/	/	/
12:0	R/W	0x0	Width Horizontal size, only valid for ISP mode pattern generation.

6.1.6.7 0x00A0 CSIC DMA0 Input Select Register (Default Value:0x0000_0000)

Offset: 0x00A0			Register Name: CSIC_DMA0_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x0	DMA0 Input Select 0000: input from ISP0 CH0 0001: input from ISP0 CH1 0010: input from ISP0 CH2 0011: input from ISP0 CH3 Others: Reserved

6.1.6.8 0x00A4 CSIC DMA1 Input Select Register (Default Value:0x0000_0000)

Offset: 0x00A4			Register Name: CSIC_DMA1_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x0	DMA1 Input Select 0000: input from ISP0 CH0 0001: input from ISP0 CH1 0010: input from ISP0 CH2

Offset: 0x00A4			Register Name: CSIC_DMA1_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
			0011: input from ISP0 CH3 Others: Reserved

6.1.6.9 0x00DC CSIC BIST CS Register (Default Value:0x0000_0000)

Offset: 0x00DC			Register Name: CSIC_BIST_CS_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2:0	R/W	0x0	BIST_CS 000: Set when BK0 memory bist 001: Set when BK1 memory bist Others: Reserved

6.1.6.10 0x00E0 CSIC BIST Control Register (Default Value:0x0000_0200)

Offset :0x00E0			Register Name: CSIC_BIST_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R	0x0	BIST_ERR_STA BIST Error Status 0: No effect 1: Error
14:12	R	0x0	BIST_ERR_PAT BIST Error Pattern
11:10	R	0x0	BIST_ERR_CYC BIST Error Cycle
9	R	0x1	BIST_STOP BIST STOP 0: Running 1: Stop
8	R	0x0	BIST_BUSY BIST Busy 0: Idle 1: Busy
7:5	R/W	0x0	BIST_REG_SEL BIST REG select
4	R/W	0x0	BIST_ADDR_Mode_SEL BIST Address Mode Select
3:1	R/W	0x0	BIST_WDATA_PAT

Offset :0x00E0			Register Name: CSIC_BIST_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			BIST Write Data Pattern 000: 0x00000000 001: 0x55555555 010: 0x33333333 011: 0x0F0F0F0F 100: 0x00FF00FF 101: 0x0000FFFF others: Reserved
0	R/W	0x0	BIST_EN BIST Enable A positive will trigger the BIST to start.

6.1.6.11 0x00E4 CSIC BIST Start Address Register (Default Value:0x0000_0000)

Offset :0x00E4			Register Name: CSIC_BIST_START_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	BIST Start Address BIST Start Address. It is 32-bit aligned.

6.1.6.12 0x00E8 CSIC BIST End Address Register (Default Value:0x0000_0000)

Offset :0x00E8			Register Name: CSIC_BIST_END_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	BIST END Address BIST END Address. It is 32-bit aligned.

6.1.6.13 0x00EC CSIC BIST Data Mask Register (Default Value:0x0000_0000)

Offset :0x00EC			Register Name: CSIC_BIST_DATA_MASK_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	BIST_DATA_MASK BIST Data Mask 0: Unmask 1: Mask

6.1.6.14 0x00F0 CSIC MBUS REQ MAX Register (Default Value:0x000F_0F0F)

Offset: 0x00F0			Register Name: CSIC_MBUS_REQ_MAX_REG
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4:0	R/W	0x0F	MCSI_MEM_REQ_MAX Maximum of request commands for the master granted in MCSI_MEM arbiter is N+1.

6.1.6.15 0x0100 CSIC Multi-Frame Mode Register (Default Value:0x0000_0000)

Offset: 0x0100			Register Name: CSIC_MULF_MOD_REG
Bit	Read/Write	Default/Hex	Description
31:24	R	0x0	MULF_STATUS
23:16	/	/	/
15:8	R/W	0x0	MULF_CS
7:1	/	/	/
0	R/W	0x0	MULF_EN

6.1.6.16 0x0104 CSIC Multi-Frame Interrupt Register (Default Value:0x0000_0000)

Offset: 0x0104			Register Name: CSIC_MULF_INT_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W1C	0x0	MULF_ERR_PD
16	R/W1C	0x0	MULF_DONE_PD
15:2	/	/	/
1	R/W	0x0	MULF_ERR_EN
0	R/W	0x0	MULF_DONE_EN

6.1.7 Parser Register Description

6.1.7.1 0x0000 Parser Enable Register (Default Value:0x0000_0000)

Offset: 0x0000			Register Name: PRS_EN_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	NCSIC_EN 0: Reset and disable the NCSIC module

Offset: 0x0000			Register Name: PRS_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			1: Enable the NCSIC module
15	R/W	0x0	PCLK_EN 0: Gate pclk input 1: Enable pclk input
14:3	/	/	/
2	R/W	0x0	PRS_CH_MODE 0: Parser output channel 0–3 corresponding from input channel 0–3 1: Parser output channel 0–3 all from input channel 0 (MIPI SEHDR)
1	R/W	0x0	PRS_MODE 0: Reserved 1: MCSI
0	R/W	0x0	PRS_EN 0: Reset and disable the parser module 1: Enable the parser module

6.1.7.2 0x0004 Parser NCSIC Interface Configuration Register (Default Value:0x0105_0080)

Offset: 0x0004			Register Name: PRS_NCSI_IF_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	YUV420_LINE_ORDER 0: YUV420 input in Y-YC-Y-YC Line Order 1: YUV420 input in YC-Y-YC-Y Line Order
30:28	/	/	/
27:24	R/W	0x1	FIELD_DT_PCLK_SHIFT Only for vsync detected field mode, the odd field permitted pclk shift = 4* FIELD_DT_PCLK_SHIFT
23:20	R/W	0x0	Source type Bit 20–23 corresponding to the SRC_TYPEs for channel0–3 0: Progressed 1: Interlaced
19	R/W	0x0	FIELD Field polarity (For YUV HV timing) 0: negative (field=0 indicates odd, field=1 indicates even) 1: positive (field=1 indicates odd, field=0 indicates even) Field sequence (For BT656 timing) 0: Normal sequence (field 0 first) 1: Inverse sequence (field 1 first)
18	R/W	0x1	VREF_POL Vref polarity

Offset: 0x0004			Register Name: PRS_NCSI_IF_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: negative 1: positive This register is not applied to CCIR656 interface.
17	R/W	0x0	HERF_POL Href polarity 0: negative 1: positive This register is not applied to CCIR656 interface.
16	R/W	0x1	CLK_POL Data clock type 0: active in rising edge 1: active in falling edge
15:14	R/W	0x0	Field_DT_MODE (only valid when CSI_IF is YUV and source type is interlaced) 00: by both field and vsync 01: by field 10: by vsync 11: reserved
13	R/W	0x0	DDR_SAMPLE_MODE_EN 0: disable 1: enable
12:11	R/W	0x0	SEQ_8PLUS2 When select IF_DATA_WIDTH to be 8+2bit, odd/even pixel byte at CSI-D[11:4] will be rearranged to D[11:2]+2'b0 at the actual CSI data bus according to these sequences: 00: 6'bx+D[9:8], D[7:0] 01: D[9:2], 6'bx+D[1:0] 10: D[7:0], D[9:8]+6'bx 11: D[7:0], 6'bx+D[9:8]
10:8	R/W	0x0	IF_DATA_WIDTH 000: 8 bit data bus 001: 10 bit data bus 010: 12 bit data bus 011: 8+2bit data bus 100: 2x8bit data bus Others: Reserved
7:6	R/W	0x2	INPUT_SEQ Input data sequence, only valid for YUV422 and YUV420 input format. All data interleaved in one channel: 00: YUYV

Offset: 0x0004			Register Name: PRS_NCSI_IF_CFG_REG
Bit	Read/Write	Default/Hex	Description
			01: YVYU 10: UYVY 11: VYUY Y and UV in separated channel: x0: UV x1: VU
5	/	/	/
4:0	R/W	0x0	CSI_IF YUV (separate syncs): 00000: RAW or YUV420/YUYV422 (each cycle one component input) Others: Reserved CCIR656 (embedded syncs): 00100: BT656 1 channel 01100: BT656 2 channels (All data interleaved in one data bus) 01110: BT656 4 channels (All data interleaved in one data bus) Others: Reserved

6.1.7.3 0x000C Parser Capture Register (Default Value:0x0000_0000)

Offset: 0x000C			Register Name: PRS_CAP_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:26	R/W	0x0	CH3_FPS_DS Fps down sample 0: no down sample 1: 1/2 fps, only receives the first frame every 2 frames 2: 1/3 fps, only receives the first frame every 3 frames 3: 1/4 fps, only receives the first frame every 4 frames 4: 1/5 fps, only receives the first frame every 4 frames …… 15: 1/16 fps, only receives the first frame every 16 frames
25	R/W	0x0	CH3_VCAP_ON Video capture control: Capture the video image data stream on channel 3. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is written to output FIFO.

Offset: 0x000C			Register Name: PRS_CAP_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			1: Enable video capture The CSI starts capturing image data at the start of the next frame.
24	RC/W	0x0	CH3_SCAP_ON Still capture control: Capture a single still image frame on channel 3. 0: Disable still capture 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self cleared and always reads as a 0.
13:12	/	/	/
21:18	R/W	0x0	CH2_FPS_DS Fps down sample 0: no down sample 1: 1/2 fps, only receives the first frame every 2 frames 2: 1/3 fps, only receives the first frame every 3 frames 3: 1/4 fps, only receives the first frame every 4 frames 4: 1/5 fps, only receives the first frame every 4 frames …… 15: 1/16 fps, only receives the first frame every 16 frames
17	R/W	0x0	CH2_VCAP_ON Video capture control: Capture the video image data stream on channel 2. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is written to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
16	RC/W	0x0	CH2_SCAP_ON Still capture control: Capture a single still image frame on channel 2. 0: Disable still capture 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self cleared and always reads as a 0.
15:14	/	/	/

Offset: 0x000C			Register Name: PRS_CAP_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
13:10	R/W	0x0	CH1_FPS_DS Fps down sample 0: no down sample 1: 1/2 fps, only receives the first frame every 2 frames 2: 1/3 fps, only receives the first frame every 3 frames 3: 1/4 fps, only receives the first frame every 4 frames 4: 1/5 fps, only receives the first frame every 4 frames …… 15: 1/16 fps, only receives the first frame every 16 frames
9	R/W	0x0	CH1_VCAP_ON Video capture control: Capture the video image data stream on channel 1. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is written to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
8	RC/W	0x0	CH1_SCAP_ON Still capture control: Capture a single still image frame on channel 1. 0: Disable still capture 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self cleared and always reads as a 0.
7:6	/	/	/
5:2	R/W	0x0	CH0_FPS_DS Fps down sample 0: no down sample 1: 1/2 fps, only receives the first frame every 2 frames 2: 1/3 fps, only receives the first frame every 3 frames 3: 1/4 fps, only receives the first frame every 4 frames 4: 1/5 fps, only receives the first frame every 4 frames …… 15: 1/16 fps, only receives the first frame every 16 frames
1	R/W	0x0	CH0_VCAP_ON Video capture control: Capture the video image data stream on channel 0. 0: Disable video capture

Offset: 0x000C			Register Name: PRS_CAP_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is written to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
0	RC/W	0x0	CH0_SCAP_ON Still capture control: Capture a single still image frame on channel 0. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self cleared and always reads as a 0.

6.1.7.4 0x0010 Parser Signal Status Register (Default Value:0x0000_0000)

Offset: 0x0010			Register Name: CSIC_PRS_SIGNAL_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R	0x0	PCLK_STA Indicates the pclk status 0: low 1: high
23:0	R	0x0	DATA_STA Indicates the Dn status (n=0–23), MSB for D23, LSB for D0 0: low 1: high

6.1.7.5 0x0014 Parser NCSIC BT656 Header Configuration Register (Default Value:0x0302_0100)

Offset: 0x0014			Register Name: CSIC_PRS_NCSIC_BT656_HEAD_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x3	CH3_ID The low 4-bit of BT656 header for channel 3 Only valid in BT656 multi-channel mode
23:20	/	/	/

Offset: 0x0014			Register Name: CSIC_PRS_NCSIC_BT656_HEAD_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
19:16	R/W	0x2	CH2_ID The low 4-bit of BT656 header for channel 2 Only valid in BT656 multi-channel mode
15:12	/	/	/
11:8	R/W	0x1	CH1_ID The low 4-bit of BT656 header for channel 1 Only valid in BT656 multi-channel mode
7:4	/	/	/
3:0	R/W	0x0	CH0_ID The low 4-bit of BT656 header for channel 0 Only valid in BT656 multi-channel mode

6.1.7.6 0x0024 Parser Channel_0 Input Format Register (Default Value:0x0000_0003)

Offset: 0x0024			Register Name: PRS_CH0_INFMT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved

6.1.7.7 0x0028 Parser Channel_0 Output Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0028			Register Name: PRS_CH0_OUTPUT_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:13	/	/	/
12:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

6.1.7.8 0x002C Parser Channel_0 Output Vertical Size Register (Default Value:0x02D0_0000)

Offset: 0x002C			Register Name: PRS_CH0_OUTPUT_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x2D0	VER_LEN Valid line number of a frame.
15:13	/	/	/
12:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

6.1.7.9 0x003C Parser Channel_0 Input Parameter0 Register (Default Value:0x0000_0000)

Offset: 0x0030			Register Name: PRS_CH0_INPUT_PARA0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE 0: Progress 1: Interlace

6.1.7.10 0x0034 Parser Channel_0 Input Parameter1 Register (Default Value:0x0000_0000)

Offset: 0x0034			Register Name: PRS_CH0_INPUT_PARA1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_VT INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT INPUT_HT = INPUT_HB+INPUT_X

6.1.7.11 0x0038 Parser Channel_0 Input Parameter2 Register (Default Value:0x0000_0000)

Offset: 0x0038			Register Name: PRS_CH0_INPUT_PARA2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_VB
15:14	/	/	/
13:0	R	0x0	INPUT_HB

6.1.7.12 0x003C Parser Channel_0 Input Parameter3 Register (Default Value:0x0000_0000)

Offset: 0x003C			Register Name: PRS_CH0_INPUT_PARA3_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_X

6.1.7.13 0x0040 Parser Channel_0 Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0040			Register Name: PRS_CH0_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN 0: disable 1: enable
0	R/W	0x0	INPUT_PARA0_INT_EN 0: disable 1: enable

6.1.7.14 0x0044 Parser Channel_0 Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0044			Register Name: PRS_CH0_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W1C	0x0	MUL_ ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update,this flag set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register, parser input parameter2 register or parser input parameter3 register update, this flag set to 1. Write 1 to clear.

6.1.7.15 0x0048 Parser Channel_0 Line Time Register (Default Value:0x0000_0000)

Offset: 0x0048			Register Name: PRS_CH0_LINE_TIME_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	RO	0x0	PRS_CH0_HBLK_TIME Time of H Blanking when vsync is valid The unit is csi_top_clk cycle
15:0	RO	0x0	PRS_CH0_HSYN_TIME Time of H SYNC when vsync is valid The unit is csi_top_clk cycle

6.1.7.16 0x0124 Parser Channel_1 Input Format Register (Default Value:0x0000_0003)

Offset: 0x0124			Register Name: PRS_CH1_INFMT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved

6.1.7.17 0x0128 Parser Channel_1 Output Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0128			Register Name: PRS_CH1_OUTPUT_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:13	/	/	/
12:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

6.1.7.18 0x012C Parser Channel_1 Output Vertical Size Register (Default Value:0x02D0_0000)

Offset: 0x012C			Register Name: PRS_CH1_OUTPUT_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x2d0	VER_LEN Valid line number of a frame.
15:13	/	/	/
12:0	R/W	0x0	VER_START Vertical line start. Data is valid from this line.

6.1.7.19 0x0130 Parser Channel_1 Input Parameter0 Register (Default Value:0x0000_0000)

Offset: 0x0130			Register Name: PRS_CH1_INPUT_PARA0_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE 0: Progress 1: Interlace

6.1.7.20 0x0134 Parser Channel_1 Input Parameter1 Register (Default Value:0x0000_0000)

Offset: 0x0134			Register Name: PRS_CH1_INPUT_PARA1_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VT INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT INPUT_HT = INPUT_HB+INPUT_X

6.1.7.21 0x0138 Parser Channel_1 Input Parameter2 Register (Default Value:0x0000_0000)

Offset: 0x0138			Register Name: PRS_CH1_INPUT_PARA2_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VB
15:14	/	/	/

Offset: 0x0138			Register Name: PRS_CH1_INPUT_PARA2_REG
Bit	Read/Write	Default/Hex	Description
13:0	R	0x0	INPUT_HB

6.1.7.22 0x013C Parser Channel_1 Input Parameter3 Register (Default Value:0x0000_0000)

Offset: 0x013C			Register Name: PRS_CH1_INPUT_PARA3_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_X

6.1.7.23 0x0140 Parser Channel_1 Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0140			Register Name: PRS_CH1_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN 0: Disable 1: Enable
0	R/W	0x0	INPUT_PARA0_INT_EN 0: Disable 1: Enable

6.1.7.24 0x0144 Parser Channel_1 Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0144			Register Name: PRS_CH1_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W1C	0x0	MUL_ ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update, this flag is set to 1. Write 1 to clear.

Offset: 0x0144			Register Name: PRS_CH1_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register, parser input parameter2 register or parser input parameter3 register update, this flag is set to 1. Write 1 to clear.

6.1.7.25 0x0148 Parser Channel_1 Line Time Register (Default Value:0x0000_0000)

Offset: 0x0148			Register Name: PRS_CH1_LINE_TIME_REG
Bit	Read/Write	Default/Hex	Description
31:16	RO	0x0	PRS_CH1_HBLK_TIME Time of H Blanking when vsync is valid The unit is csi_top_clk cycle.
15:0	RO	0x0	PRS_CH1_HSYN_TIME Time of H SYNC when vsync is valid The unit is csi_top_clk cycle.

6.1.7.26 0x0224 Parser Channel_2 Input Format Register (Default Value:0x0000_0003)

Offset: 0x0224			Register Name: PRS_CH2_INFMT_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved

6.1.7.27 0x0228 Parser Channel_2 Output Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0228			Register Name: PRS_CH2_OUTPUT_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:13	/	/	/

Offset: 0x0228			Register Name: PRS_CH2_OUTPUT_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
12:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

6.1.7.28 0x022C Parser Channel_2 Output Vertical Size Register (Default Value:0x02D0_0000)

Offset: 0x022C			Register Name: PRS_CH2_OUTPUT_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x2D0	VER_LEN Valid line number of a frame.
15:13	/	/	/
12:0	R/W	0x0	VER_START Vertical line start. Data is valid from this line.

6.1.7.29 0x0230 Parser Channel_2 Input Parameter0 Register (Default Value:0x0000_0000)

Offset: 0x0230			Register Name: PRS_CH2_INPUT_PARA0_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE 0:Progress 1:Interlace

6.1.7.30 0x0234 Parser Channel_2 Input Parameter1 Register (Default Value:0x0000_0000)

Offset: 0x0234			Register Name: PRS_CH2_INPUT_PARA1_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VT INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT INPUT_HT = INPUT_HB+INPUT_X

6.1.7.31 0x0238 Parser Channel_2 Input Parameter2 Register (Default Value:0x0000_0000)

Offset: 0x0238			Register Name: PRS_CH2_INPUT_PARA2_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VB
15:14	/	/	/
13:0	R	0x0	INPUT_HB

6.1.7.32 0x023C Parser Channel_2 Input Parameter3 Register (Default Value:0x0000_0000)

Offset: 0x023C			Register Name: PRS_CH2_INPUT_PARA3_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_X

6.1.7.33 0x0240 Parser Channel_2 Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0240			Register Name: PRS_CH2_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN 0: disable 1: enable
0	R/W	0x0	INPUT_PARA0_INT_EN 0: disable 1: enable

6.1.7.34 0x0244 Parser Channel_2 Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0244			Register Name: PRS_CH2_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/

Offset: 0x0244			Register Name: PRS_CH2_INT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
2	R/W1C	0x0	MUL_ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update, this flag set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register, parser input parameter2 register or parser input parameter3 register update, this flag set to 1. Write 1 to clear.

6.1.7.35 0x0248 Parser Channel_2 Line Time Register (Default Value:0x0000_0000)

Offset: 0x0248			Register Name: PRS_CH2_LINE_TIME_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	RO	0x0	PRS_CH2_HBLK_TIME Time of H Blanking when vsync is valid The unit is csi_top_clk cycle
15:0	RO	0x0	PRS_CH2_HSYN_TIME Time of H SYNC when vsync is valid The unit is csi_top_clk cycle

6.1.7.36 0x0324 Parser Channel_3 Input Format Register (Default Value:0x0000_0003)

Offset: 0x0324			Register Name: PRS_CH3_INFMT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved

6.1.7.37 0x0328 Parser Channel_3 Output Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0328			Register Name: PRS_CH3_OUTPUT_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:13	/	/	/
12:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

6.1.7.38 0x032C Parser Channel_3 Output Vertical Size Register (Default Value:0x02D0_0000)

Offset: 0x032C			Register Name: PRS_CH3_OUTPUT_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x2d0	VER_LEN Valid line number of a frame.
15:13	/	/	/
12:0	R/W	0x0	VER_START Vertical line start. Data is valid from this line.

6.1.7.39 0x0330 Parser Channel_3 Input Parameter0 Register (Default Value:0x0000_0000)

Offset: 0x0330			Register Name: PRS_CH3_INPUT_PARA0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE 0:Progress 1:Interlace

6.1.7.40 Parser Channel_3 Input Parameter1 Register (Default Value:0x0000_0000)

Offset: 0x0334			Register Name: PRS_CH3_INPUT_PARA1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_VT INPUT_VT = INPUT_VB+INPUT_Y

Offset: 0x0334			Register Name: PRS_CH3_INPUT_PARA1_REG
Bit	Read/Write	Default/Hex	Description
15:14	/	/	/
13:0	R	0x0	INPUT_HT INPUT_HT = INPUT_HB+INPUT_X

6.1.7.41 0x0338 Parser Channel_3 Input Parameter2 Register (Default Value:0x0000_0000)

Offset: 0x0338			Register Name: PRS_CH3_INPUT_PARA2_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VB
15:14	/	/	/
13:0	R	0x0	INPUT_HB

6.1.7.42 0x033C Parser Channel_3 Input Parameter3 Register(Default Value:0x0000_0000)

Offset: 0x033C			Register Name: PRS_CH3_INPUT_PARA3_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_X

6.1.7.43 0x0340 Parser Channel_3 Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0340			Register Name: PRS_CH3_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN 0:disable 1:enable
0	R/W	0x0	INPUT_PARA0_INT_EN 0:disable 1:enable

6.1.7.44 0x0344 Parser Channel_3 Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0344			Register Name: PRS_CH3_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W1C	0x0	MUL_ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update, this flag is set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register, parser input parameter2 register or parser input parameter3 register update, this flag is set to 1. Write 1 to clear.

6.1.7.45 0x0348 Parser Channel_3 Line Time Register (Default Value:0x0000_0000)

Offset: 0x0348			Register Name: PRS_CH3_LINE_TIME_REG
Bit	Read/Write	Default/Hex	Description
31:16	RO	0x0	PRS_CH3_HBLK_TIME Time of H Blanking when vsync is valid The unit is csi_top_clk cycle
15:0	RO	0x0	PRS_CH3_HSYN_TIME Time of H SYNC when vsync is valid The unit is csi_top_clk cycle

6.1.7.46 0x0500 CSIC Parser NCSIC RX Signal0 Delay Adjust Register (Default Value:0x0000_0000)

Offset: 0x0500			Register Name: CSIC_PRS_NCSIC_RX_SIGNAL0_DLY_ADJ_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x0	Filed_dly 32 Step for adjust, 1 step = 0.2 ns
23:21	/	/	/
20:16	R/W	0x0	Vsync_dly 32 Step for adjust, 1 step = 0.2 ns
15:13	/	/	/
12:8	R/W	0x0	Hsync_dly 32 Step for adjust, 1 step = 0.2 ns

Offset: 0x0500			Register Name: CSIC_PRS_NCSIC_RX_SIGNAL0_DLY_ADJ_REG
Bit	Read/Write	Default/Hex	Description
7:5	/	/	/
4:0	R/W	0x0	Pclk_dly 32 Step for adjust, 1 step = 0.2 ns

6.1.7.47 0x0514 CSIC Parser NCSIC RX Signal5 Delay Adjust Register (Default Value:0x0000_0000)

Offset: 0x0514			Register Name: CSIC_PRS_NCSIC_RX_SIGNAL5_DLY_ADJ_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x0	D7_dly 32 Step for adjust, 1 step = 0.2 ns
23:21	/	/	/
20:16	R/W	0x0	D6_dly 32 Step for adjust, 1 step = 0.2 ns
15:13	/	/	/
12:8	R/W	0x0	D5_dly 32 Step for adjust, 1 step = 0.2 ns
7:5	/	/	/
4:0	R/W	0x0	D4_dly 32 Step for adjust, 1 step = 0.2 ns

6.1.7.48 0x0518 CSIC Parser NCSIC RX Signal6 Delay Adjust Register (Default Value:0x0000_0000)

Offset: 0x0518			Register Name: CSIC_PRS_NCSIC_RX_SIGNAL6_DLY_ADJ_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x0	D3_dly 32 Step for adjust, 1 step = 0.2 ns
23:21	/	/	/
20:16	R/W	0x0	D2_dly 32 Step for adjust, 1 step = 0.2 ns
15:13	/	/	/
12:8	R/W	0x0	D1_dly 32 Step for adjust, 1 step = 0.2 ns
7:5	/	/	/
4:0	R/W	0x0	D0_dly 32 Step for adjust, 1 step = 0.2 ns

6.1.8 CSIC DMA Register Description

6.1.8.1 0x0000 CSIC DMA Enable Register (Default Value:0x7000_0000)

Offset:0x0000			Register Name: CSIC_DMA_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	VER_EN
30	R/W	0x1	VFLIP_BUF_ADDR_CFG_MODE Vflip buffer address set by software or calculated by hardware 0: Hardware 1: Software
29	R/W	0x1	BUF_LENGTH_CFG_MODE Buffer length set by software or calculated by hardware 0: Hardware 1: Software
28	R/W	0x1	FLIP_SIZE_CFG_MODE FLIP SIZE set by software or calculated by hardware 0: Hardware 1: Software
27:8	/	/	/
7	R/W	0x0	BUF_ADDR_MODE 0: Buffer Address Register Mode 1: Buffer Address FIFO Mode
6	R/W	0x0	VI_TO_CNT_EN Enable Video Input Timeout counter, add 1 when there is no effective video input in a 12M clock, clear to 0 when detecting effective video input. 0: Disable 1: Enable
5	R/W	0x0	FRAME_CNT_EN When BK_TOP_EN is enabled, setting 1 to this bit indicates the Frame counter starts to add. 0: Disable 1: Enable
4	R/W	0x0	DMA_EN When BK_TOP_EN is enabled, setting 1 to this bit indicates the module works in DMA mode. 0: Disable 1: Enable
3	/	/	/
2	R/W	0x0	CLK_CNT_SPL Sampling time for clk counter per frame 0: Sampling clock counter every frame done 1: Sampling clock counter every vsync

Offset:0x0000			Register Name: CSIC_DMA_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
1	R/W	0x0	CLK_CNT_EN clk count per frame enable
0	R/W	0x0	BK_TOP_EN 0: Disable 1: Enable

6.1.8.2 0x0004 CSIC DMA Configuration Register (Default Value:0x0000_0000)

Offset: 0x0004			Register Name: CSIC_DMA_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	PAD_VAL Padding value when OUTPUT_FMT is prgb888 0x00–0xff
23:22	/	/	/
21	R/W	0x0	YUV 10-bit input cut to 8-bit 0: Disable 1: Enable
20	R/W	0x0	YUV 10-bit store configuration 0: YUV 10-bit stored in low 10-bit of a 16-bit word 1: YUV 10-bit stored in high 10-bit of a 16-bit word
19:16	R/W	0x0	OUTPUT_FMT Output data format When the input format is set to RAW stream 0000: field-raw-8 0001: field-raw-10 0010: field-raw-12 0011: reserved 0100: field-rgb565 0101: field-rgb888 0110: field-prgb888 0111: reserved 1000: frame-raw-8 1001: frame-raw-10 1010: frame-raw-12 1011: reserved 1100: frame-rgb565 1101: frame-rgb888 1110: frame-prgb888 1111: reserved When the input format is set to YUV422

Offset: 0x0004			Register Name: CSIC_DMA_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined (UV sequence) 0101: field planar YCbCr 420 UV combined (UV sequence) 0110: frame planar YCbCr 420 UV combined (UV sequence) 0111: frame planar YCbCr 422 UV combined (UV sequence) 1000: filed planar YCbCr 422 UV combined (VU sequence) 1001: field planar YCbCr 420 UV combined (VU sequence) 1010: frame planar YCbCr 420 UV combined (VU sequence) 1011: frame planar YCbCr 422 UV combined (VU sequence) 1100: reserved 1101: field YCbCr 400 1110: reserved 1111: frame YCbCr 400 When the input format is set to YUV420 0000: reserved 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: reserved 0100: reserved 0101: field planar YCbCr 420 UV combined (UV sequence) 0110: frame planar YCbCr 420 UV combined (UV sequence) 0111~1000: reserved 1001: field planar YCbCr 420 UV combined (VU sequence) 1010: frame planar YCbCr 420 UV combined (VU sequence) 1011~1100: reserved 1101: field YCbCr 400 1110: reserved 1111: frame YCbCr 400
15:14	/	/	/
13	R/W	0x0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0: Disable 1: Enable
12	R/W	0x0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0: Disable

Offset: 0x0004			Register Name: CSIC_DMA_CFG_REG
Bit	Read/Write	Default/Hex	Description
			1: Enable
11:10	R/W	0x0	FIELD_SEL Field selection 00: Capturing with field 0 01: Capturing with field 1 10: Capturing with either field 11: Reserved
9:6	R/W	0x0	FPS_DS Fps down sample 0: no down sample 1: 1/2 fps, only receives the first frame every 2 frames 2: 1/3 fps, only receives the first frame every 3 frames 3: 1/4 fps, only receives the first frame every 4 frames 4: 1/5 fps, only receives the first frame every 4 frames …… 15: 1/16 fps, only receives the first frame every 16 frames
5:2	/	/	/
1:0	R/W	0x0	MIN_SDR_WR_SIZE Minimum size of SDRAM block write 00: 256 bytes (if hflip is enabled, always select 256 bytes) 01: 512 bytes 10: 1K bytes 11: 2K bytes

6.1.8.3 0x0010 CSIC DMA Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0010			Register Name: CSIC_DMA_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x500	HOR_LEN When BK_TOP_EN is enabled, DMA_EN is enabled, these bits indicate Horizontal pixel unit length. Valid pixel of a line in DMA mode.
15:13	/	/	/
12:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

6.1.8.4 0x0014 CSIC DMA Vertical Size Register (Default Value:0x02D0_0000)

Offset: 0x0014			Register Name: CSIC_DMA_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x2D0	VER_LEN When BK_TOP_EN is enabled, DMA_EN is enabled, these bits indicate Valid line number of a frame in DMA mode.
15:13	/	/	/
12:0	R/W	0x0	VER_START Vertical line start Data is valid from this line.

6.1.8.5 0x0020 CSIC DMA FIFO 0 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0020			Register Name: CSIC_DMA_F0_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	F0_BUFA When BK_TOP_EN is enabled, FBC_EN is enabled, DMA_EN is disabled, these bits indicate output address of overhead data in FBC mode. When BK_TOP_EN is enabled, FBC_EN is disabled, DMA_EN is enabled, LBC_EN is disabled, these bits indicate FIFO 0 output buffer-A address in DMA mode. When BK_TOP_EN is enabled, FBC_EN is disabled, DMA_EN is enabled, LBC_EN is enabled, these bits indicate the output buffer address in LBC mode.

6.1.8.6 0x0024 CSIC DMA FIFO 0 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x0024			Register Name: CSIC_DMA_F0_BUFA_RESULT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	RO	0x0	F0_BUFA_RESULT Indicate the final F0_BUFA address used for DMA or FBC after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

6.1.8.7 0x0028 CSIC DMA FIFO 1 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0028			Register Name: CSIC_DMA_F1_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F1_BUFA When BK_TOP_EN is enabled, FBC_EN is enabled, DMA_EN is disabled, these bits indicate the output address of compressed data in FBC mode. When BK_TOP_EN is enabled, FBC_EN is disabled, DMA_EN is enabled, these bits indicate the FIFO 1 output buffer-A address in DMA mode.

6.1.8.8 0x002C CSIC DMA FIFO 1 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x002C			Register Name: CSIC_DMA_F1_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	RO	0x0	F1_BUFA_RESULT Indicate the final F1_BUFA address used for DMA or FBC after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

6.1.8.9 0x0030 CSIC DMA FIFO 2 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0030			Register Name: CSIC_DMA_F2_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F2_BUFA FIFO 2 output buffer-A address.

6.1.8.10 0x0034 CSIC DMA FIFO 2 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x0034			Register Name: CSIC_DMA_F2_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	RO	0x0	F2_BUFA_RESULT Indicate the final F2_BUFA address used for DMA or FBC after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

6.1.8.11 0x0038 CSIC DMA Buffer Length Register (Default Value:0x0280_0500)

Offset: 0x0038			Register Name: CSIC_DMA_BUF_LEN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R/W	0x280	BUF_LEN_C DMA_MODE: Buffer length of chroma C in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y in ONLY Y line. Unit is byte. Only Readable when BUF_LENGTH_CFG_MODE is set 0.
15:14	/	/	/
13:0	R/W	0x500	BUF_LEN DMA_MODE:Buffer length of luminance Y in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y and chroma C in YC line. Unit is byte. Only Readable when BUF_LENGTH_CFG_MODE is set 0.

6.1.8.12 0x003C CSIC DMA Flip Size Register (Default Value:0x02D0_0500)

Offset: 0x003C			Register Name: CSIC_DMA_FLIP_SIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x2d0	VER_LEN Vertical line number when in VFLIP mode. Unit is line. Only Readable when FLIP_SIZE_CFG_MODE is set to 0.
15:14	/	/	/
13:0	R/W	0x500	VALID_LEN Valid components of a line when in HFLIP mode. Unit is pixel component. Only Readable when FLIP_SIZE_CFG_MODE is set to 0.

6.1.8.13 0x0040 CSIC DMA Video Input Timeout Threshold0 Register (Default Value:0x0000_0000)

Offset: 0x0040			Register Name: CSIC_DMA_VI_TO_TH0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	Video Input Timeout Threshold0 Set VIDEO_INPUT_TO_INT_PD when VI Counter reaches TH0 after VI_TO_CNT_EN is set, the Time Unit is a 12M clock period.

6.1.8.14 0x0044 CSIC DMA Video Input Timeout Threshold1 Register(Default Value:0x0000_0000)

Offset: 0x0044			Register Name: CSIC_DMA_VI_TO_TH1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	Video Input Timeout Threshold1 Set VIDEO_INPUT_TO_INT_PD when VI Counter reaches TH1 after getting the first frame has been input, the Time Unit is a 12M clock period.

6.1.8.15 0x0048 CSIC DMA Video Input Timeout Counter Value Register (Default Value:0x0000_0000)

Offset: 0x0048			Register Name: CSIC_DMA_VI_TO_CNT_VAL_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	Video Input Timeout Counter Value Indicate the current value of Video Input Timeout Counter

6.1.8.16 0x004C CSIC DMA Capture Status Register (Default Value:0x0000_0000)

Offset: 0x004C			Register Name: CSIC_DMA_CAP_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R	0x0	FIELD_STA The status of the received field 0: Field 0 1: Field 1
1	R	0x0	VCAP_STA Video capture in progress Indicates the CSI is capturing video image data (multiple frames). The bit is set at the start of the first frame after enabling video capture. When software disables video capture, it clears itself after the last pixel of the current frame is captured.
0	R	0x0	SCAP_STA Still capture in progress Indicates the CSI is capturing still image data (single frame). The bit is set at the start of the first frame after enabling still frame capture. It clears itself after the last pixel of the first frame is captured. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means filed end.

6.1.8.17 0x0050 CSIC DMA Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0050			Register Name: CSIC_DMA_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	FRM_LOST_INT_EN Set an INT when frame starts with empty Buffer Address FIFO, only use in BUF Address FIFO MODE.
14	R/W	0x0	STORED_FRM_CNT_INT_EN Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD, only use in BUF Address FIFO MODE.
13	R/W	0x0	BUF_ADDR_FIFO_INT_EN Set an INT when content in BUF Address FIFO less than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE.
12	R/W	0x0	VIDEO_INPUT_TO_INT_EN Set an INT when no video input exceeds the setting threshold time
11	R/W	0x0	CLR_FRAME_CNT_INT_EN Set a INT when clear Frame cnt.
10:8	/	/	/
7	R/W	0x0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, changing the buffer address could only effect next frame
6	R/W	0x0	HB_OF_INT_EN Hblank FIFO overflow The bit is set when 3 FIFOs still overflow after the hblank.
5	R/W	0x0	LC_INT_EN Line counter flag The bit is set when the specific line has been written to dram every frame. The line number is set in the line counter register.
4	R/W	0x0	FIFO2_OF_INT_EN FIFO 2 overflow The bit is set when the FIFO 2 became overflow.
3	R/W	0x0	FIFO1_OF_INT_EN FIFO 1 overflow The bit is set when the FIFO 1 became overflow.
2	R/W	0x0	FIFO0_OF_INT_EN FIFO 0 overflow The bit is set when the FIFO 0 became overflow.
1	R/W	0x0	FD_INT_EN

Offset: 0x0050			Register Name: CSIC_DMA_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
			Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is written to buffer as long as video capture remains enabled.
0	R/W	0x0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been written to buffer. For video capture, the bit is set when the last frame has been written to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

6.1.8.18 0x0054 CSIC DMA Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0054			Register Name: CSIC_DMA_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W1C	0x0	FRM_LOST_INT_PD Set an INT when frame starts with empty Buffer Address FIFO, only use in BUF Address FIFO MODE.
14	R/W1C	0x0	STORED_FRM_CNT_INT_PD Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD, only use in BUF Address FIFO MODE.
13	R/W1C	0x0	BUF_ADDR_FIFO_INT_PD Set an INT when content in BUF Address FIFO less than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE.
12	R/W1C	0x0	VIDEO_INPUT_TO_INT_PD Set an INT Pending when no video input exceeds the setting threshold time.
11	R/W1C	0x0	CLR_FRAME_CNT_INT Set a INT when clear Frame cnt.
10:8	/	/	/
7	R/W1C	0x0	VS_PD vsync flag
6	R/W1C	0x0	LI_OF_PD

Offset: 0x0054			Register Name: CSIC_DMA_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
			Line information FIFO (16 lines) overflow
5	R/W1C	0x0	LC_PD Line counter flag
4	R/W1C	0x0	FIFO2_OF_PD FIFO 2 overflow
3	R/W1C	0x0	FIFO1_OF_PD FIFO 1 overflow
2	R/W1C	0x0	FIFO0_OF_PD FIFO 0 overflow
1	R/W1C	0x0	FD_PD Frame done
0	R/W1C	0x0	CD_PD Capture done

6.1.8.19 0x0058 CSIC DMA Line Counter Register (Default Value:0x0000_0000)

Offset: 0x0058			Register Name: CSIC_DMA_LINE_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	LINE_CNT_NUM The LINE_CNT_NUM value is set by user,when internal line counter reach the set value, the LC_PD will be set.

6.1.8.20 0x005C CSIC DMA Frame Counter Register (Default Value:0x0001_0000)

Offset: 0x005C			Register Name: CSIC_DMA_FRM_CNT_REG
Bit	Read/Write	Default/Hex	Description
31	R/W1C	0x0	FRM_CNT_CLR When the bit set to 1, Frame cnt is cleared to 0.
30:16	R/W	0x1	PCLK_DMA_CLR_DISTANCE Frame cnt clear cycle $N*T_{SYNC}$
15:0	R	0x0	FRM_CNT Counter value of frame. When frame done comes, the internal counter value add 1, and when the reg full, it is cleared to 0 . When parser sent a sync signal, it is cleared to 0.

6.1.8.21 0x0060 CSIC DMA Frame Clock Counter Register (Default Value:0x0000_0000)

Offset: 0x0060			Register Name: CSIC_DMA_FRM_CLK_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R	0x0	FRM_CLK_CNT Counter value between every frame. For instant hardware frame rate statics. The internal counter is added by one every 12 MHz clock cycle. When frame done or vsync comes, the internal counter value is sampled to FRM_CLK_CNT, and cleared to 0.

6.1.8.22 0x0064 CSIC DMA Accumulated and Internal Clock Counter Register (Default Value:0x0000_0000)

Offset: 0x0064			Register Name: CSIC_DMA_ACC_ITNL_CLK_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/WC	0x0	ACC_CLK_CNT The accumulated value of FRM_CLK_CNT for software frame rate statics. Every interrupt of frame is done, the software checks this accumulated value and clears it to 0. If the ACC_CLK_CNT is larger than 1, the software has lost frame. When frame done or vsync comes, ACC_CLK_CNT = ACC_CLK_CNT + 1, and cleared to 0 when writing this register.
23:0	R	0x0	ITNL_CLK_CNT The instant value of internal frame clock counter. When frame done interrupt comes, the software can query this counter for judging whether it is the time for updating the double buffer address registers.

6.1.8.23 0x0068 CSIC DMA FIFO Statistic Register (Default Value:0x0000_0000)

Offset: 0x0068			Register Name: CSIC_DMA_FIFO_STAT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	Line Index Indicates the line index in current vsync.
15:13	/	/	/
12:0	R	0x0	FIFO_FRM_MAX Indicates the maximum depth of FIFO being occupied for whole frame. Update at every vsync or framedone.

6.1.8.24 0x006C CSIC DMA FIFO Threshold Register (Default Value:0x0000_0400)

Offset: 0x006C			Register Name: CSIC_DMA_FIFO_THRS_REG
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R/W	0x400	FIFO_THRS When FIFO occupied memory exceed the threshold, dram frequency can not change.

6.1.8.25 0x0070 CSIC DMA PCLK Statistic Register (Default Value:0x0000_7FFF)

Offset: 0x0070			Register Name: CSIC_DMA_PCLK_STAT_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:16	R	0x0	PCLK_CNT_LINE_MAX Indicates maximum pixel clock counter value for each line. Update at every vsync or framedone.
15	/	/	/
14:0	R	0x7FFF	PCLK_CNT_LINE_MIN Indicates minimum pixel clock counter value for each line. Update at every vsync or framedone.

6.1.8.26 0x0080 CSIC DMA BUF Address FIFO0 Entry Register (Default Value:0x0000_0000)

Offset: 0x0080			Register Name: CSIC_DMA_BUF_ADDR_FIFO0_ENTRY_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CSIC_DMA_BUF_ADDR_FIFO0_ENTRY FIFO Entry of Buffer Address FIFO0 for input frames to be stored, only used in Buffer Addr FIFO Mode

6.1.8.27 0x0084 CSIC DMA BUF Address FIFO1 Entry Register (Default Value:0x0000_0000)

Offset: 0x0084			Register Name: CSIC_DMA_BUF_ADDR_FIFO1_ENTRY_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CSIC_DMA_BUF_ADDR_FIFO1_ENTRY FIFO Entry of Buffer Address FIFO1 for input frames to be stored, only used in Buffer Addr FIFO Mode.

6.1.8.28 0x0088 CSIC DMA BUF Address FIFO2 Entry Register (Default Value:0x0000_0000)

Offset: 0x0088			Register Name: CSIC_DMA_BUF_ADDR_FIFO2_ENTRY_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	CSIC_DMA_BUF_ADDR_FIFO2_ENTRY FIFO Entry of Buffer Address FIFO2 for input frames to be stored, only used in Buffer Addr FIFO Mode.

6.1.8.29 0x008C CSIC DMA BUF Threshold Register (Default Value:0x0020_0000)

Offset: 0x008C			Register Name: CSIC_DMA_BUF_TH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
21:16	R/W	0x20	CSIC_DMA_STORED_FRM_THRESHOLD when stored frame counter value reaches the threshold , counter is cleared to 0 , only used in Buffer Addr FIFO Mode.
15:6	/	/	/
5:0	R/W	0x0	CSIC_DMA_BUF_ADDR_FIFO_THRESHOLD when content in Buffer Address FIFO less than the threshold, an interrupt is set, only used in Buffer Addr FIFO Mode.

6.1.8.30 0x0090 CSIC DMA BUF Address FIFO Content Register (Default Value:0x0000_0000)

Offset: 0x0090			Register Name: CSIC_DMA_BUF_ADDR_FIFO_CON_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:16	RO	0x0	CSIC_DMA_BUF_ADDR_FIFO2_CONTENT FIFO Content of address buffered in Buffer Address FIFO2, only used in Buffer Addr FIFO Mode.
15:14	/	/	/
13:8	RO	0x0	CSIC_DMA_BUF_ADDR_FIFO1_CONTENT FIFO Content of address buffered in Buffer Address FIFO1, only used in Buffer Addr FIFO Mode.
7:6	/	/	/
5:0	RO	0x0	CSIC_DMA_BUF_ADDR_FIFO0_CONTENT FIFO Content of address buffered in Buffer Address FIFO0, only used in Buffer Addr FIFO Mode.

6.1.8.31 0x0094 CSIC DMA Stored Frame Counter Register (Default Value:0x0000_0000)

Offset: 0x0094			Register Name: CSIC_DMA_STORED_FRM_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	RO	0x0	CSIC_DMA_STORED_FRM_CNT Indicates value of stored frames counter. When the counter value reaches CSIC_DMA_STORED_FRM_THRESHOLD, the counter is cleared to 0. Only used in Buffer Addr FIFO Mode.

6.1.8.32 0x01F4 CSIC DMA Feature List Register(Default Value:0x0000_0000)

Offset: 0x01F4			Register Name: CSIC_FEATURE_REG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R	0x0	DMA0_EMBEDDED_LBC 0: No Embedded LBC 1: Embedded LBC
0	R	0x0	DMA0_EMBEDDED_FBC 0: No Embedded DMA 1: Embedded FBC

6.2 TV Decoder

6.2.1 Overview

The Television Decoder (TVD) is an interface that transforms Composite Video Broadcast Signal (CVBS) or component signal into YUV data.

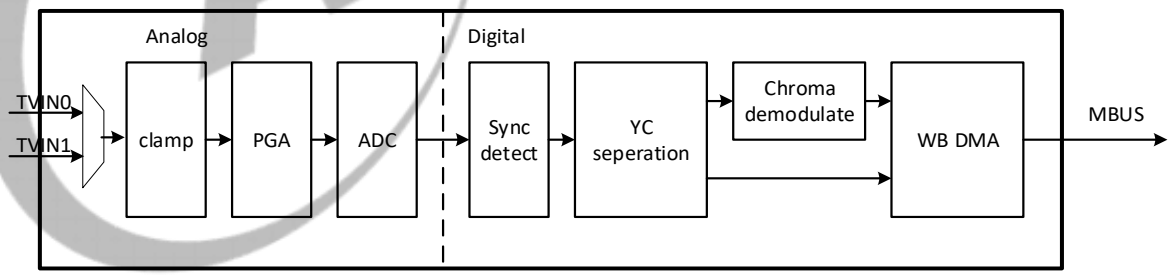
Features:

- 2-channel CVBS input and 1-channel CVBS decoder
- CVBS input, NTSC and PAL supported
- Supports YUV422, YUV420 format
- With 1 channel 3D comb filter
- Detection for signal locked and 625 lines
- Programmable brightness, contrast, saturation
- 10-bit video ADCs

6.2.2 Block Diagram

Figure 6-8 shows a block diagram of the TVD.

Figure 6-8 TVD Block Diagram



6.2.3 Functional Description

6.2.3.1 External Signals

Table 6-3 describes the external signals of TVD.

Table 6-3 TVD External Signals

Port Name	Description	Type
TVIN0	TV CVBS Input 0	AI
TVIN1	TV CVBS Input 1	AI
TVIN-VRP	TV CVBS ADC Positive Reference Voltage	P
TVIN-VRN	TV CVBS ADC Negative Reference Voltage	P
VCC-TVIN	TV CVBS ADC Power	P

6.2.4 Register List

Module Name	Base Address
TVD_TOP	0x05C00000
TVD0	0x05C01000

Register Name	Offset	Description
TVD_TOP		
TVD_TOP_MAP	0x0000	TVD TOP MAP Register
TVD_3D_CTL1	0x0008	TVD 3D DMA CONTROL Register1
TVD_3D_CTL2	0x000C	TVD 3D DMA CONTROL Register2
TVD_3D_CTL3	0x0010	TVD 3D DMA CONTROL Register3
TVD_3D_CTL4	0x0014	TVD 3D DMA CONTROL Register4
TVD_3D_CTL5	0x0018	TVD 3D DMA CONTROL Register5
TVD_TOP_CTL	0x0024+0x20*N (N=0–3)	TVD TOP CONTROL Register
TVD_ADC_CTL	0x0028+0x20*N (N=0–3)	TVD ADC CONTROL Register
TVD_ADC_CFG	0x002C+0x20*N (N=0–3)	TVD ADC CONFIGURATION Register
TVD0		
TVD_EN	0x0000	TVD MODULE CONTROL Register
TVD_MODE	0x0004	TVD MODE CONTROL Register
TVD_CLAMP_AGC1	0x0008	TVD CLAMP & AGC CONTROL Register1
TVD_CLAMP_AGC2	0x000C	TVD CLAMP & AGC CONTROL Register2
TVD_HLOCK1	0x0010	TVD HLOCK CONTROL Register1
TVD_HLOCK2	0x0014	TVD HLOCK CONTROL Register2
TVD_HLOCK3	0x0018	TVD HLOCK CONTROL Register3
TVD_HLOCK4	0x001C	TVD HLOCK CONTROL Register4

Register Name	Offset	Description
TVD_HLOCK5	0x0020	TVD HLOCK CONTROL Register5
TVD_VLOCK1	0x0024	TVD VLOCK CONTROL Register1
TVD_VLOCK2	0x0028	TVD VLOCK CONTROL Register2
TVD_CLOCK1	0x0030	TVD CHROMA LOCK CONTROL Register1
TVD_CLOCK2	0x0034	TVD CHROMA LOCK CONTROL Register2
TVD_YC_SEP1	0x0040	TVD YC SEPERATION CONROL Register1
TVD_YC_SEP2	0x0044	TVD YC SEPERATION CONROL Register2
TVD_ENHANCE1	0x0050	TVD ENHANCEMENT CONTROL Register1
TVD_ENHANCE2	0x0054	TVD ENHANCEMENT CONTROL Register2
TVD_ENHANCE3	0x0058	TVD ENHANCEMENT CONTROL Register3
TVD_WB1	0x0060	TVD WB DMA CONTROL Register1
TVD_WB2	0x0064	TVD WB DMA CONTROL Register2
TVD_WB3	0x0068	TVD WB DMA CONTROL Register3
TVD_WB4	0x006C	TVD WB DMA CONTROL Register4
TVD_IRQ_CTL	0x0080	TVD DMA Interrupt Control Register
TVD_IRQ_STATUS	0x0090	TVD DMA Interrupt Status Register
TVD_DEBUG1	0x0100	TVD DEBUG CONTROL Register1
TVD_STATUS1	0x0180	TVD DEBUG STATUS Register1
TVD_STATUS2	0x0184	TVD DEBUG STATUS Register2
TVD_STATUS3	0x0188	TVD DEBUG STATUS Register3
TVD_STATUS4	0x018C	TVD DEBUG STATUS Register4
TVD_STATUS5	0x0190	TVD DEBUG STATUS Register5
TVD_STATUS6	0x0194	TVD DEBUG STATUS Register6

6.2.5 Register Description

6.2.5.1 0x0000 TVD TOP MAP Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: TVD_TOP_MAP
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R/W	0x0	TVIN_SEL TVIN Select 0:TVIN0 1:TVIN1
3:2	/	/	/
1:0	R/W	0x0	TVD_ADC_MAP TVD ADC Map 01: CVBS_MODE Others: Reserved

6.2.5.2 0x0008 TVD 3D DMA CONTROL Register1 (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: TVD_3D_CTL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5:4	R/W	0x0	COMB_3D_SEL Comb 3D Select 00: TVD0 Others: Reserved
3:2	/	/	/
1	R/W	0x0	COMB_3D_EN Comb 3D Enable 0: Disable 1: Enable
0	R/W	0x0	TVD_EN_3D_DMA TVD Enable 3D DMA 0: Disable 1: Enable Set 0x1 when enable 3D comb filter.

6.2.5.3 0x000C TVD 3D DMA CONTROL Register2 (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: TVD_3D_CTL2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DRAM_TRIG DRAM Trigger

6.2.5.4 0x0010 TVD 3D DMA CONTROL Register3 (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: TVD_3D_CTL3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	COMB_3D_ADDR0 Comb 3D Address0

6.2.5.5 0x0014 TVD 3D DMA CONTROL Register4 (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: TVD_3D_CTL4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	COMB_3D_ADDR1 Comb 3D Address1

6.2.5.6 0x0018 TVD 3D DMA CONTROL Register5 (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: TVD_3D_CTL5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	COMB_3D_SIZE Comb 3D Size

6.2.5.7 0x0024+0x20*N(N=0~3) TVD TOP CONTROL Register (Default Value: 0x0000_0000)

Offset: 0x0024+0x20*N(N=0~3)			Register Name: TVD_TOP_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	LPF_DIG_SEL Low Pass Filter Digital Select 0: 6M 1: 8M
23:5	/	/	/
4	R/W	0x0	LPF_DIG_EN Low Pass Filter Digital Enable 0: Disable 1: Enable
3:0	/	/	/

6.2.5.8 0x0028+0x20*N(N=0~3) TVD ADC CONTROL Register (Default Value: 0x0000_0000)

Offset: 0x0028+0x20*N(N=0~3)			Register Name: TVD_ADC_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4:3	R/W	0x0	LPF_SEL Low Pass Filter Select 00: 11M 01: 16M
2	R/W	0x0	LPF_EN Low Pass Filter Enable 0: Disable LPF circuit 1: Enable LPF circuit
1	R/W	0x0	AFE_EN AFE Enable 0: Disable AFE circuit 1: Enable AFE circuit
0	R/W	0x0	ADC_EN ADC Enable 0: Disable ADC circuit 1: Enable ADC circuit

6.2.5.9 0x002C+0x20*N(N=0~3) TVD ADC CONFIGURATION Register (Default Value: 0x0000_0000)

Offset: 0x002C+0x20*N(N=0~3)			Register Name: TVD_ADC_CFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	ADC_TEST ADC Test Mode Configuration 0: Normal mode 1: For ADC test
30:29	/	/	/
28	R/W	0x0	DATA_DLY Data Delay Configuration 0: No delay 1: Delay ADC output data for half circle
27:19	/	/	/
18:16	R/W	0x0	CLP_STEP CLAMP Step Configuration DC level size step for up and down.
15:14	R/W	0x0	STAGE8_IBIAS Stage8 Ibias Configuration
13:12	R/W	0x0	STAGE7_IBIAS Stage7 Ibias Configuration
11:10	R/W	0x0	STAGE6_IBIAS Stage6 Ibias Configuration
9:8	R/W	0x0	STAGE5_IBIAS Stage5 Ibias Configuration
7:6	R/W	0x0	STAGE4_IBIAS Stage4 Ibias Configuration
5:4	R/W	0x0	STAGE3_IBIAS Stage3 Ibias Configuration
3:2	R/W	0x0	STAGE2_IBIAS Stage2 Ibias Configuration
1:0	R/W	0x0	STAGE1_IBIAS Stage1 Ibias Configuration

6.2.5.10 0x0000 TVD MODULE CONTROL Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: TVD_EN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26	R/W	0x0	EN_LOCK_DISABLE_WB2 Enable Lock Disable WB2
25	R/W	0x0	EN_LOCK_DISABLE_WB1 Enable Lock Disable WB1
24:16	/	/	/
15	R/W	0x0	CLR_RSMP_FIFO Clear Resample FIFO 0: Release 1: Clear Set 0x1 then 0x0 to reset resample FIFO.
14:1	/	/	/
0	R/W	0x0	TVD_EN_CH TVD Enable CH 0: Disable 1: Enable

6.2.5.11 0x0004 TVD MODE CONTROL Register (Default Value: 0x0000_0020)

Offset: 0x0004			Register Name: TVD_MODE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	BLUE_MODE_COLOR Blue Mode Color 0: Blue 1: Black
7:6	/	/	/
5:4	R/W	0x2	BLUE_DISPLAY_MODE Blue Display Mode 00 : Disabled 01 : Enabled 10 : Auto 11 : Reserved
3	/	/	/
2	R/W	0x0	PROGRESSIVE_MODE Progressive Mode 0: Interlace mode 1: Progressive mode
1	R/W	0x0	SVIDEO_MODE Svideo Mode 0 : CVBS 1 : S-Video
0	R/W	0x0	YPBPR_MODE Ypbpr Mode 0 : Disable the component input 1 : Enable the component input

6.2.5.12 0x0008 TVD CLAMP & AGC CONTROL Register1 (Default Value: 0xA001_DD02)

Offset: 0x0008			Register Name: TVD_CLAMP_AGC1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0xA0	CAGC_TARGET Cagc Target These bits set the chroma AGC target
23:17	/	/	/
16	R/W	0x1	CAGC_EN Cagc Enable 0 : OFF 1 : ON
15:8	R/W	0xDD	AGC_TARGET Auto Gain Control Target When AGC_EN = 1 , the AGC_TARGET is used to directly digital AGC circuit. When AGC_EN = 0 , the AGC_TARGET is used to directly drive the analog PGA. (64 represents 1x, 32 represents 0.5x).
7:2	/	/	/
1	R/W	0x1	AGC_FREQUENCE Auto Gain Control Freqence 0 : AGC gain update once per line 1 : AGC gain update once per frame
0	R/W	0x0	AGC_EN Auto Gain Control Enable 0 : AGC disable 1 : AGC enable

6.2.5.13 0x000C TVD CLAMP & AGC CONTROL Register2 (Default Value: 0x8682_6440)

Offset: 0x000C			Register Name: TVD_CLAMP_AGC2
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	BLACK_LVL_CLP Black Level Clamp 0: subtraction 0 1: subtraction 16
30:29	/	/	/
28:16	R/W	0x682	AGC_GATE_BEGIN AGC Gate Begin Count from hsync to the next line AGC gate
15:8	R/W	0x64	AGC_BACKPORCH_DLY AGC Backporch Delay Count from sync tip to back porch gate
7	/	/	/
6:0	R/W	0x40	AGC_GATE_WIDTH AGC Gate Width

6.2.5.14 0x0010 TVD HLOCK CONTROL Register1 (Default Value: 0x2000_0000)

Offset: 0x0010			Register Name: TVD_HLOCK1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x20000000	H_SAMPLE_STEP H Sample Step H_SAMPLE_STEP = Fout/Fin X 2^30

6.2.5.15 0x0014 TVD HLOCK CONTROL Register2 (Default Value: 0x4ED6_0000)

Offset: 0x0014			Register Name: TVD_HLOCK2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x4E	HS_FILTER_GATE_END_TIME HSYNC Filter Gate End Time These bits specify the end of the horizontal-blank-interval window. Default/Hex = 78
23:16	R/W	0xD6	HS_FILTER_GATE_START_TIME HSYNC Filter Gate Start Time These bits specify the beginning of the horizontal-blank-interval window. Default/Hex = -42
15:4	/	/	/
3:0	R/W	0x0	HTOL Horizontal Total Pixels Per Line 0: 858 1: 864 2~7: Reserved

6.2.5.16 0x0018 TVD HLOCK CONTROL Register3 (Default Value: 0x0FE9_502D)

Offset: 0x0018			Register Name: TVD_HLOCK3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0F	HS_TIP_DET_WIN_END_TIME HSYNC Tip Detect Window End Time
23:16	R/W	0xE9	HS_TIP_DET_WIN_START_TIME HSYNC Tip Detect Window Start Time
15:8	R/W	0x50	HS_RISING_DET_WIN_END_TIME HSYNC Rising Detect Window End Time
7:0	R/W	0x2D	HS_RISING_DETECT_WINDOW_START_TIME HSYNC Rising Detect Window Start Time

6.2.5.17 0x001C TVD HLOCK CONTROL Register4 (Default Value: 0x3E3E_8000)

Offset: 0x001C			Register Name: TVD_HLOCK4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x3E	HS_FINE_TO_COARSE_OFFSET HSYNC Fine To Coarse Offset
23:16	R/W	0x3E	HS_RISING_TIME_FOR_FINE_DET HSYNC Rising Time For Fine Detect
15:8	R/W	0x80	HS_DET_WIN_END_TIME_FOR_CORASE_DET HSYNC Detect Window End Time For Corase Detect
7:0	R/W	0x00	HS_DET_WIN_START_TIME_FOR_COARSE_DET HSYNC Detect Window Start Time For Coarse Detect

6.2.5.18 0x0020 TVD HLOCK CONTROL Register5 (Default Value: 0x4E22_5082)

Offset: 0x0020			Register Name: TVD_HLOCK5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x4E	BACKPORCH_DET_WIN_END_TIME Backporch Detect Window End Time
23:16	R/W	0x22	BACKPORCH_DET_WIN_START_TIME Backporch Detect Window Start Time
15:8	R/W	0x50	HACT_WIDTH Hactive Width
7:0	R/W	0x82	HACT_START Hactive Start

6.2.5.19 0x0024 TVD VLOCK CONTROL Register1 (Default Value: 0x0061_0220)

Offset: 0x0024			Register Name: TVD_VLOCK1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:16	R/W	0x61	VACT_HEIGHT Vactive Height
15	/	/	/
14:4	R/W	0x22	VACTIVE_START VACT START
3	/	/	/
2:0	R/W	0x0	VTOL Vertical Total Line Per Frame 0 : 525 line 1 : 625 line

6.2.5.20 0x0028 TVD VLOCK CONTROL Register2 (Default Value: 0x000E_0070)

Offset: 0x0028			Register Name: TVD_VLOCK2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0xE	HS_DET_DISABLE_END_LINE Hsync Detector Disable End Line
15:7	/	/	/
6:0	R/W	0x70	HS_DET_DISABLE_START_LINE Hsync Dectector Disable Start Line

6.2.5.21 0x0030 TVD CHROMA LOCK CONTROL Register1 (Default Value: 0x0046_3201)

Offset: 0x0030			Register Name: TVD_CLOCK1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x0	COLOR_STD_NTSC Color Standard Ntsc 0: NTSC358 1: NTSC443 Only valid when COLOR_STD set as NTSC
27:26	R/W	0x0	CHROMA_LPF CHROMA Low Pass Filter 00: Narrow 01: Middle 10: Wide 11: Reserved
25	/	/	/
24	R/W	0x0	WIDE_BURST_GATE Wide Burst_Gate 0: Narrow burst gate 1: Wide burst gate
23:16	R/W	0x46	BURST_GATE_END_TIME Burst Gate End Time
15:8	R/W	0x32	BURST_GATE_START_TIME Burst Gate Start Time
7:4	/	/	/
3:1	R/W	0x0	COLOR_STD COLOR Standard 000: NTSC 001: PAL (I,B,G,H,D,N) 010: PAL (M) 011: PAL (CN) 100: SECAM
0	R/W	0x1	COLOR_KILLER_EN Color Killer Enable 1: Disable color when chroma unlock

6.2.5.22 0x0034 TVD CHROMA LOCK CONTROL Register2 (Default Value: 0x21F0_7C1F)

Offset: 0x0034			Register Name: TVD_CLOCK2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x21F07C1F	C_SAMPLE_STEP C Sample Step C_SAMPLE_STEP = Fsc/Fin X 2^30

6.2.5.23 0x0040 TVD YC SEPERATION CONROL Register1 (Default Value: 0x0000_4209)

Offset: 0x0040			Register Name: TVD_YC_SEP1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	CHROMA_CORING_EN Chroma Coring Enable
28:26	R/W	0x0	3D_COMB_FACTOR 3D Comb Factor
25:23	R/W	0x0	2D_COMB_FACTOR 2D Comb Factor
22:20	R/W	0x0	NOTCH_FACTOR Notch Factor
19:17	/	/	/
16	R/W	0x0	COMB_FILTER_BUF_CLR Comb Filter Buffer Clear 0: Not clear 1: Clear
15:10	R/W	0x10	PAL_CHROMA_LVL PAL Chroma Level Chroma level threshold for chroma comb filter select
9	R/W	0x1	CHROMA_BANDPASS_FILTER_EN Chroma Bandpass Filter Enable 0: Disable 1: Enable
8	R/W	0x0	SECAM_NOTCH_WIDE Notch bandwidth 0 : Narrow 1 : Wide

7:4	R/W	0x0	2D_COMB_FILTER_MODE 2D Comb Filter Mode For NTSC: 0000: 2D comb 0001~0010: Reserved 0011: 1D comb 0100~1000: Reserved For PAL: 0000:2D comb filter1 0001: 1D comb filter1 0010: 2D comb filter2 0011: 1D comb filter2 0100: 1D comb filter3 0101: Reserved 0110: 2D comb filter3 0111~1000:Reserved
3	R/W	0x1	3D_COMB_FILTER_DIS 3D Comb Filter Disable 0: Enable 3D comb filter 1: Disable 3D comb filter
2:0	R/W	0x1	3D_COMB_FILTER_MODE 3D Comb_Filter Mode 000: 2D mode 001: 3D YC separation mode1 010~011: reserved 0100: 3D YC separation mode2

6.2.5.24 0x0044 TVD YC SEPERATION CONROL Register2 (Default Value: 0xFF64_40AF)

Offset: 0x0044			Register Name: TVD_YC_SEP2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x3	V_NOISE_FACTOR Vertical Noise Factor
29:28	R/W	0x3	BURST_NOISE_FACTOR Burst Noise Factor
27:26	R/W	0x3	CHROMA_NOISE_FACTOR Chroma Noise Factor
25:24	R/W	0x3	LUMA_NOISE_FACTOR Luma Noise Factor
23:17	R/W	0x32	NOISE_THRESHOLD Noise Threshold
16	R/W	0x0	NOISE_DET_EN Noise Detect Enable
15:9	R/W	0x20	MOTION_DET_NOISE_THRESHOLD Motion Detect Noise Threshold
8	R/W	0x0	MOTION_DET_NOISE_DET_EN Motion Detect Noise Detect Enable
7:6	R/W	0x2	CHROMA_V_FILTER_GAIN Chroma Vertical Filter Gain
5:4	R/W	0x2	LUMA_V_FILTER_GAIN Luma Vertical Filter Gain
3:2	R/W	0x3	H_CHROMA_FILTER_GAIN Horizontal Chroma Filter Gain
1:0	R/W	0x3	H_LUMA_FILTER_GAIN Horizontal Luma Filter Gain

6.2.5.25 0x0050 TVD ENHANCEMENT CONTROL Register1 (Default Value: 0x1420_8000)

Offset: 0x0050			Register Name: TVD_ENHANCE1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:28	R/W	0x1	SHARP_COEF2 Sharp Coef2
27:25	R/W	0x2	SHARP_COEF1 Sharp Coef1 Ysharp = Y + YH *(SHARP_COEF1/ SHARP_COEF2)
24	R/W	0x0	SHARP_EN Sharp Enable 0: Disable 1: Enable
23:16	R/W	0x20	BRIGHT_OFFSET Bright Offset Set 0x00, brightness offset is -32; Set 0x20, brightness offset is 0. Set 0xFF, brightness offset is max.
15:8	R/W	0x80	CONTRAST_GAIN Contrast Gain Set 0x00, contrast gain is min ; Set 0x80, contrast gain is 1. Set 0xFF, contrast gain is max.
7:4	/	/	/

3:0	R/W	0x0	YC_DLY YC Delay 0000: Y and C no delay 0001: Y delay 1 cycle to C 0010: Y delay 2 cycle to C 0011: Y delay 3 cycle to C 0100: Y delay 4 cycle to C 0101: Y delay 5 cycle to C 0110: Y delay 6 cycle to C 0111: Y delay 7 cycle to C 1000: Reserved 1001: Reserved 1010: Reserved 1011: C delay 5 cycle to Y 1100: C delay 4 cycle to Y 1101: C delay 3 cycle to Y 1110: C delay 2 cycle to Y 1111: C delay 1 cycle to Y

6.2.5.26 0x0054 TVD ENHANCEMENT CONTROL Register2 (Default Value: 0x0000_0680)

Offset: 0x0054			Register Name: TVD_ENHANCE2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:9	R/W	0x3	CHROMA_ENHANCE_STRENGTH Chroma Enhance Strength 00: Mild 01: Low 10: Middle 11: High
8	R/W	0x0	CHROMA_ENHANCE_EN Chroma Enhance Enable 0: Disable 1: Enable
7:0	R/W	0x80	SATURATION_GAIN Saturation Gain Set 0x00, saturation gain is min ; Set 0x80, saturation gain is 1. Set 0xFF, saturation gain is max.

6.2.5.27 0x0058 TVD ENHANCEMENT CONTROL Register3 (Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: TVD_ENHANCE3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x0	CB_CR_GAIN_EN Cb Cr Gain Enable
27:16	R/W	0x0	CR_GAIN Cr Gain
15:12	/	/	/
11:0	R/W	0x00	CB_GAIN Cb Gain

6.2.5.28 0x0060 TVD WB DMA CONTROL Register1 (Default Value: 0x02D0_0020)

Offset: 0x0060			Register Name: TVD_WB1
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	UV_SEQ UV Sequence 0: UVUV 1: VUVU
30:29	/	/	/
28	R/W	0x0	YUV420_FILTER_EN YUV420 Filter Enable 0: disable YUV420 WB data from YUV422 without chroma filter 1: enable YUV420 WB data from YUV422 with chroma filter
27:16	R/W	0x2D0	HACT_STRIDE Hactive Stride Horizontal active line stride
15:9	/	/	/
8	R/W	0x0	WB_ADDR_VALID WB Address Valid 0: Invalid 1: Valid
7	/	/	/
6	R/W	0x0	FLIP_FIELD Flip Field This bit flips even/odd fields
5	R/W	0x1	WB_FRAME_MODE WB Frame Mode 0: Odd field or even field (decided by bit2) 1: Frame
4	R/W	0x0	WB_MB_MODE WB MB Mode 0: Planar mode 1: Mb mode
3	R/W	0x0	HYSCALE_EN Hyscale_Enable
2	R/W	0x0	FIELD_SEL Field_Select 0: field 0 only 1: filed 1 only

1	R/W	0x0	WB_FMT WB Format 0: YUV420 1: YUV422
0	R/W	0x0	WB_EN WB Enable 0: Disable 1: Enable

6.2.5.29 0x0064 TVD WB DMA CONTROL Register2 (Default Value: 0x00F0_02D0)

Offset: 0x0064			Register Name: TVD_WB2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:16	R/W	0xF0	VACT_NUM Vertical active line number
15:12	/	/	/
11:0	R/W	0x2D0	HACT_NUM Horizontal active pixel number

6.2.5.30 0x0068 TVD WB DMA CONTROL Register3 (Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: TVD_WB3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	CH1_Y_ADDR Ch1 Y Address

6.2.5.31 0x006C TVD WB DMA CONTROL Register4 (Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: TVD_WB4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	CH1_C_ADDR Ch1 C Address

6.2.5.32 0x0080 TVD DMA Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: TVD_IRQ_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	FIFO_3D_TX_O_EN FIFO 3D TX Overflow Enable 0: IRQ disable 1: IRQ enable
30	R/W	0x0	FIFO_3D_TX_U_EN FIFO 3D TX Underflow Enable 0: IRQ disable 1: IRQ enable
29	R/W	0x0	FIFO_3D_RX_O_EN FIFO 3D RX Overflow ENable 0: IRQ disable 1: IRQ enable
28	R/W	0x0	FIFO_3D_RX_U_EN FIFO 3D RX Underflow Enable 0: IRQ disable 1: IRQ enable
27:25	/	/	/
24	R/W	0x0	FRAME_END_EN Frame End Enable 0: IRQ disable 1: IRQ enable
23:9	/	/	/
8	R/W	0x0	FIFO_Y_U_EN FIFO Y Underflow Enable 0: IRQ disable 1: IRQ enable
7	R/W	0x0	FIFO_PB_U_EN FIFO PB Underflow ENable 0: IRQ disable 1: IRQ enable
6	R/W	0x0	FIFO_PR_U_EN FIFO PR Underflow Enable 0: IRQ disable 1: IRQ enable

5	R/W	0x0	FIFO_Y_O_EN FIFO Y Overflow Enable 0: IRQ disable 1: IRQ enable
4	R/W	0x0	FIFO_PB_O_EN FIFO PB Overflow Enable 0: IRQ disable 1: IRQ enable
3	R/W	0x0	FIFO_PR_O_EN FIFO PR Overflow Enable 0: IRQ disable 1: IRQ enable
2	/	/	/
1	R/W	0x0	UNLOCK_EN Unlock Enable 0: IRQ disable 1: IRQ enable
0	R/W	0x0	LOCK_EN Lock Enable 0: IRQ disable 1: IRQ enable

6.2.5.33 0x0090 TVD DMA Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: TVD_IRQ_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	FIFO_3D_TX_O FIFO 3D TX Overflow 0: FIFO work normal 1: FIFO overflow Write 0x1 to clear this bit.
30	R/W	0x0	FIFO_3D_TX_U FIFO 3D TX Underflow 0: FIFO work normal 1: FIFO underflow Write 0x1 to clear this bit.
29	R/W	0x0	FIFO_3D_RX_O FIFO 3D RX Overflow 0: FIFO work normal 1: FIFO overflow Write 0x1 to clear this bit.
28	R/W	0x0	FIFO_3D_RX_U FIFO 3D RX Underflow 0: FIFO work normal 1: FIFO underflow Write 0x1 to clear this bit.
27:25	/	/	/
24	R/W	0x0	FRAME_END Frame End This bit is auto set every write back frame. Set 0x1 to clear this bit.
23:17	/	/	/
16	R/W	0x0	WB_ADDR_CHANGE_ERR WB Address Change_Error Write back address change error
15:9	/	/	/
8	R/W	0x0	FIFO_Y_U FIFO Y Underflow 0: FIFO work normal 1: FIFO underflow Write 0x1 to clear this bit.

7	R/W	0x0	FIFO_C_U FIFO C Underflow 0: FIFO work normal 1: FIFO underflow Write 0x1 to clear this bit.
6	/	/	/
5	R/W	0x0	FIFO_Y_O FIFO Y Overflow 0: FIFO work normal 1: FIFO overflow Write 0x1 to clear this bit.
4	R/W	0x0	FIFO_C_O FIFO C Overflow 0: FIFO work normal 1: FIFO overflow Write 0x1 to clear this bit.
3:2	/	/	/
1	R/W	0x0	UNLOCK Unlock 0: TVD status no change 1: TVD status change from lock to unlock
0	R/W	0x0	LOCK Lock 0: TVD status no change 1: TVD status change from unlock to lock

6.2.5.34 0x0100 TVD DEBUG CONTROL Register1 (Default Value: 0x0010_0000)

Offset: 0x0100			Register Name: TVD_DEBUG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	R/W	0x0	CLAMP_UPDN_CYCLES Clamp Updn Cycles
24	R/W	0x0	CLAMP_DN_START Clamp Dn Start Write 0x1 to make clamp up, clamp up value is determine by CLAMP_UPDN_CYCLES. Note that this bit is only valid when CLAMP_MODE is set as 0x1.
23	R/W	0x0	CLAMP_UP_START Clamp Up Start Write 0x1 to make clamp up, clamp up value is determine by CLAMP_UPDN_CYCLES. Note that this bit is only valid when CLAMP_MODE is set as 0x1.
22	R/W	0x0	CLAMP_MODE Clamp Mode 0: Normal, auto clamp control 1: Debug mode, clamp control by register
21	R/W	0x0	AFE_GAIN_MODE Afe Gain Mode 0: Auto gain mode 1: Debug mode, AFE gain is determine by AFE_GAIN_VALUE
20	R/W	0x1	UNLOCK_RST_GAIN_EN Unlock Reset Gain Enable
19	R/W	0x0	TRUNCATION_RST_GAIN_EN Truncation Reset Gain Enable
18	R/W	0x0	TRUNCATION2_RST_GAIN_EN Truncation2 Reset Gain Enable
17	R/W	0x0	TVIN_LOCK_HIGH TVIN Lock High
16	R/W	0x0	TVIN_LOCK_DEBUG TVIN Lock Debug
15:8	R/W	0x0	AFE_GAIN_VALUE AFE Gain Value
7:0	/	/	/

6.2.5.35 0x0180 TVD DEBUG STATUS Register1 (Default Value: 0x0000_0020)

Offset: 0x0180			Register Name: TVD_STATUS1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R	0x0	CHROMA_MAGNITUDE_STATUS These bits contain the chroma magnitude.
15:8	R	0x0	AGC_DEGITAL_GAIN_STATUS These bits contain the digital AGC gain value.
7:0	R	0x20	AGC_ANALOG_GAIN_STATUS These bits contain the analog AGC gain value.

6.2.5.36 0x0184 TVD DEBUG STATUS Register2 (Default Value: 0x21F0_7C1F)

Offset: 0x0184			Register Name: TVD_STATUS2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x21f07c1f	CHROMA_SYNC_DTO_STATUS

6.2.5.37 0x0188 TVD DEBUG STATUS Register3 (Default Value: 0x2000_0000)

Offset: 0x0188			Register Name: TVD_STATUS3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:0	R	0x20000000	H_SYNC_DTO_STS Horizontal Sync Dto Status

6.2.5.38 0x018C TVD DEBUG STATUS Register4 (Default Value: 0x0000_0001)

Offset: 0x018C			Register Name: TVD_STATUS4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23	R	0x0	VCR_REW VCR Rewind Detected
22	R	0x0	VCR_FF VCR Fast-Forward Detected
21	R	0x0	VCR_TRICK VCR Trick-Mode Detected
20	R	0x0	VCR VCR Detected
19	R	0x0	NOISY Noisy Signal Detected. This bit is set when the detected noise value (status register 7Fh) is greater than the value programmed into the “noise_thresh” register (05h).
18	R	0x0	DET_625_LINE Detect 625 Line 0: 525 lines 1: 625 lines
17	R	0x0	SECAM_DET SECAM Colour Mode Detected
16	R	0x0	PAL_DET PAL Colour Mode Detected
15:11	/	/	/
10	R	0x0	VNON_STANDARD Vertical Frequency Non-Standard Input Signal Detected
9	R	0x0	HNON_STANDARD Horizontal Frequency Non-Standard Input Signal Detected
8	R	0x0	PROSCAN_DET Progressive Scan Detected
7:5	R	0x0	MACROVISION_COLOR_STRIPES_DET The Number Indicates The Number Of Color Stripe lines in each group
4	R	0x0	MACROVISION_VBI_PSEUDO_SYNC_PULSES_DET Macrovision Vbi Pseudo Sync Pulses Detect 0: Undetected 1: Detected

3	R	0x0	CHROMA_PLL_LOCKED_TO_COLOR_BURST Chroma Pll Locked To Color Burst 0: Unlock 1: Locked
2	R	0x0	V_LOCK Vertical Lock 0: Unlock 1: Locked
1	R	0x0	H_LINE_LOCK Horizontal line locked 0: Unlock 1: Locked
0	R	0x1	NO_SIG_DET No Signal Detected 0 : Signal Detected 1 :No Signal Detected

6.2.5.39 0x0190 TVD DEBUG STATUS Register5 (Default Value: 0x0000_0000)

Offset: 0x0190			Register Name: TVD_STATUS5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	R	0x0	BLK_LVL Blank Level
21:12	R	0x0	SYNC_LVL Sync Level
11	R/W	0x0	ADC_DAT_SH ADC Data Show
10	/	/	/
9:0	R	0x0	ADC_DAT_VAL ADC Data Value

6.2.5.40 0x0194 TVD DEBUG STATUS Register6 (Default Value: 0x0000_0000)

Offset: 0x0194			Register Name: TVD_STATUS6
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10	R/W	0x0	MASK_UNKNOWN Mask Unknown
9	R/W	0x0	MASK_SECAM Mask Secam
8	R/W	0x0	MASK_NTSC443 Mask NTSC443
7	R/W	0x0	MASK_PAL60 Mask PAL60
6	R/W	0x0	MASK_PALCN Mask Palcn
5	R/W	0x0	MASK_PALM Mask Palm
4	R/W	0x0	AUTO_DET_EN Auto Detect Enable 0: Disable 1: Enable
3:1	R	0x0	TV_STD TV Standard 001: V525_NTSC 010: V625_PAL 011: V525_PALM 100: V625_PALN 101: V525_PAL60 110: V525_NTSC443 111: V625_SECAM
0	R	0x0	AUTO_DET_FINISH Auto Detect Finish

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7.1 SDRAM Controller (DRAMC)

The DRAMC is embedded with 128 MB DDR3.

The DRAMC has the following features:

- Embedded with 128 MB DDR3
- Supports clock frequency up to 800 MHz

7.2 SD/MMC Host Controller (SMHC)

7.2.1 Overview

The SMHC controls the read/write operations on the secure digital (SD) cards, multimedia cards (MMC), and various extended devices that is based on the secure digital input/output (SDIO) protocol. The processor provides three SMHC interfaces for controlling the SD cards, MMCs, and SDIO devices.

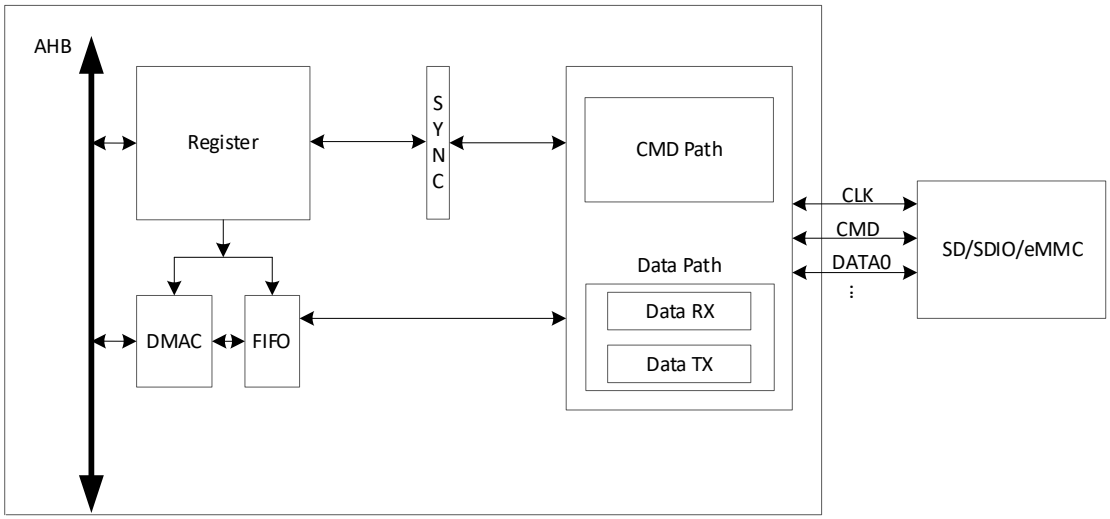
The SMHC has the following features:

- Supports Command Completion signals and interrupts to host processor, and Command Completion signal disable feature
- The SMHC0 controls the devices that comply with the Secure Digital Memory (SD mem-version 3.0)
- The SMHC1 controls the device that complies with the protocol Secure Digital I/O (SDIO-version 3.0)
- The SMHC2 controls the device that complies with the Multimedia Card (eMMC-version 5.0)
- Maximum performance:
  - SDR mode: 150 MHz@1.8 V IO pad
  - DDR mode: 50 MHz@1.8 V IO pad
  - DDR mode: 50 MHz@3.3 V IO pad
- Supports 1-bit or 4-bit data width
- Hardware CRC generation and error detection
- Programmable baud rate
- Supports SDIO interrupt in 1-bit and 4-bit modes
- Block size of 1 to 65535 bytes
- Descriptor-based internal DMA controller
- Internal 1 KB RXFIFO and 1 KB TXFIFO

7.2.2 Block Diagram

The following figure shows a block diagram of the SMHC.

Figure 7-1 SMHC Block Diagram



SMHC contains the following sub-blocks:

Table 7-1 SMHC Sub-blocks

Sub-block	Description
Register	Used to configure the control signal for reading or writing the SD/SDIO/eMMC.
DMAC	The DMA controller that controls the data transfer between the memory and SMHC.
FIFO	A buffer for the data stream between the memory and the SMHC asynchronous clock domain.
SYNC	Synchronizes the signals from the AHB clock domain to the SMHC clock domain.
CMD Path	Sends commands to or receives commands from the SD/SDIO/eMMC.
Data Path	Consists of Data TX and Data RX sub-modules. The Data TX sends data blocks and the CRC codes to the SD/SDIO/eMMC. The Data RX receives data blocks and the CRC codes from the SD/SDIO/eMMC.

7.2.3 Functional Description

7.2.3.1 External Signals

The following table describes the external signals of SMHC.

Table 7-2 SMHC External Signals

Port Name	Type	Description
SDC0-CMD	I/O, OD	Command Signal for SD Card
SDC0-CLK	O	Clock for SD Card
SDC0-D[3:0]	I/O	Data Input and Output for SD Card
SDC0-RST	O	Reset for SD Card
SDC1-CMD	I/O, OD	Command Signal for SDIO Wi-Fi
SDC1-CLK	O	Clock for SDIO Wi-Fi
SDC1-D[3:0]	I/O	Data Input and Output for SDIO Wi-Fi
SDC2-CMD	I/O, OD	Command Signal for eMMC
SDC2-CLK	O	Clock for eMMC
SDC2-D[3:0]	I/O	Data Input and Output for eMMC

7.2.3.2 Clock Sources

The SMHC0/1 has 4 different clock sources. The SMHC2 has 5 different clock sources. You can select one of them as the SMHC clock source. The following table describes the clock sources of the SMHC.

For clock setting, configurations, and gating information, refer to section 3.3 "CCU".

Table 7-3 SMHC0/1 Clock Sources

Clock Sources	Description
HOSC	24 MHz Crystal
PLL_PERI(1X)	Peripheral Clock, the default value is 600 MHz
PLL_PERI(2X)	Peripheral Clock, the default value is 1.2 GHz
PLL_AUDIO1(DIV2)	Audio clock, the default value is 1536 MHz

Table 7-4 SMHC2 Clock Sources

Clock Sources	Description
HOSC	24 MHz Crystal
PLL_PERI(1X)	Peripheral Clock, the default value is 600 MHz
PLL_PERI(2X)	Peripheral Clock, the default value is 1.2 GHz
PLL_PERI(800M)	Peripheral Clock, the default value is 800 MHz
PLL_AUDIO1(DIV2)	Audio clock, the default value is 1536 MHz

7.2.3.3 Timing Diagram

Refer to the following relative specifications:

- Physical Layer Specification Ver3.00 Final
- SDIO Specification Ver2.00
- Multimedia Cards (MMC – version 4.2)
- JEDEC Standard – JESD84-44, Embedded Multimedia Card (eMMC) Card Product Standard
- JEDEC Standard – JESD84-B45, Embedded Multimedia Card (eMMC) Electrical Standard (4.5 Device)
- JEDEC Standard – JESD84-B50, Embedded Multimedia Card (eMMC) Electrical Standard (5.0)

7.2.3.4 Data Path

The SMHC and SD/SDIO/eMMC contains the following interface buses: CLK, CMD, and DATA 1/4. During one clock cycle, the SMHC can transmit one bit command with one or two bits data in 1-ch DATA mode, or four or eight bits data in 4-ch DATA mode. The CMD is a bidirection channel for initializing the SD/SDIO/eMMC and transmitting commands. It can work in both the open-drain mode and push-pull mode. The DATA is also a bidirection channel. It works in the push-pull mode.

Reading Data from the SD/SDIO/eMMC

The register configures the signals for the read operation, and synchronize the signals to the SMHC clock domain. Then the Data RX reads data from the SD/SDIO/eMMC via the CLK/CMD/DATA interface buses and writes the data in the FIFO. After that, the DMAC transfers the data from the FIFO to the memory.

Writing Data to the SD/SDIO/eMMC

The register configures the signals for the write operation, and synchronize the signals to the SMHC clock domain. Then the DMAC reads data from the memory and writes the data to the FIFO. After that, the Data TX reads the data from the FIFO and writes the data to the SD/SDIO/eMMC via the CLK/CMD/DATA interface buses.

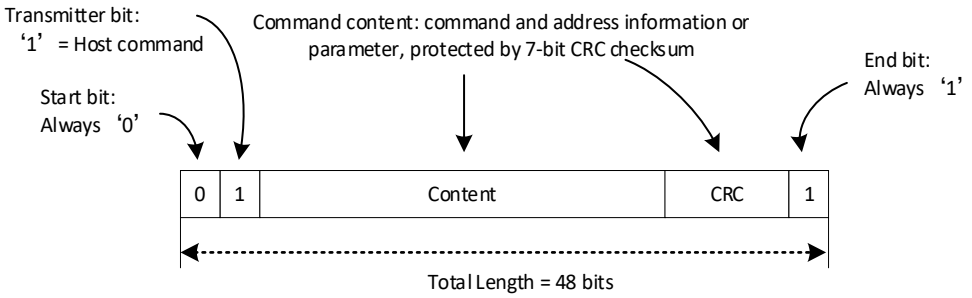
7.2.3.5 Package Format

Data transfer over the SD/eMMC bus is based on command and data bitstreams that are initiated by a start bit and terminated by a stop bit. There are three types of SD/eMMC packets: command token, response token, and data packet.

Command Tokens

The command token starts an operation. A command is sent from the host to a device. It is transferred serially on the CMD line. Command tokens have the following coding scheme:

Figure 7-2 Command Token Format



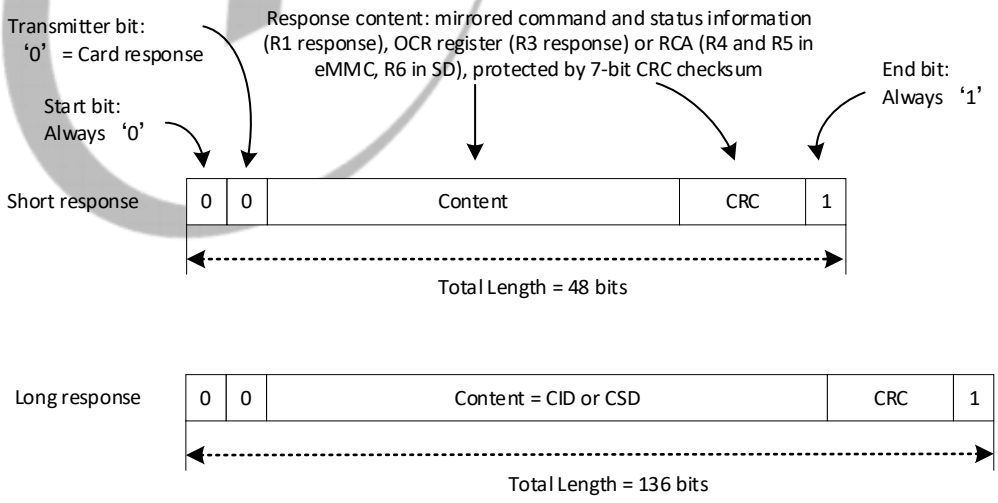
Each command token has 48 bits, preceded by a start bit ('0') and succeeded by an end bit ('1'). To detect transmission errors, each token is protected by CRC bits.

Response Tokens

After receiving a command, the card returns a 48-bit or 136-bit response based on the command type.

A response token is sent from the device to the host as an answer to a previously received command. It is transferred serially on the CMD line.

Figure 7-3 Response Token Format



Data Packets

Data can be transferred from the device to the host or vice versa. Data are transferred via the data lines.

NOTE

T113-S3 does not support the bus width of 8 bits.

Figure 7-4 Data Packet Format for SDR

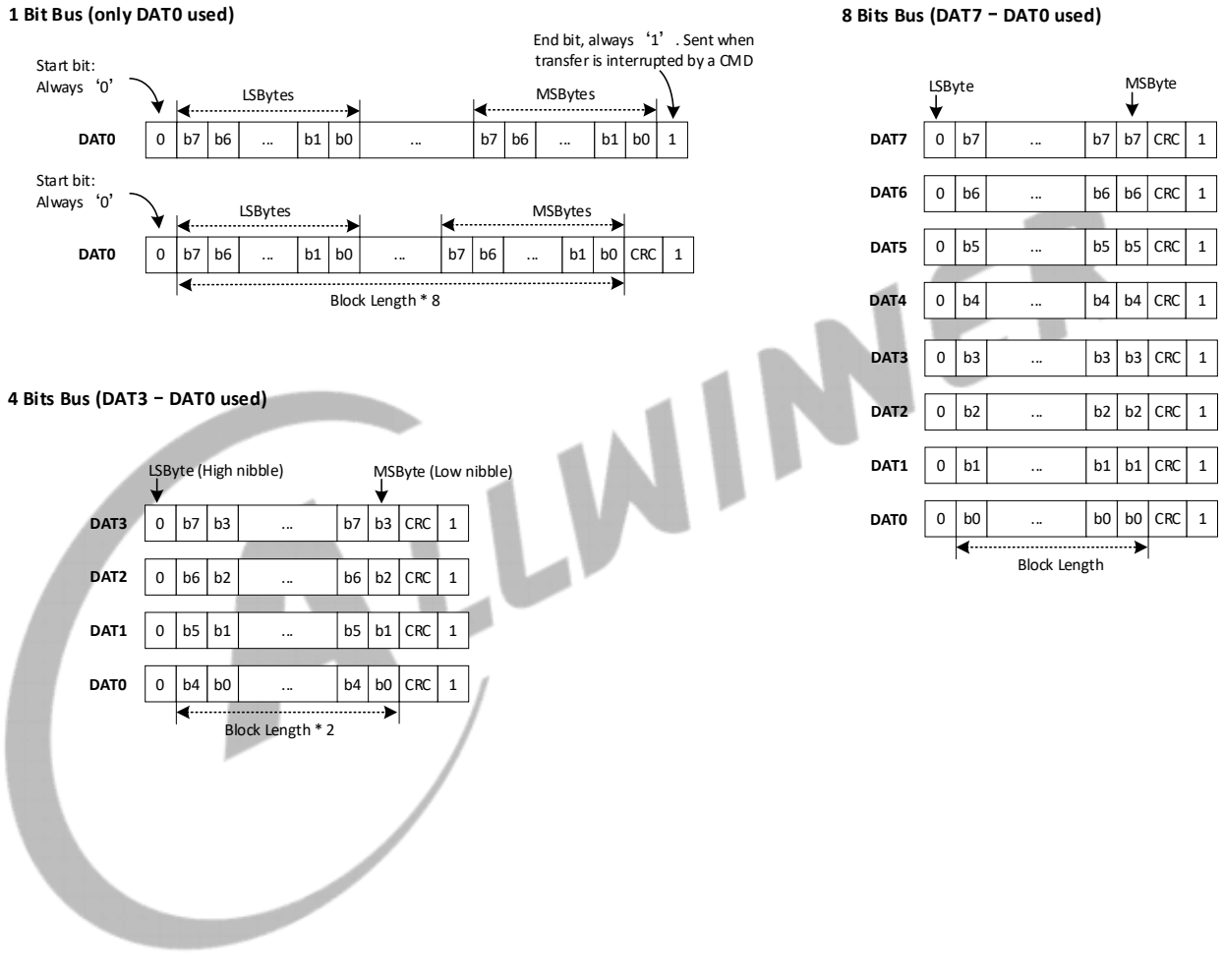
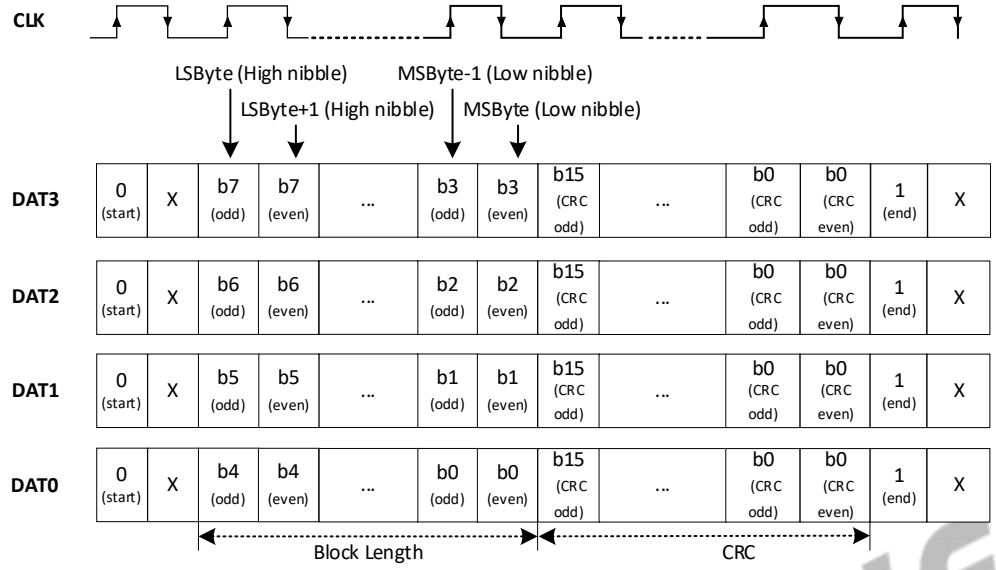
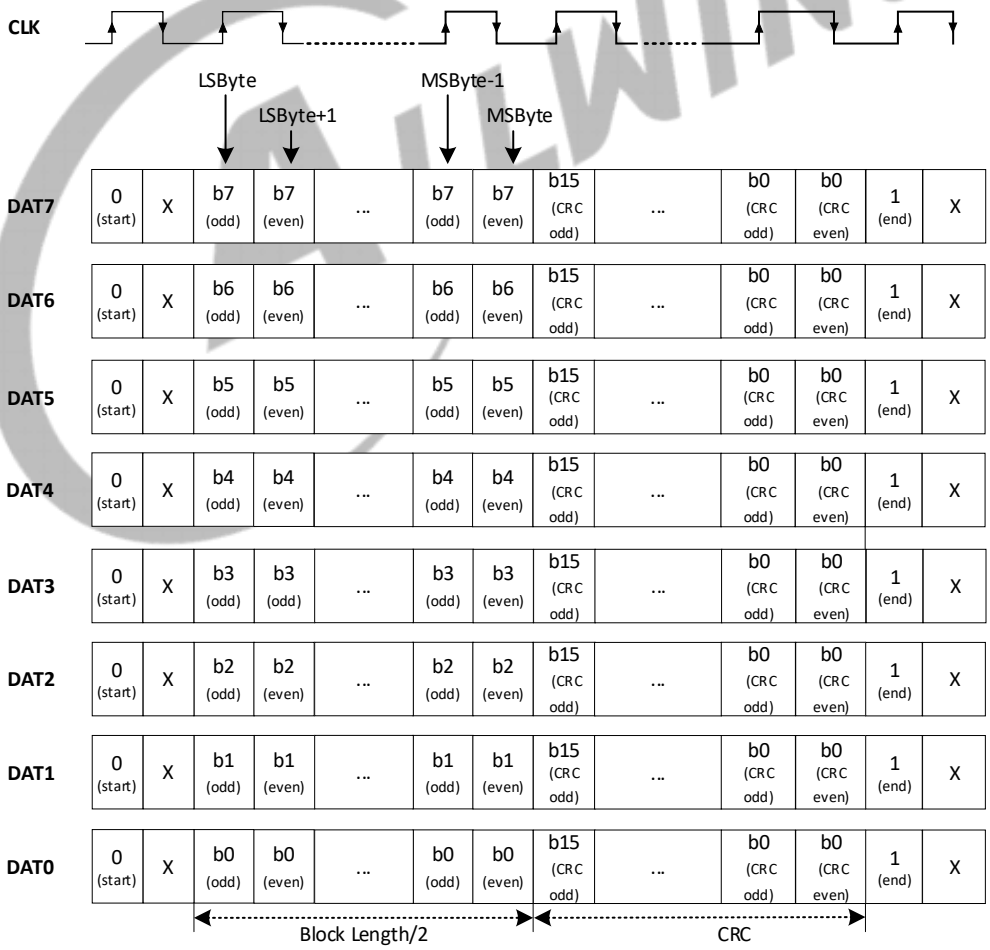


Figure 7-5 Data Packet Format for DDR

4 Bits Bus DDR (DAT3 – DAT0 used)



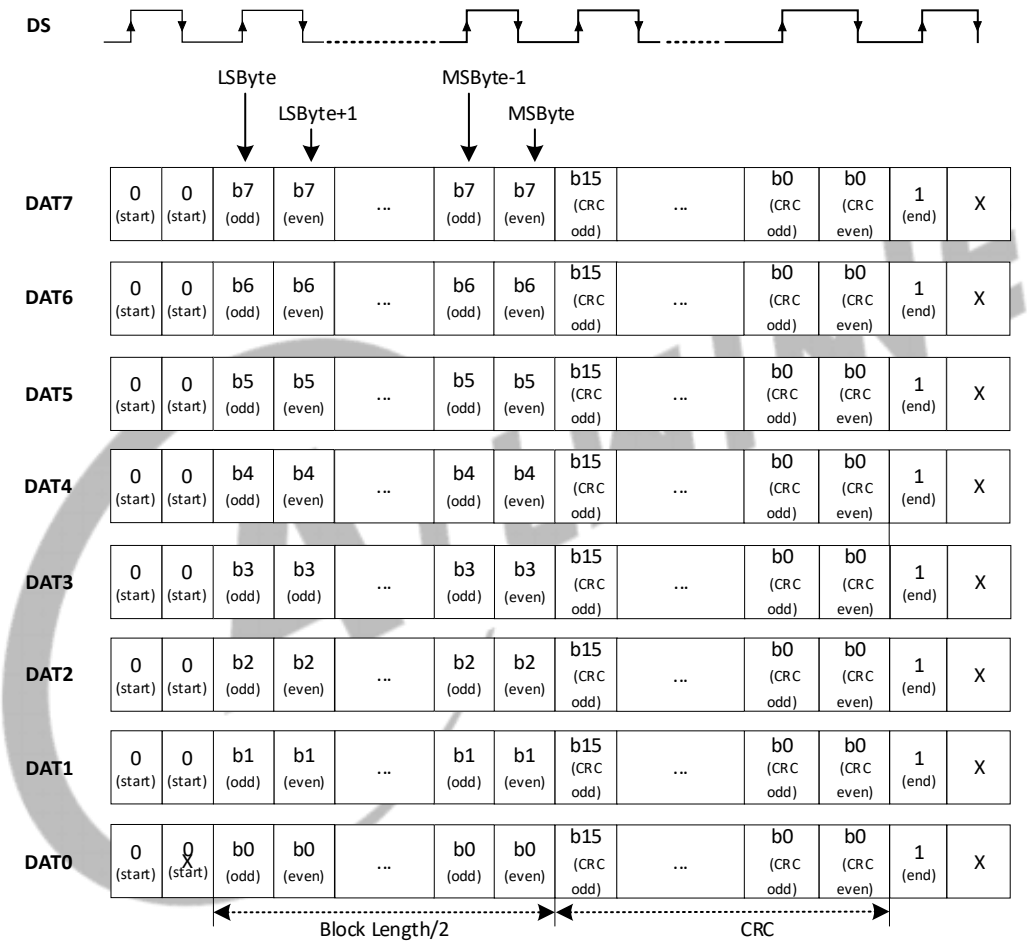
8 Bits Bus DDR (DAT7 – DAT0 used)



NOTE

- Bytes data are not interleaved but CRCs are interleaved.
- Start and end bits are only valid on the rising edge (“X” indicates “undefined”).

Figure 7-6 Data Packet Format for DDR in HS400 Mode



NOTE

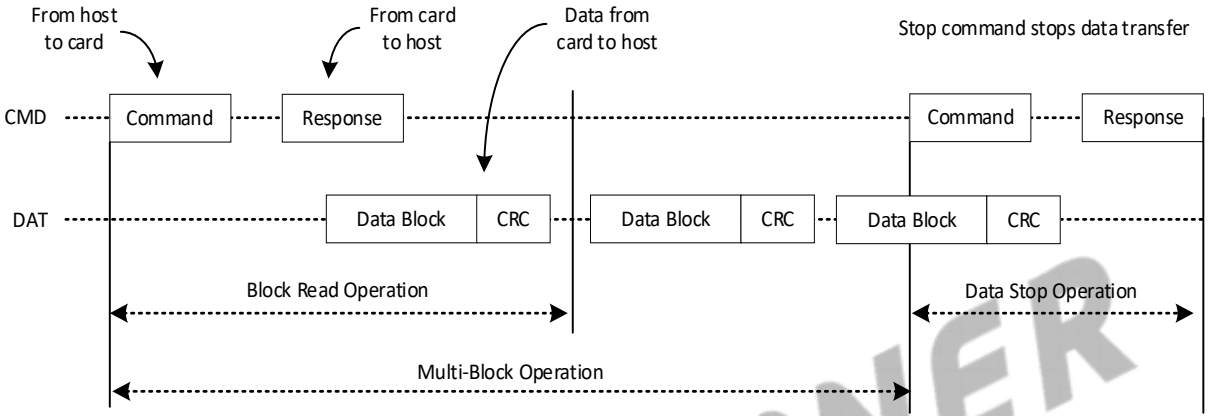
- Bytes data are not interleaved but CRCs are interleaved.
- Start bits are valid when Data Strobe is High and Low.
- End bits are only valid when Data Strobe is High (“X” indicates “undefined”).

7.2.3.6 Data Transfer

Data transfers to or from the SD/eMMC card are done in blocks. Single and multiple block operations are widely used during data transfer.

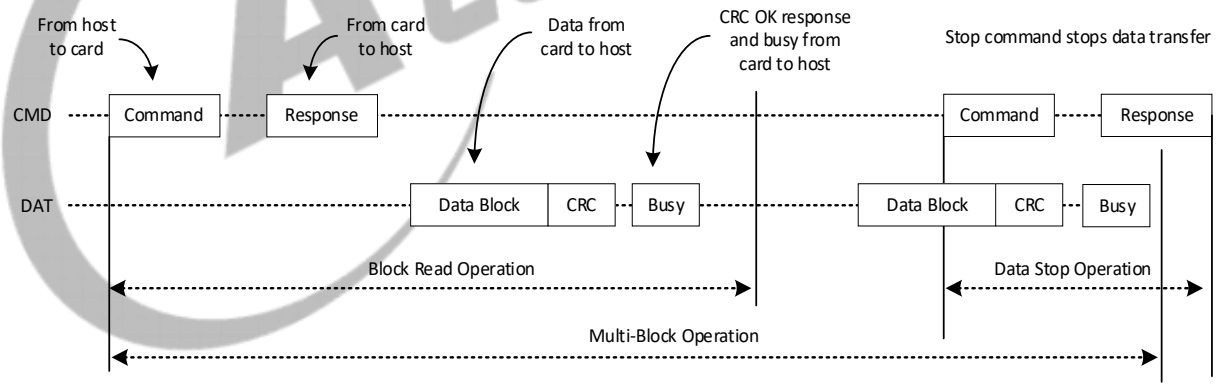
The following figure shows the single-block and multi-block read operation.

Figure 7-7 Single-Block and Multi-Block Read Operation



The following figure shows the single-block and multi-block write operation.

Figure 7-8 Single-Block and Multi-Block Read Operation



7.2.3.7 Bus Speed Modes

The following table shows the bus speed modes supported by SD 3.0.

Table 7-5 Speed Modes Supported by SD 3.0

Mode	I/O Voltage	Bus Width	Frequency	Throughput
SDR104	1.8 V	1, 4 bits	0 to 208 MHz	0 to 104 MB/s

Mode	I/O Voltage	Bus Width	Frequency	Throughput
SDR50	1.8 V	1, 4 bits	0 to 100MHz	0 to 50 MB/s
DDR50	1.8 V	1, 4 bits	0 to 50 MHz	0 to 50 MB/s
SDR25	1.8 V	1, 4 bits	0 to 50 MHz	0 to 25 MB/s
SDR12	1.8 V	1, 4 bits	0 to 25 MHz	0 to 12 MB/s
High Speed Mode (HS)	3.3 V	1, 4 bits	0 to 50 MHz	0 to 25 MB/s
Default Speed Mode (DS)	3.3 V	1, 4 bits	0 to 25 MHz	0 to 12 MB/s

The following table shows the bus speed modes supported by eMMC 5.0.

Table 7-6 Speed Modes Supported by eMMC 5.0

Mode	Data Rate	I/O Voltage	Bus Width	Frequency	Throughput
Backwards Compatibility with legacy MMC card	Single	3.3 V/1.8 V	1, 4 bits	0 to 26 MHz	0 to 26 MB/s
High Speed SDR	Single	3.3 V/1.8 V	1, 4 bits	0 to 52 MHz	0 to 52 MB/s
High Speed DDR	Dual	3.3 V/1.8 V	4 bits	0 to 52 MHz	0 to 104 MB/s
HS200	Single	1.8 V	4 bits	0 to 200 MHz	0 to 200 MB/s

7.2.3.8 Phase Offset of the Command and Data

You can configure the phase offset of the command and data by the **SMHC_DRV_DL** register.

SDR Mode

The following figure shows the phase offset of SDR command and data.

Figure 7-9 Phase Offset of Command and Data in SDR Mode

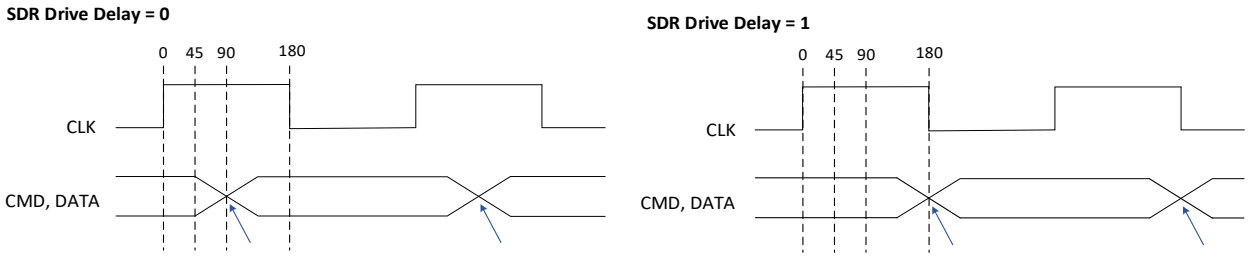


Table 7-7 Phase Offset of Command and Data in SDR Mode

Drive Delay	Command	Data
0	The command is updated in 90° clock position	The data is updated in 90° clock position
1	The command is updated in 180° clock position	The data is updated in 180° clock position

DDR4 Mode

The following figure shows the phase offset of DDR4 command and data.

Figure 7-10 Phase Offset of Command and Data in DDR4 Mode (SMHC_NTSR[31] = 0)

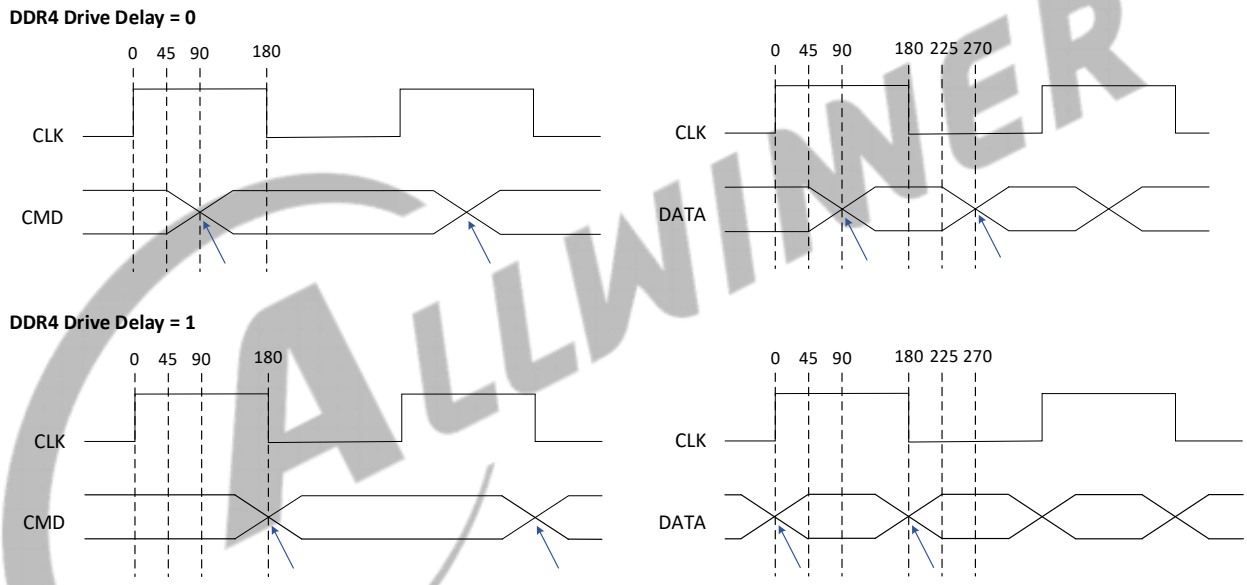


Figure 7-11 Phase Offset of Command and Data in DDR4 Mode

Drive Delay	Command	Data
0	The command is updated in 90° clock position	The data is updated in 90° clock position
1	The command is updated in 180° clock position	The data is updated in 0° or 180° clock position

DDR4 (2x) Mode

The following figure shows the phase offset of DDR4 (2x mode) command and data.

Figure 7-12 Phase Offset of Command and Data in DDR4 (2x Mode) (SMHC_NTSR[31] = 1)

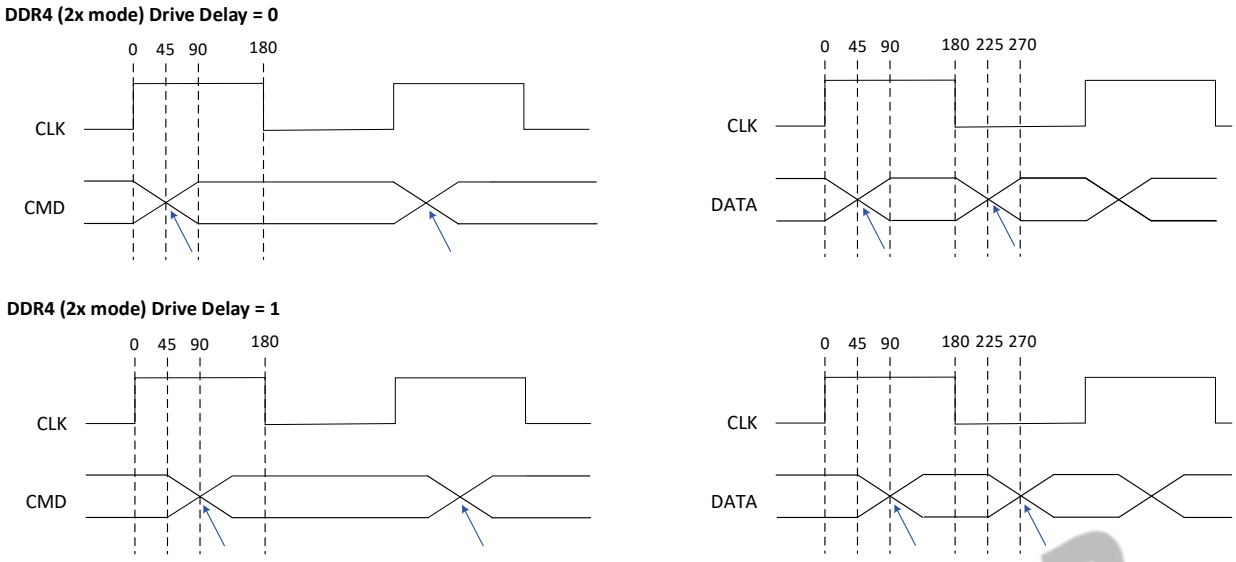


Table 7-8 Phase Offset of Command and Data in DDR4 (2x) Mode

Drive Delay	Command	Data
0	The command is updated in 45° clock position	The data is updated in 45° clock position
1	The command is updated in 90° clock position	The data is updated in 90° clock position

7.2.3.9 Internal DMA Controller Description

The SMHC has an internal DMA controller (IDMAC) to transfer data between the host memory and SMHC port. With a descriptor, the IDMAC can efficiently move data from the source to destination by automatically loading the next DMA transfer arguments, which needs less CPU intervention. Before transferring data in the IDMAC, the host driver should construct a descriptor list, configure arguments of every DMA transfer, and then launch the descriptor and start the DMA.

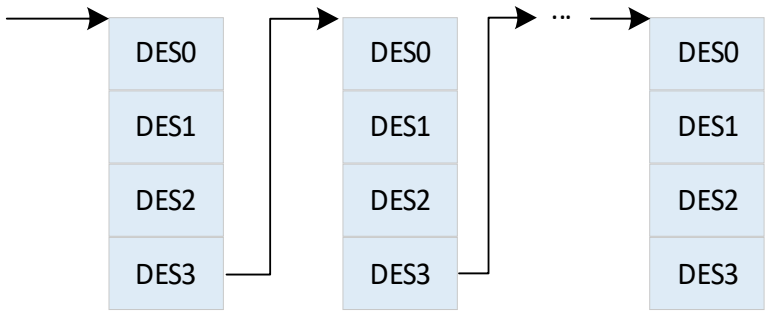
The IDMAC has an interrupt controller. When enabled, it generates an interrupt to the HOST CPU in situations such as data transmission is completed or some error is happened.

IDMAC Descriptor Structure

The IDMAC uses a descriptor with a chain structure, and each descriptor points to a unique buffer and the next descriptor.

The following figure shows the internal formats of a descriptor.

Figure 7-13 IDMAC Descriptor Structure Diagram



This figure illustrates the internal formats of a descriptor. The descriptor address must be aligned to the bus width used for 32-bit buses. Each descriptor contains 16 bytes of control and status information.

DES0 corresponds to the [31:0] bits, DES1 corresponds to the [63:32] bits, DES2 corresponds to the [95:64] bits, and DES3 corresponds the [127:96] bits in a descriptor.

The following table shows the bit definition of DES0.

Table 7-9 DES0 Definition

Bits	Name	Description
31	HOLD	DES_OWN_FLAG When set, this bit indicates that the descriptor is owned by the IDMAC. When this bit is reset, it indicates that the descriptor is owned by the host. This bit is cleared when the transfer is over.
30	ERROR	ERR_FLAG When some errors happen in transfer, this bit will be set to 1.
29:5	/	/
4	Chain Flag	CHAIN_MOD When set to 1, this bit indicates that the second address in the descriptor is the next descriptor address. It must be set to 1.
3	First DES Flag	FIRST_FLAG When set to 1, this bit indicates that this descriptor contains the first buffer of data. It must be set to 1 in the first DES.
2	Last DES Flag	LAST_FLAG When set to 1, this bit indicates that the buffers this descriptor points to are the last data buffer.
1	Disable Interrupt on completion	CUR_TXRX_OVER_INT_DIS When set to 1, this bit will prevent the setting of the TX/RX interrupt bit of the IDMAC status register for data that ends in the buffer the descriptor points to.
0	/	/

The following table shows the bit definition of DES1.

Table 7-10 DES1 Definition

Bits	Name	Description
31:13	/	/
12:0	Buffer size	BUFF_SIZE The bits indicate the data buffer byte size, which must be a multiple of 4 bytes. If this field is 0, the DMA ignores this buffer and proceeds to the next descriptor.

The following table shows the bit definition of DES2.

Table 7-11 DES2 Definition

Bits	Name	Descriptor
31:0	Buffer address pointer	BUFF_ADDR The bits indicate the physical address of the data buffer. It is a word address.

The following table shows the bit definition of DES3.

Table 7-12 DES3 Definition

Bits	Name	Descriptor
31:0	Next descriptor address	NEXT_DESP_ADDR The bits indicate the pointer to the physical memory where the next descriptor is present. It is a word address.

7.2.3.10 Calibrating the Delay Chain

There are two delay chains in SMHC: data strobe delay chain and sample delay chain.

Data strobe delay chain: used to generate delay to make proper timing between Data Strobe and data signals.

Sample delay chain: used to generate delay to make proper timing between the internal card clock signal and data signals.

Each delay chain is made up with 64 delay cells. The delay time of one delay cell can be estimated through delay chain calibration.

Follow the steps below to calibrate the delay chain:

Step 1 Enable SMHC. In order to calibrate the delay chain by the operation registers in SMHC, the SMHC must be enabled through SMHC Bus Gating Reset Register and SMHCx Clock Register.

Step 2 Configure a proper clock for SMHC. The delay chain calibration is based on the clock for SMHC from Clock Control Unit (CCU). The delay chain calibration is an internal function in SMHC and needs no devices. So it is unnecessary to open the clock signal for devices. The recommended clock frequency is 200 MHz.

Step 3 Set proper initial delay value. Writing 0xA0 to **delay control register** enables **Delay Software Enable** (bit[7]) and sets initial delay value 0x20 to **Delay chain** (bit[5:0]). Then write 0x0 to **delay control register** to clear the value.

Step 4 Write 0x8000 to **delay control register** to start calibrating the delay chain.

Step 5 Wait until the flag (bit14 in **delay control register**) of calibration done is set. The number of delay cells is shown at bit[13:8] in **delay control register**. The delay time generated by these delay cells is equal to the cycle of the SMHC clock nearly. This value is the result of calibration.

Step 6 Calculate the delay time of one delay cell according to the cycle of the SMHC clock and the result of calibration.

7.2.4 Programming Guidelines

7.2.4.1 Initializing SMHC

Before data and commands are exchanged between a card and the SMHC, the SMHC needs to be initialized. Follow the steps below to initialize the SMHC:

Step 1 Configure the corresponding GPIO register as an SMHC by Port Controller module; reset clock by writing 1 to **SMHC_BGR_REG**[SMHCx_RST], and open clock gating by writing 1 to **SMHC_BGR_REG**[SMHCx_GATING]; select clock sources and set the division factor by configuring the **SMHCx_CLK_REG** (x = 0, 1) register.

Step 2 Configure **SMHC_CTRL** to reset the FIFO and controller, and enable the global interrupt; configure **SMHC_INTMASK** to 0xFFCE to enable normal interrupts and error abnormal interrupts, and then register the interrupt function.

Step 3 Configure **SMHC_CLKDIV** to open clock for devices; configure **SMHC_CMD** as the change clock command (for example 0x80202000); send the update clock command to deliver clocks to devices.

Step 4 Configure SMHC_CMD as a normal command. Configure SMHC_CMDARG to set command parameters. Configure SMHC_CMD to set parameters like whether to send the response, the response type, and the response length and then send the commands. According to the initialization process in the protocol, you can finish SMHC initialization by sending the corresponding command one by one.

7.2.4.2 Writing a Single Data Block

To write a single data block, follow the steps below:

Step 1 Write 0x1 to SMHC_CTRL[DMA_RST] to reset the internal DMA controller; write 0x82 to SMHC_IDMAC to enable the IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable the transfer interrupt, receive interrupt, and abnormal interrupt.

Step 2 Configure SMHC_FIFOTH to determine the burst size and TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, it indicates the burst size is 16, TX_TL is 15, and RX_TL is 240. Configure SMHC_DLBA to determine the start address of the DMA descriptor.

Step 3 To write one block data to sector1, configure SMHC_BYTCNT[BYTE_CNT] to 0x200 and configure the descriptor according to the data size; set the data sector address of CMD24 (Single Data Block Write) to 0x1, write 0x80002758 to SMHC_CMD, and send CMD24 command to write data to the device.

Step 4 Check whether SMHC_RINTSTS[CC] is 1. If yes, the command is sent successfully; otherwise, continue to wait until timeout, and then exit the process.

Step 5 Check whether SMHC_IDST[TX_INT] is 1. If yes, the data transfer for writing DMA is completed. Write 0x337 to SMHC_IDST to clear the interrupt flag. Otherwise, continue to wait until timeout, and then exit the process.

Step 6 Check whether SMHC_RINTSTS[DTC] is 1. If yes, the data transfer and CMD24 writing operations are completed. Otherwise, abnormity exists. Read SMHC_RINTSTS and SMHC_STATUS to query the existing abnormity.

Step 7 Send CMD13 command to query whether the device writing operation is completed and returns to the idle status. For example, device RCA is 0x1234, first set SMHC_CMDARG to 0x12340000, write 0x8000014D to SMHC_CMD, go to step4 to ensure command transfer completed, and then check whether the highest bit of SMHC_RESP0 (CMD13 response) is 1. If yes, the device is in the idle status, and the next command can be sent. Otherwise, the device is in the busy status. Continue to send CMD13 to wait for the device to enter the idle status until timeout.

7.2.4.3 Reading a Single Data Block

To read a single data block, follow the steps below:

Step 1 Write 0x1 to SMHC_CTRL[DMA_RST] to reset the internal DMA controller; write 0x82 to SMHC_IDMAC to enable the IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable the transfer interrupt, receive interrupt, and abnormal interrupt.

Step 2 Configure SMHC_FIFOTH to determine the burst size and TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, it indicates the burst size is 16, TX_TL is 15, and RX_TL is 240. Configure SMHC_DLBA to determine the start address of the DMA descriptor.

Step 3 To read one block data from sector1, configure SMHC_BYTCNT[BYTE_CNT] to 0x200 and configure the descriptor according to the data size; set the data sector address of CMD17 command (Single Data Block Read) to 0x1, write 0x80002351 to SMHC_CMD, and send CMD17 command to read data from the device to DRAM/SRAM.

Step 4 Check whether SMHC_RINTSTS[CC] is 1. If yes, the command is sent successfully; otherwise, continue to wait until timeout, and then exit the process.

Step 5 Check whether SMHC_IDST[RX_INT] is 1. If yes, the data transfer for writing DMA is completed. Write 0x337 to SMHC_IDST to clear the interrupt flag. Otherwise, continue to wait until timeout, and then exit the process.

Step 6 Check whether SMHC_RINTSTS[DTC] is 1. If yes, data transfer and CMD17 reading operation are completed. Otherwise, abnormity exists. Read SMHC_RINTSTS and SMHC_STATUS to query the existing abnormity.

7.2.4.4 Writing Open-Ended Multiple Data Blocks (CMD25 + Auto CMD12)

To write open-ended multiple data blocks, follow the steps below:

Step 1 Write 0x1 to SMHC_CTRL[DMA_RST] to reset the internal DMA controller; write 0x82 to SMHC_IDMAC to enable the IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable the transfer interrupt, receive interrupt, and abnormal interrupt.

Step 2 Configure SMHC_FIFOTH to determine the burst size and TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, it indicates the burst size is 16, TX_TL is 15, and RX_TL is 240. Configure SMHC_DLBA to determine the start address of the DMA descriptor.

Step 3 To write three blocks of data to sectors begin with sector0, configure SMHC_BYTCNT[BYTE_CNT] to 0x600 and configure the descriptor according to the data size; set the data sector address of CMD25 command (Multiple Data Blocks Write) to 0x0, write 0x80003759 to SMHC_CMD, and send CMD25 command to read data from the device to DRAM/SRAM.

Step 4 Check whether SMHC_RINTSTS[CC] is 1. If yes, the command is sent successfully; otherwise, continue to wait until timeout, and then exit the process.

Step 5 Check whether SMHC_IDST[RX_INT] is 1. If yes, the data transfer for writing DMA is completed. Write 0x337 to SMHC_IDST to clear the interrupt flag. Otherwise, continue to wait until timeout, and then exit the process.

Step 6 Check whether SMHC_RINTSTS [ACD] and SMHC_RINTSTS[DTC] are both 1. If yes, the data transfer, CMD12 transfer, and CMD25 writing operations are completed. Otherwise, abnormity exists. Read SMHC_RINTSTS and SMHC_STATUS to query the existing abnormity.

Step 7 Send CMD13 command to query whether the device writing operation is completed and returns to the idle status. For example, device RCA is 0x1234, first set SMHC_CMDARG to 0x12340000, write 0x8000014D to SMHC_CMD, go to step4 to ensure command transfer completed, and then check whether the highest bit of SMHC_RESP0 (CMD13 response) is 1. If yes, the device is in the idle status, and the next command can be sent. Otherwise, the device is in the busy status. Continue to send CMD13 to wait for the device to enter the idle status until timeout.

7.2.4.5 Reading Open-Ended Multiple Data Blocks (CMD18 + Auto CMD12)

To read open-ended multiple data blocks, follow the steps below:

Step 1 Write 0x1 to SMHC_CTRL[DMA_RST] to reset the internal DMA controller; write 0x82 to SMHC_IDMAC to enable the IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable the transfer interrupt, receive interrupt, and abnormal interrupt.

Step 2 Configure SMHC_FIFOTH to determine the burst size and TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, it indicates the burst size is 16, TX_TL is 15, and RX_TL is 240. Configure SMHC_DLBA to determine the start address of the DMA descriptor.

Step 3 To read three blocks of data from sectors begin with sector0, configure SMHC_BYTCNT[BYTE_CNT] to 0x600 and configure the descriptor according to the data size; set the data sector address of CMD18 command (Multiple Data Blocks Read) to 0x0, write 0x80003352 to SMHC_CMD, and send CMD18 command to read data to the device. When the data transfer is completed, CMD12 will be sent automatically.

Step 4 Check whether SMHC_RINTSTS[CC] is 1. If yes, the command is sent successfully; otherwise, continue to wait until timeout, and then exit the process.

Step 5 Check whether SMHC_IDST[RX_INT] is 1. If yes, the data transfer for writing DMA is completed. Write 0x337 to SMHC_IDST to clear the interrupt flag. Otherwise, continue to wait until timeout, and then exit the process.

Step 6 Check whether SMHC_RINTSTS[ACD] and SMHC_RINTSTS[DTC] are both 1. If yes, data transfer, CMD12 transfer, and CMD18 reading operation are completed. Otherwise, abnormity exists. Read SMHC_RINTSTS and SMHC_STATUS to query the existing abnormity.

7.2.4.6 Writing Pre-Defined Multiple Data Blocks (CMD23 + CMD25)

To write pre-defined multiple data blocks, follow the steps below:

Step 1 Write 0x1 to SMHC_CTRL[DMA_RST] to reset the internal DMA controller; write 0x82 to SMHC_IDMAC to enable the IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable the transfer interrupt, receive interrupt, and abnormal interrupt.

Step 2 Configure SMHC_FIFOTH to determine the burst size and TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, it indicates the burst size is 16, TX_TL is 15, and RX_TL is 240. Configure SMHC_DLBA to determine the start address of the DMA descriptor.

Step 3 To write three blocks of data, configure SMHC_CMDARG to 0x3 to specify the number of data blocks as three. Then write 0x80000157 to SMHC_CMD to send the CMD23 command. Check whether SMHC_RINTSTS[CC] is 1. If yes, the command is sent successful; otherwise, continue to wait until timeout, and then exit the process.

Step 4 Configure SMHC_BYTCNT[BYTE_CNT] to 0x600 and configure the descriptor according to the data size; set the data sector address of CMD25 command (Multiple Data Blocks Write) to 0x0, write 0x80002759 to SMHC_CMD, and send CMD25 command to write data to the device.

Step 5 Check whether SMHC_RINTSTS[CC] is 1. If yes, the command is sent successful; otherwise, continue to wait until timeout, and then exit the process.

Step 6 Check whether SMHC_IDST[TX_INT] is 1. If yes, the data transfer for writing DMA is completed. Write 0x337 to SMHC_IDST to clear the interrupt flag. Otherwise, continue to wait until timeout, and then exit the process.

Step 7 Check whether SMHC_RINTSTS[DTC] is 1. If yes, the data transfer and CMD25 writing operations are completed. Otherwise, abnormity exists. Read SMHC_RINTSTS and SMHC_STATUS to query the existing abnormity.

Step 8 Send CMD13 command to query whether the device writing operation is completed and returns to the idle status. For example, device RCA is 0x1234, first set SMHC_CMDARG to 0x12340000, write 0x8000014D to SMHC_CMD, go to step4 to ensure command transfer completed, and then check whether the highest bit of SMHC_RESP0 (CMD13 response) is 1. If yes, the device is in the idle status, and the next command can be sent. Otherwise, the device is in the busy status. Continue to send CMD13 to wait for the device to enter the idle status until timeout.

7.2.4.7 Reading Pre-Defined Multiple Data Blocks (CMD23 + CMD18)

To read pre-defined multiple data blocks, follow the steps below:

Step 1 Write 0x1 to SMHC_CTRL[DMA_RST] to reset the internal DMA controller; write 0x82 to SMHC_IDMAC to enable the IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable the transfer interrupt, receive interrupt, and abnormal interrupt.

Step 2 Configure SMHC_FIFOTH to determine the burst size and TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, it indicates the burst size is 16, TX_TL is 15, and RX_TL is 240. Configure SMHC_DLBA to determine the start address of the DMA descriptor.

Step 3 To read three blocks of data, configure SMHC_CMDARG to 0x3 to specify the number of data blocks as three. Then write 0x80000157 to SMHC_CMD to send the CMD23 command. Check whether SMHC_RINTSTS[CC] is 1. If yes, the command is sent successful; otherwise, continue to wait until timeout, and then exit the process.

Step 4 Configure SMHC_BYTCNT[BYTE_CNT] to 0x600 and configure the descriptor according to the data size; set the data sector address of CMD18 (Multiple Data Blocks Read) to 0x0, write 0x80002352 to SMHC_CMD, and send CMD18 command to read data from device to DRAM/SRAM.

Step 5 Check whether SMHC_RINTSTS[CC] is 1. If yes, the command is sent successful; otherwise, continue to wait until timeout, and then exit the process.

Step 6 Check whether SMHC_IDST[TX_INT] is 1. If yes, the data transfer for writing DMA is completed. Write 0x337 to SMHC_IDST to clear the interrupt flag. Otherwise, continue to wait until timeout, and then exit the process.

Step 7 Check whether SMHC_RINTSTS[DTC] is 1. If yes, the data transfer and CMD18 writing operations are completed. Otherwise, abnormity exists. Read SMHC_RINTSTS and SMHC_STATUS to query the existing abnormity.

7.2.5 Register List

Module Name	Base Address
SMHC0	0x04020000
SMHC1	0x04021000
SMHC2	0x04022000

Register Name	Offset	Description
SMHC_CTRL	0x0000	Control Register
SMHC_CLKDIV	0x0004	Clock Control Register
SMHC_TMOUT	0x0008	Time Out Register
SMHC_CTYPE	0x000C	Bus Width Register

Register Name	Offset	Description
SMHC_BLKSIZ	0x0010	Block Size Register
SMHC_BYTCNT	0x0014	Byte Count Register
SMHC_CMD	0x0018	Command Register
SMHC_CMDARG	0x001C	Command Argument Register
SMHC_RESP0	0x0020	Response 0 Register
SMHC_RESP1	0x0024	Response 1 Register
SMHC_RESP2	0x0028	Response 2 Register
SMHC_RESP3	0x002C	Response 3 Register
SMHC_INTMASK	0x0030	Interrupt Mask Register
SMHC_MINTSTS	0x0034	Masked Interrupt Status Register
SMHC_RINTSTS	0x0038	Raw Interrupt Status Register
SMHC_STATUS	0x003C	Status Register
SMHC_FIFOTH	0x0040	FIFO Water Level Register
SMHC_FUNS	0x0044	FIFO Function Select Register
SMHC_TCBCNT	0x0048	Transferred Byte Count between Controller and Card
SMHC_TBBCNT	0x004C	Transferred Byte Count between Host Memory and Internal FIFO
SMHC_DBGC	0x0050	Current Debug Control Register
SMHC_CSDC	0x0054	CRC Status Detect Control Registers
SMHC_A12A	0x0058	Auto Command 12 Argument Register
SMHC_NTSR	0x005C	SD New Timing Set Register
SMHC_HWRST	0x0078	Hardware Reset Register
SMHC_IDMAC	0x0080	IDMAC Control Register
SMHC_DLBA	0x0084	Descriptor List Base Address Register
SMHC_IDST	0x0088	IDMAC Status Register
SMHC_IDIE	0x008C	IDMAC Interrupt Enable Register
SMHC_THLD	0x0100	Card Threshold Control Register
SMHC_SFC	0x0104	Sample FIFO Control Register
SMHC_A23A	0x0108	Auto Command 23 Argument Register
EMMC_DDR_SBIT_DET	0x010C	eMMC4.5 DDR Start Bit Detection Control Register
SMHC_EXT_CMD	0x0138	Extended Command Register
SMHC_EXT_RESP	0x013C	Extended Response Register
SMHC_DRV_DL	0x0140	Drive Delay Control Register
SMHC_SMAP_DL	0x0144	Sample Delay Control Register

Register Name	Offset	Description
SMHC_DS_DL	0x0148	Data Strobe Delay Control Register
SMHC_HS400_DL	0x014C	HS400 Delay Control Register
SMHC_FIFO	0x0200	Read/Write FIFO

7.2.6 Register Description

7.2.6.1 0x0000 SMHC Global Control Register (Default Value: 0x0000_0100)

Offset: 0x0000			Register Name: SMHC_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	FIFO_AC_MOD FIFO Access Mode 0: DMA bus 1: AHB bus
30:13	/	/	/
12	R/W	0x0	TIME_UNIT_CMD Time unit for command line The time unit is used to calculate the command line time out value defined in RTO_LMT. 0: 1 card clock period 1: 256 card clock period
11	R/W	0x0	TIME_UNIT_DAT Time unit for data line Time unit is used to calculate the data line time out value defined in DTO_LMT. 0: 1 card clock period 1: 256 card clock period
10	R/W	0x0	DDR_MOD_SEL DDR Mode Select Although the HS400 speed mode of eMMC is 8-bit DDR, this field should be cleared when HS400_MD_EN is set. 0: SDR mode 1: DDR mode
9	/	/	/

Offset: 0x0000			Register Name: SMHC_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
8	R/W	0x1	CD_DBC_ENB Card Detect (Data[3] status) De-bounce Enable 0: Disable de-bounce 1: Enable de-bounce
7:6	/	/	/
5	R/W	0x0	DMA_ENB DMA Global Enable 0: Disable DMA to transfer data via AHB bus 1: Enable DMA to transfer data
4	R/W	0x0	INT_ENB Global Interrupt Enable 0: Disable interrupts 1: Enable interrupts
3	/	/	/
2	R/W	0x0	DMA_RST DMA Reset
1	R/W	0x0	FIFO_RST FIFO Reset 0: No effect 1: Reset the FIFO This bit is auto-cleared after the completion of the reset operation.
0	R/W	0x0	SOFT_RST Software Reset 0: No effect 1: Reset SD/MMC controller This bit is auto-cleared after the completion of reset operation.

7.2.6.2 0x0004 SMHC Clock Control Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: SMHC_CLKDIV
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MASK_DATA0 0: Do not mask data0 when update clock 1: Mask data0 when update clock
30:18	/	/	/

Offset: 0x0004			Register Name: SMHC_CLKDIV
Bit	**Read/Write**	**Default/Hex**	**Description**
17	R/W	0x0	CCLK_CTRL Card Clock Output Control 0: Card clock is always on. 1: Turn off card clock when FSM is in IDLE state.
16	R/W	0x0	CCLK_ENB Card Clock Enable 0: Card Clock is off. 1: Card Clock is on.
15:8	/	/	/
7:0	R/W	0x0	CCLK_DIV Card Clock Divider n: Source clock is divided by 2*n. (n = 0 to 255) When HS400_MD_EN is set, this field must be cleared.

7.2.6.3 0x0008 SMHC Timeout Register (Default Value: 0xFFFF_FF40)

Offset: 0x0008			Register Name: SMHC_TMOUT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	R/W	0xffffff	DTO_LMT Data Timeout Limit This field can set the time that the host waits for the data from the device. Ensure to communicate with the device, this field must be set to the maximum that is greater than the time N_{AC}. About the N_{AC}, the explanation is as follows: When Host read data, data transmission from the Device starts after the access time delay N_{AC} beginning from the end bit of the read command (ACMD51, CMD8, CMD17, and CMD18). When the host reads multiple block (CMD18), a next block's data transmission from the Device starts after the access time delay N_{AC} beginning from the end bit of the previous block. When the host writes data, the value is no effect.
7:0	R/W	0x40	RTO_LMT Response Timeout Limit

7.2.6.4 0x000C SMHC Bus Width Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: SMHC_CTYPE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x0	CARD_WID Card Width 00: 1-bit width 01: 4-bit width 1x: 8-bit width

7.2.6.5 0x0010 SMHC Block Size Register (Default Value: 0x0000_0200)

Offset: 0x0010			Register Name: SMHC_BLKSIZ
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x200	BLK_SZ Block Size

7.2.6.6 0x0014 SMHC Byte Count Register (Default Value: 0x0000_0200)

Offset: 0x0014			Register Name: SMHC_BYTCNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x200	BYTE_CNT Byte counter The number of bytes to be transferred. It must be integer multiple of Block Size (BLK_SZ) for block transfers.

7.2.6.7 0x0018 SMHC Command Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: SMHC_CMD
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CMD_LOAD Start Command This bit is automatically cleared when the current command is sent. If there is no response error happens, a command complete interrupt bit (CMD_OVER) will be set in the interrupt register. Do not write any other commands until this bit is cleared.
30:29	/	/	/
28	R/W	0x0	VOL_SW Voltage Switch 0: Normal command 1: Voltage switch command, set for CMD11 only.
27	R/W	0x0	BOOT_ABT Boot Abort Setting this bit will terminate the boot operation.
26	R/W	0x0	EXP_BOOT_ACK Expect Boot Acknowledge When the software sets this bit along in mandatory boot operation, the controller expects a boot acknowledge start pattern of 0-1-0 from the selected card.
25:24	R/W	0x0	BOOT_MOD Boot Mode 00: Normal command 01: Mandatory Boot operation 10: Alternate Boot operation 11: Reserved
23:22	/	/	/
21	R/W	0x0	PRG_CLK Change Clock 0: Normal command 1: Change Card Clock When this bit is set, the controller will change the clock domain and clock output. No commands will be sent.
20:16	/	/	/

Offset: 0x0018			Register Name: SMHC_CMD
Bit	**Read/Write**	**Default/Hex**	**Description**
15	R/W	0x0	SEND_INIT_SEQ Send Initialization 0: Normal command sending 1: Send initialization sequence before sending this command.
14	R/W	0x0	STOP_ABT_CMD Stop Abort Command 0: Normal command sending 1: Send *Stop* or *Abort* command to stop the current data transfer in progress. (CMD12, CMD52 for writing "I/O Abort" in SDIO CCCR)
13	R/W	0x0	WAIT_PRE_OVER Wait for Data Transfer Over 0: Send command at once, does not care about data transferring. 1: Wait for data transfer completion before sending the current command.
12	R/W	0x0	STOP_CMD_FLAG Send Stop CMD Automatically (CMD12) 0: Do not send stop command at the end of the data transfer. 1: Send stop command automatically at the end of the data transfer. If set, the SMHC_RESP1 will record the response of auto CMD12.
11	R/W	0x0	TRANS_MODE Transfer Mode 0: Block data transfer command 1: Stream data transfer command
10	R/W	0x0	TRANS_DIR Transfer Direction 0: Read operation 1: Write operation
9	R/W	0x0	DATA_TRANS Data Transfer 0: Without data transfer 1: With data transfer

Offset: 0x0018			Register Name: SMHC_CMD
Bit	**Read/Write**	**Default/Hex**	**Description**
8	R/W	0x0	CHK_RESP_CRC Check Response CRC 0: Do not check response CRC 1: Check response CRC
7	R/W	0x0	LONG_RESP Response Type 0: Short Response (48 bits) 1: Long Response (136 bits)
6	R/W	0x0	RESP_RCV Response Receive 0: Command without response 1: Command with response
5:0	R/W	0x0	CMD_IDX CMD Index Command index value

7.2.6.8 0x001C SMHC Command Argument Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: SMHC_CMDARG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	CMD_ARG Command argument

7.2.6.9 0x0020 SMHC Response 0 Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SMHC_RESP0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CMD_RESP0 Response 0 Bit[31:0] of response

7.2.6.10 0x0024 SMHC Response 1 Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: SMHC_RESP1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CMD_RESP1 Response 1 Bit[63:31] of response

7.2.6.11 0x0028 SMHC Response 2 Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: SMHC_RESP2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CMD_RESP2 Response 2 Bit[95:64] of response

7.2.6.12 0x002C SMHC Response 3 Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: SMHC_RESP3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CMD_RESP3 Response 3 Bit[127:96] of response

7.2.6.13 0x0030 SMHC Interrupt Mask Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: SMHC_INTMASK
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CARD_REMOVAL_INT_EN Card Removed Interrupt Enable
30	R/W	0x0	CARD_INSERT_INT_EN Card Inserted Interrupt Enable
29:17	/	/	/
16	R/W	0x0	SDIO_INT_EN SDIO Interrupt Enable

Offset: 0x0030			Register Name: SMHC_INTMASK
Bit	**Read/Write**	**Default/Hex**	**Description**
15	R/W	0x0	DEE_INT_EN Data End-bit Error Interrupt Enable
14	R/W	0x0	ACD_INT_EN Auto Command Done Interrupt Enable
13	R/W	0x0	DSE_BC_INT_EN Data Start Error Interrupt Enable
12	R/W	0x0	CB_IW_INT_EN Command Busy and Illegal Write Interrupt Enable
11	R/W	0x0	FU_FO_INT_EN FIFO Underrun/Overflow Interrupt Enable
10	R/W	0x0	DSTO_VSD_INT_EN Data Starvation Timeout/V1.8 Switch Done Interrupt Enable
9	R/W	0x0	DTO_BDS_INT_EN Data Timeout/Boot Data Start Interrupt Enable
8	R/W	0x0	RTO_BACK_INT_EN Response Timeout/Boot ACK Received Interrupt Enable
7	R/W	0x0	DCE_INT_EN Data CRC Error Interrupt Enable
6	R/W	0x0	RCE_INT_EN Response CRC Error Interrupt Enable
5	R/W	0x0	DRR_INT_EN Data Receive Request Interrupt Enable
4	R/W	0x0	DTR_INT_EN Data Transmit Request Interrupt Enable
3	R/W	0x0	DTC_INT_EN Data Transfer Complete Interrupt Enable
2	R/W	0x0	CC_INT_EN Command Complete Interrupt Enable
1	R/W	0x0	RE_INT_EN Response Error Interrupt Enable
0	/	/	/

7.2.6.14 0x0034 SMHC Masked Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: SMHC_MINTSTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	M_CARD_REMOVAL_INT Card Removed
30	R	0x0	M_CARD_INSERT Card Inserted
29:17	/	/	/
16	R	0x0	M_SDIO_INT SDIO Interrupt
15	R	0x0	M_DEE_INT Data End-bit Error When the bit is set during receiving data, it means that the host controller does not receive the valid data end bit. When the bit is set during transmitting data, it means that the host controller does not receive the CRC status token. This is a write-1-to-clear bit.
14	R	0x0	M_ACD_INT Auto Command Done When set, it means auto-stop command (CMD12) completed.
13	R	0x0	M_DSE_BC_INT Data Start Error/Busy Clear When set during receiving data, it means that the host controller found an error start bit. When the bit is set during transmitting data, it means that the busy signal is cleared after the last block.
12	R	0x0	M_CB_IW_INT Command Busy and Illegal Write
11	R	0x0	M_FU_FO_INT FIFO Underrun/Overflow
10	R	0x0	M_DSTO_VSD_INT Data Starvation Timeout/V1.8 Switch Done
9	R	0x0	M_DTO_BDS_INT Data Timeout/Boot Data Start
8	R	0x0	M_RTO_BACK_INT Response Timeout/Boot ACK Received

Offset: 0x0034			Register Name: SMHC_MINTSTS
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R	0x0	M_DCE_INT Data CRC Error When the bit is set during receiving data, it means that the received data have data CRC error. When the bit is set during transmitting data, it means that the received CRC status taken is negative.
6	R	0x0	M_RCE_INT Response CRC Error
5	R	0x0	M_DRR_INT Data Receive Request When set, it means that there are enough data in FIFO during receiving data.
4	R	0x0	M_DTR_INT Data Transmit Request When set, it means that there is enough space in FIFO during transmitting data.
3	R	0x0	M_DTC_INT Data Transfer Complete
2	R	0x0	M_CC_INT Command Complete
1	R	0x0	M_RE_INT Response Error When set, Transmit Bit error or End Bit error or CMD Index error may occurs.
0	/	/	/

7.2.6.15 0x0038 SMHC Raw Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: SMHC_RINTSTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W1C	0x0	CARD_REMOVAL Card Removed Write 1 to clear this bit.

Offset: 0x0038			Register Name: SMHC_RINTSTS
Bit	**Read/Write**	**Default/Hex**	**Description**
30	R/W1C	0x0	CARD_INSERT Card Inserted Write 1 to clear this bit.
29:17	/	/	/
16	R/W1C	0x0	SDIOI_INT SDIO Interrupt Write 1 to clear this bit.
15	R/W1C	0x0	DEE Data End-bit Error When the bit is set during receiving data, it means that the host controller does not receive the valid data end bit. When the bit is set during transmitting data, it means that the host controller does not receive the CRC status token. Write 1 to clear this bit.
14	R/W1C	0x0	ACD Auto Command Done When set, it means that the auto-stop command (CMD12) is completed. Write 1 to clear this bit.
13	R/W1C	0x0	DSE_BC Data Start Error/Busy Clear When the bit is set during receiving data, it means that the host controller found an error start bit. When the bit is set during transmitting data, it means that the busy signal is cleared after the last block. Write 1 to clear this bit.
12	R/W1C	0x0	CB_IW Command Busy and Illegal Write Write 1 to clear this bit.
11	R/W1C	0x0	FU_FO FIFO Underrun/Overflow Write 1 to clear this bit.
10	R/W1C	0x0	DSTO_VSD Data Starvation Timeout/V1.8 Switch Done Write 1 to clear this bit.

Offset: 0x0038			Register Name: SMHC_RINTSTS
Bit	**Read/Write**	**Default/Hex**	**Description**
9	R/W1C	0x0	DTO_BDS Data Timeout/Boot Data Start When the bit is set during receiving data, it means that some of the channel of DATA[3:0] lack of the start bit. Write 1 to clear this bit.
8	R/W1C	0x0	RTO_BACK Response Timeout/Boot ACK Received Write 1 to clear this bit.
7	R/W1C	0x0	DCE Data CRC Error When the bit is set during receiving data, it means that the received data have data CRC error. When the bit is set during transmitting data, it means that the received CRC status taken is negative. Write 1 to clear this bit.
6	R/W1C	0x0	RCE Response CRC Error Write 1 to clear this bit.
5	R/W1C	0x0	DRR Data Receive Request When set, it means that there are enough data in FIFO during receiving data. Write 1 to clear this bit.
4	R/W1C	0x0	DTR Data Transmit Request When set, it means that there is enough space in FIFO during transmitting data. Write 1 to clear this bit.
3	R/W1C	0x0	DTC Data Transfer Complete When set, it means that the current command completes even through error occurs. Write 1 to clear this bit.

Offset: 0x0038			Register Name: SMHC_RINTSTS
Bit	**Read/Write**	**Default/Hex**	**Description**
2	R/W1C	0x0	CC Command Complete When set, it means that the current command completes even through error occurs. Write 1 to clear this bit.
1	R/W1C	0x0	RE Response Error When set, it means that the transmit bit error, end bit error, or CMD index error may occur. Write 1 to clear this bit.
0	/	/	/

7.2.6.16 0x003C SMHC Status Register (Default Value: 0x0000_0006)

Offset: 0x003C			Register Name: SMHC_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	DMA_REQ DMA Request DMA request signal state
30:26	/	/	/
25:17	R	0x0	FIFO_LEVEL FIFO Level Number of filled locations in FIFO
16:11	R	0x0	RESP_IDX Response Index Index of previous response, including any auto-stop sent by the controller.
10	R	0x0	FSM_BUSY Data FSM Busy Data transmit or receive state-machine is busy.
9	R	0x0	CARD_BUSY Card Data Busy Inverted version of DATA[0] 0: Card data is not busy. 1: Card data is busy.

Offset: 0x003C			Register Name: SMHC_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
8	R	0x0	CARD_PRESENT Data[3] Status The level of DATA[3], checks whether the card is present. 0: The card is not present. 1: The card is present.
7:4	R	0x0	FSM_STA Command FSM States 0000: Idle 0001: Send init sequence 0010: TX CMD start bit 0011: TX CMD TX bit 0100: TX CMD index + argument 0101: TX CMD CRC7 0110: TX CMD end bit 0111: RX response start bit 1000: RX response IRQ response 1001: RX response TX bit 1010: RX response CMD index 1011: RX response data 1100: RX response CRC7 1101: RX response end bit 1110: CMD path wait NCC 1111: Wait; CMD-to-response turn around
3	R	0x0	FIFO_FULL FIFO Full 0: FIFO is not full 1: FIFO is full
2	R	0x1	FIFO_EMPTY FIFO Empty 0: FIFO is not empty 1: FIFO is empty
1	R	0x1	FIFO_TX_LEVEL FIFO TX Water Level Flag 0: FIFO does not reach the transmit trigger level 1: FIFO reaches the transmit trigger level

Offset: 0x003C			Register Name: SMHC_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
0	R	0x0	FIFO_RX_LEVEL FIFO RX Water Level Flag 0: FIFO does not reach the receive trigger level. 1: FIFO reaches the receive trigger level.

7.2.6.17 0x0040 SMHC FIFO Water Level Register (Default Value: 0x000F_0000)

Offset: 0x0040			Register Name: SMHC_FIFOTH
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x0	BSIZE_OF_TRANS Burst Size of Multiple Transaction 000: 1 transfers 001: 4 010: 8 011: 16 Others: Reserved It should be programmed the same as the DMA controller multiple transaction size. The units for the transfer are the DWORD. A single transfer would be signaled based on this value. The value should be sub-multiple of (RX_TL + 1) and (FIFO_DEPTH - TX_TL) Recommended: FIFO_DEPTH = 256, FIFO_SIZE = 256 * 32 = 1K MSize = 16, TX_TL = 240, RX_TL = 15
27:24	/	/	/

Offset: 0x0040			Register Name: SMHC_FIFOTH
Bit	**Read/Write**	**Default/Hex**	**Description**
23:16	R/W	0xF	RX_TL RX Trigger Level 0x0 to 0xFE: The RX trigger level is from 0 to 254. 0xFF: Reserved Indicates the FIFO threshold for the FIFO request host to receive data from the FIFO. When the FIFO data level is greater than this value, the DMA request is raised if DMA enabled, or the RX interrupt bit is set if interrupt enabled. At the end of the packet, if the last transfer is less than this level, the value is ignored and the relative request will be raised as usual. Recommended: 15 (means greater than 15)
15:8	/	/	/
7:0	R/W	0x0	TX_TL TX Trigger Level 0x1 to 0xFF: The TX trigger level is 1 to 255. 0x0: No trigger Indicates the FIFO threshold for the FIFO request host to transmit data to the FIFO. When the FIFO data level is less than or equal to this value, the DMA TX request is raised if DMA enabled, or TX request interrupt bit is set if interrupt enabled. At the end of the packet, if the last transfer is less than this level, the value is ignored and the relative request will be raised as usual. Recommended: 240 (means less than or equal to 240)

7.2.6.18 0x0044 SMHC Function Select Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: SMHC_FUNS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/

Offset: 0x0044			Register Name: SMHC_FUNS
Bit	**Read/Write**	**Default/Hex**	**Description**
2	R/W	0x0	ABT_RDATA Abort Read Data 0: Ignored 1: After the suspend command is issued during the read-transfer, the software polls card to find when the suspend happens. Once the suspend occurs, the software sets the bit to reset the data state-machine, which is waiting for the next block of data. This bit is used in the SDIO card suspends sequence and is auto-cleared once the controller resets to the idle state.
1	R/W	0x0	READ_WAIT Read Wait 0: Clear SDIO read wait 1: Assert SDIO read wait
0	R/W	0x0	HOST_SEND_MMC_IRQRESQ Host Send MMC IRQ Response 0: Ignored 1: Send auto IRQ response When the host is waiting for the MMC card interrupt response, setting this bit will make the controller cancel the waiting state and return to the idle state, at which time, the controller will receive the IRQ response sent by itself. This bit is auto-cleared after the response is sent.

7.2.6.19 0x0048 SMHC Transferred Byte Count Register 0 (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: SMHC_TBC0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	TBC0 Transferred Count 0 The number of bytes transferred between the card and internal FIFO. The register should be accessed in full to avoid read-coherency problems and read only after the data transfer completes.

7.2.6.20 0x004C SMHC Transferred Byte Count Register 1 (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: SMHC_TBC1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	TBC1 Transferred Count 1 The number of bytes transferred between the Host/DMA memory and internal FIFO. The register should be accessed in full to avoid read-coherency problems and read only after the data transfer completes.

7.2.6.21 0x0054 SMHC CRC Status Detect Control Register (Default Value: 0x0000_0003)

Offset: 0x0054			Register Name: SMHC_CSDC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x3	CRC_DET_PARA 110: HS400 speed mode 011: Other speed mode Others: Reserved

7.2.6.22 0x0058 SMHC Auto Command 12 Argument Register (Default Value: 0x0000_FFFF)

Offset: 0x0058			Register Name: SMHC_A12A
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xffff	SD_A12A Auto CMD12 Argument The argument of command 12 automatically sent by the controller.

7.2.6.23 0x005C SMHC New Timing Set Register (Default Value: 0x8171_0000)

Offset: 0x005C			Register Name: SMHC_NTSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	MODE_SELECT 0: Old mode of Sample/Output Timing 1: New mode of Sample/Output Timing
30:25	/	/	/
24	R/W	0x1	CMD_DAT_RX_PHASE_CLR Clear the input phase of command lines and data lines during the update clock operation. 0: Disabled 1: Enabled
23	/	/	/
22	R/W	0x1	DAT_CRC_STATUS_RX_PHASE_CLR Clear the input phase of data lines before receiving the CRC status. 0: Disabled 1: Enabled
21	R/W	0x1	DAT_TRANS_RX_PHASE_CLR Clear the input phase of data lines before transferring the data. 0: Disabled 1: Enabled
20	R/W	0x1	DAT_RECV_RX_PHASE_CLR Clear the input phase of data lines before receiving the data. 0: Disabled 1: Enabled
19:17	/	/	/
16	R/W	0x1	CMD_SEND_RX_PHASE_CLR Clear command rx phase before sending the command. 0: Disabled 1: Enabled
15:10	/	/	/
9:8	R/W	0x0	DAT_SAMPLE_TIMING_PHASE 00: Sample timing phase offset 90^0 01: Sample timing phase offset 180^0 10: Sample timing phase offset 270^0 11: Sample timing phase offset 0^0 (only for SD2 hs400 mode)

Offset: 0x005C			Register Name: SMHC_NTSR
Bit	**Read/Write**	**Default/Hex**	**Description**
7:6	/	/	/
5:4	R/W	0x0	CMD_SAMPLE_TIMING_PHASE 00: Sample timing phase offset 90^0 01: Sample timing phase offset 180^0 10: Sample timing phase offset 270^0 11: Ignore
3:1	/	/	/
0	R/W	0x0	HS400_NEW_SAMPLE_EN 0: Disable hs400 new sample method 1: Enable hs400 new sample method

7.2.6.24 0x0078 SMHC Hardware Reset Register (Default Value: 0x0000_0001)

Offset: 0x0078			Register Name: SMHC_HWRST
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x1	HW_RST 1: Active mode 0: Reset These bits cause the cards to enter the pre-idle state, which requires them to be re-initialized.

7.2.6.25 0x0080 SMHC IDMAC Control Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: SMHC_IDMAC
Bit	**Read/Write**	**Default/Hex**	**Description**
31	W	0x0	DES_LOAD_CTRL When IDMAC fetches a descriptor, if the valid bit of a descriptor is not set, IDMAC FSM will go to the suspend state. Setting this bit will make the IDMAC refetch descriptor again and do the transfer normally.
30:11	/	/	/
10:8	R	0x0	Reserved

Offset: 0x0080			Register Name: SMHC_IDMAC
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x0	IDMAC_ENB IDMAC Enable When set, the IDMAC is enabled.
6:2	R/W	0x0	Reserved
1	R/W	0x0	FIX_BUST_CTRL Fixed Burst Controls whether the AHB Master interface performs fixed burst transfers or not. When set, the AHB will use only SINGLE, INCR4, and INCR8 during the start of normal burst transfers. When reset, the AHB will use SINGLE and INCR burst transfer operations.
0	R/W	0x0	IDMAC_RST DMA Reset When set, the DMA Controller resets all its internal registers. It is automatically cleared after 1 clock cycle.

7.2.6.26 0x0084 SMHC Descriptor List Base Address Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: SMHC_DLBA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DES_BASE_ADDR Start of Descriptor List Contains the base address of the First Descriptor. It is a word (4 Byte) address.

7.2.6.27 0x0088 SMHC IDMAC Status Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: SMHC_IDST_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16:13	R	0x0	Reserved

Offset: 0x0088			Register Name: SMHC_IDST_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
12:10	R	0x0	IDMAC_ERR_STA Error Bits Indicates the type of error that caused a Bus Error. Valid only with Fatal Bus Error bit (IDST[2]) set. This field does not generate an interrupt. 001: Host Abort received during the transmission. 010: Host Abort received during the reception. Others: Reserved
9	R/W1C	0x0	ABN_INT_SUM (AIS) Abnormal Interrupt Summary Logical OR of the following: IDST[2]: Fatal Bus Interrupt IDST[4]: Descriptor Unavailable Bit Interrupt IDST[5]: Card Error Summary Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes AIS to be set is cleared.
8	R/W1C	0x0	NOR_INT_SUM (NIS) Normal Interrupt Summary Logical OR of the following: IDST[0]: Transmit Interrupt IDST[1]: Receive Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes NIS to be set is cleared.
7:6	/	/	/
5	R/W1C	0x0	ERR_FLAG_SUM Card Error Summary Indicates the status of the transaction to/from the card; also present in RINTSTS. Indicates the logical OR of the following bits: EBE: End Bit Error RTO: Response Timeout RCRC: Response CRC SBE: Start Bit Error DRTO: Data Read Timeout DCRC: Data CRC for Receive RE: Response Error Writing 1 clears this bit.

Offset: 0x0088			Register Name: SMHC_IDST_REG
Bit	Read/Write	Default/Hex	Description
4	R/W1C	0x0	DES_UNAVL_INT Descriptor Unavailable Interrupt This bit is set when the descriptor is unavailable due to OWN bit = 0 (DES0[31] =0). Writing 1 clears this bit.
3	/	/	/
2	R/W1C	0x0	FATAL_BERR_INT Fatal Bus Error Interrupt Indicates that a Bus Error occurred (IDST[12:10]). When this bit is set, the DMA disables all its bus accesses. Writing 1 clears this bit.
1	R/W1C	0x0	RX_INT Receive Interrupt Indicates the completion of data reception for a descriptor. Writing 1 clears this bit.
0	R/W1C	0x0	TX_INT Transmit Interrupt Indicates that data transmission is finished for a descriptor. Writing 1 clears this bit.

7.2.6.28 0x008C SMHC IDMAC Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: SMHC_IDIE_REG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	ERR_SUM_INT_ENB Card Error Summary Interrupt Enable. When set, it enables the Card Interrupt Summary.
4	R/W	0x0	DES_UNAVL_INT_ENB Descriptor Unavailable Interrupt. When set along with Abnormal Interrupt Summary Enable, the Descriptor Unavailable Interrupt is enabled.
3	/	/	/

Offset: 0x008C			Register Name: SMHC_IDIE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
2	R/W	0x0	FERR_INT_ENB Fatal Bus Error Enable When set with Abnormal Interrupt Summary Enable, the Fatal Bus Error Interrupt is enabled. When reset, the Fatal Bus Error Enable Interrupt is disabled.
1	R/W	0x0	RX_INT_ENB Receive Interrupt Enable. When set with Normal Interrupt Summary Enable, Receive Interrupt is enabled. When reset, the Receive Interrupt is disabled.
0	R/W	0x0	TX_INT_ENB Transmit Interrupt Enable. When set with Normal Interrupt Summary Enable, Transmit Interrupt is enabled. When reset, the Transmit Interrupt is disabled.

7.2.6.29 0x0100 SMHC Card Threshold Control Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: SMHC_THLD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	CARD_WR_THLD Card Read/Write Threshold Size
15:3	/	/	/
2	R/W	0x0	CARD_WR_THLD_ENB Card Write Threshold Enable 0: Card write threshold disabled 1: Card write threshold enabled Host controller initiates write transfer only if the card threshold amount of data is available in transmit FIFO.
1	R/W	0x0	BCIG Busy Clear Interrupt Generation 0: Busy clear interrupt disabled 1: Busy clear interrupt enabled The application can disable this feature if it does not want to wait for a Busy Clear Interrupt.

Offset: 0x0100			Register Name: SMHC_THLD
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	CARD_RD_THLD_ENB Card Read Threshold Enable 0: Card read threshold disabled 1: Card read threshold enabled Host controller initiates Read Transfer only if the CARD_RD_THLD amount of space is available in receive FIFO.

7.2.6.30 0x0104 SMHC Sample FIFO Control Register (Default Value: 0x0000_0006)

Offset: 0x0104			Register Name: SMHC_SFC
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4:1	R/W	0x3	STOP_CLK_CTRL Stop Clock Control When receiving data, if CARD_RD_THLD_ENB is set and CARD_RD_THLD is set the same with BLK_SZ, the device clock may stop at the block gap during data receiving. This field is used to control the position of the stopping clock. The value can be changed between 0x0 and 0xF, but actually, the available value and the position of the stopping clock must be decided by the actual situation. The value increases one in this field is linked to one cycle (two cycles in DDR mode) that the position of the stopping clock moved up.
0	R/W	0x0	BYPASS_EN Bypass enable When set, sample FIFO will be bypassed.

7.2.6.31 0x0108 SMHC Auto Command 23 Argument Register (Default Value: 0x0000_0000)

Offset: 0x0108			Register Name: SMHC_A23A
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	A23A Auto CMD23 Argument The argument of command 23 is automatically sent by controller with this field.

7.2.6.32 0x010C SMHC eMMC4.5 DDR Start Bit Detection Control Register (Default Value: 0x0000_0000)

Offset: 0x010C			Register Name: EMMC_DDR_SBIT_DET
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HS400_MD_EN HS400 Mode Enable 0: Disabled 1: Enabled It is required to set this bit to '1' before initiating any data transfer CMD in HS400 mode.
30:1	/	/	/
0	R/W	0x0	HALF_START_BIT Control for start bit detection mechanism inside mstorage based on duration of start bit. For eMMC 4.5, start bit can be: 0: Full cycle 1: Less than one full cycle Set HALF_START_BIT = 1 for eMMC 4.5 and above; set to 0 for SD applications.

7.2.6.33 0x0138 SMHC Extended Command Register (Default Value: 0x0000_0000)

Offset: 0x0138			Register Name: SMHC_EXT_CMD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	AUTO_CMD23_EN Send CMD23 Automatically When setting this bit, send CMD23 automatically before sending the command specified in the SMHC_CMD register. When SOFT_RST is set, this field will be cleared.

7.2.6.34 0x013C SMHC Extended Response Register (Default Value: 0x0000_0000)

Offset: 0x013C			Register Name: SMHC_EXT_RESP
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	SMHC_EXT_RESP When AUTO_CMD23_EN is set, this register stores the response of CMD23.

7.2.6.35 0x0140 SMHC Drive Delay Control Register (Default Value: 0x0001_0000)

Offset: 0x0140			Register Name: SMHC_DRV_DL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x0	DAT_DRV_PH_SEL Data Drive Phase Select **When 0x005C[31]=0:** 0: Data drive phase offset is 90° at SDR mode, 45° at DDR8 mode, and 90° at DDR4 mode. 1: Data drive phase offset is 180° at SDR mode, 90° at DDR8 mode, and 0° at DDR4 mode. **When 0x005C[31]=1:** 0: Data drive phase offset is 90° at SDR mode, and 45° at DDR mode. 1: Data drive phase offset is 180° at SDR mode, and 90° at DDR mode.
16	R/W	0x1	CMD_DRV_PH_SEL Command Drive Phase Select **When 0x005C[31]=0:** 0: Command drive phase offset is 90° at SDR mode, 45° at DDR8 mode, and 90° at DDR4 mode. 1: Command drive phase offset is 180° at SDR mode, 90° at DDR8 mode, and 180° at DDR4 mode. **When 0x005C[31]=1:** 0: Command drive phase offset is 90° at SDR mode and 45° at DDR mode. 1: Command drive phase offset is 180° at SDR mode and 90° at DDR mode.
15:0	/	/	/

7.2.6.36 0x0144 SMHC Sample Delay Control Register (Default Value: 0x0000_2000)

Offset: 0x0144			Register Name: SMHC_SAMP_DL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	SAMP_DL_CAL_START Sample Delay Calibration Start When set, it means that start sample delay chain calibration.
14	R	0x0	SAMP_DL_CAL_DONE Sample Delay Calibration Done When set, it means that sample delay chain calibration is done and the result of calibration is shown in SAMP_DL.
13:8	R	0x20	SAMP_DL Sample Delay It indicates the number of delay cells corresponding to the current card clock. The delay time generated by these delay cells is equal to the cycle of the card clock nearly. Generally, it is necessary to do drive delay calibration when the card clock is changed. This bit is valid only when SAMP_DL_CAL_DONE is set.
7	R/W	0x0	SAMP_DL_SW_EN Sample Delay Software Enable When set, it means that enable the sample delay specified at SAMP_DL_SW.
6	/	/	/
5:0	R/W	0x0	SAMP_DL_SW Sample Delay Software The relative delay between the clock line and command line, data line. It can be determined according to the value of SAMP_DL, the cycle of the card clock and the input timing requirement of the device.

7.2.6.37 0x0148 SMHC Data Strobe Delay Control Register (Default Value: 0x0000_2000)

Offset: 0x0148			Register Name: SMHC_DS_DL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/

Offset: 0x0148			Register Name: SMHC_DS_DL
Bit	**Read/Write**	**Default/Hex**	**Description**
15	R/W	0x0	DS_DL_CAL_START Data Strobe Delay Calibration Start When set, it means that start sample delay chain calibration.
14	R	0x0	DS_DL_CAL_DONE Data Strobe Delay Calibration Done When set, it means that sample delay chain calibration is done and the result of calibration is shown in DS_DL.
13:8	R	0x20	DS_DL Data Strobe Delay It indicates the number of delay cells corresponding to the current card clock. The delay time generated by these delay cells is equal to the cycle of SMHC's clock nearly. This bit is valid only when SAMP_DL_CAL_DONE is set.
7	R/W	0x0	DS_DL_SW_EN Sample Delay Software Enable
6	/	/	/
5:0	R/W	0x0	DS_DL_SW Data Strobe Delay Software

7.2.6.38 0x014C SMHC HS400 New Timing Delay Control Register (Default Value: 0x0000_8000)

Offset: 0x014C			Register Name: SMHC_HS400_DL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	HS400_DL_CAL_START HS400 Delay Calibration Start When set, it means that start sample delay chain calibration.
14	R	0x0	HS400_DL_CAL_DONE HS400 Delay Calibration Done When set, it means that sample delay chain calibration is done and the result of calibration is shown in HS400_DL.
13:12	/	/	/

Offset: 0x014C			Register Name: SMHC_HS400_DL
Bit	**Read/Write**	**Default/Hex**	**Description**
11:8	R	0x8	HS400_DL HS400 Delay It indicates the number of delay cells corresponding to the current card clock. The delay time generated by these delay cells is equal to the cycle of the SMHC clock nearly. This bit is valid only when HS400_DL_CAL_DONE is set.
7	R/W	0x0	HS400_DL_SW_EN Sample Delay Software Enable
6	/	/	/
3:0	R/W	0x0	HS400_DL_SW HS400 Delay Software

7.2.6.39 0x0200 SMHC FIFO Register (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: SMHC_FIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TX/RX_FIFO Data FIFO

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8.1 I2S/PCM

8.1.1 Overview

The I2S/PCM controller is designed to transfer streaming audio-data between the system memory and the codec chip. The controller supports standard I2S format, Left-justified mode format, Right-justified mode format, PCM mode format, and TDM mode format.

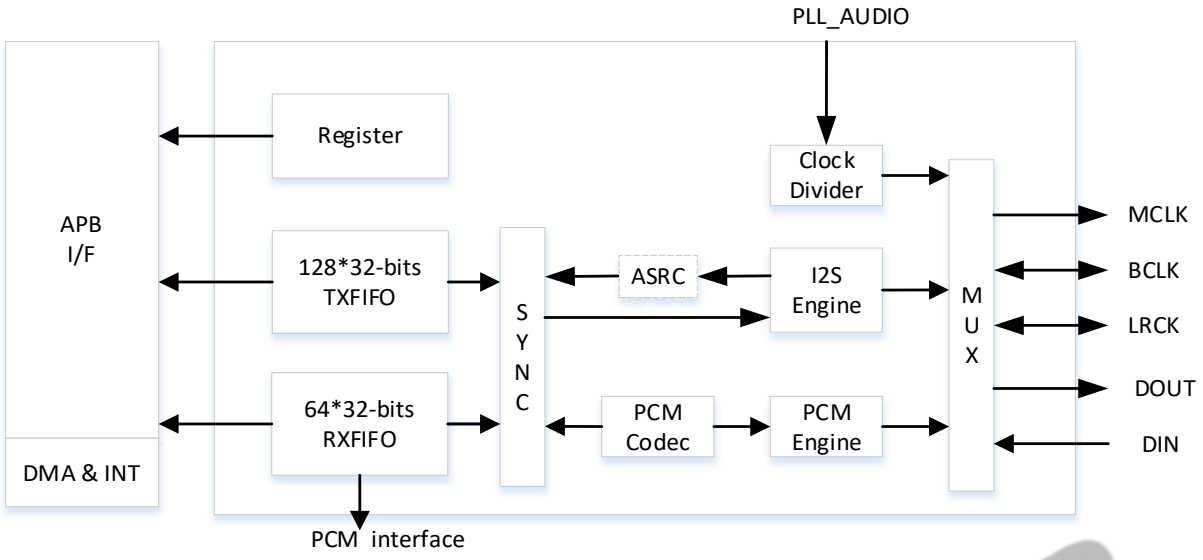
The I2S/PCM controller includes the following features:

- Two I2S/PCM external interfaces (I2S1, I2S2) for connecting external power amplifier and MIC ADC
- Compliant with standard Philips Inter-IC sound (I2S) bus specification
  - Left-justified, Right-justified, PCM mode, and Time Division Multiplexing (TDM) format
  - Programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)
- Transmit and Receive data FIFOs
  - Programmable FIFO thresholds
  - 128 depth x 32-bit width TXFIFO and 64 depth x 32-bit width RXFIFO
- Supports multiple function clock
  - Clock up to 24.576 MHz Data Output of I2S/PCM in Master mode (Only if the IO PAD and Peripheral I2S/PCM satisfy Timing Parameters)
  - Clock up to 12.288 MHz Data Input of I2S/PCM in Master mode
- Supports TX/RX DMA Slave interface
- Supports multiple application scenarios
  - Up to 16 channels (fs = 48 kHz) which has adjustable width from 8-bit to 32-bit
  - Sample rate from 8 kHz to 384 kHz (CHAN = 2)
  - 8-bit u-law and 8-bit A-law companded sample
- Supports master/slave mode

8.1.2 Block Diagram

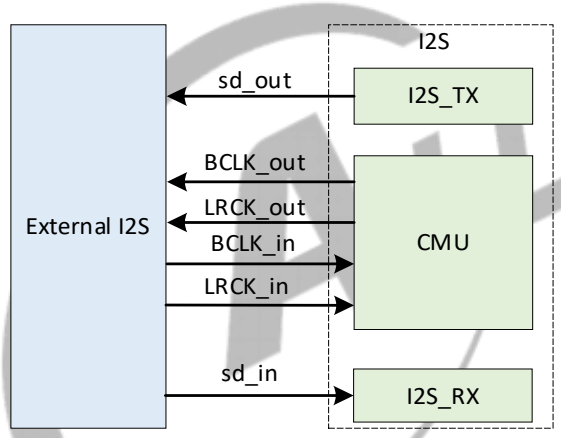
The following figure shows the functional block diagram of the I2S/PCM interface.

Figure 8-1 I2S/PCM Interface System Block Diagram



The following figure shows the typical application of the I2S/PCM interface.

Figure 8-2 Typical Application of I2S/PCM Interface



The I2S/PCM interface system integrates one I2S_TX and one I2S_RX.

- The I2S_TX is for playing music in I2S or PCM format.
- The I2S_RX is for receiving data in I2S or PCM format.
- When the I2S works in the master mode, the external I2S module provides BCLK_in and LRCK_in for the clock management unit (CMU), and the I2S_TX and I2S_RX work with the two external clocks.
- When the I2S works in the slave mode, the CMU provides clocks BCLK_out and LRCK_out for the external I2S module, and the I2S_TX and I2S_RX work with the internal clocks.