SSD202D
INTR_CPUINT Module Description

1. REGISTER DESCRIPTION

1.1. INTR_CPUINT Register (Bank = 1008)

INTR_CPUINT Register (Bank = 1008)				
Index (Absolute)	Mnemonic	Bit	Description	
20h (100840h)	REG100840	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	HST0TO3_INT	2	Host0 to Host3 interrupt.	
	HST0TO2_INT	1	Host0 to Host2 interrupt.	
	HST0TO1_INT	0	Host0 to Host1 interrupt.	
22h (100844h)	REG100844	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	HST1TO3_INT	2	Host1 to Host3 interrupt.	
	HST1TO2_INT	1	Host1 to Host2 interrupt.	
	HST1TO0_INT	0	Host1 to Host0 interrupt.	
24h (100848h)	REG100848	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	HST2TO3_INT	2	Host2 to Host3 interrupt.	
	HST2TO1_INT	1	Host2 to Host1 interrupt.	
	HST2TO0_INT	0	Host2 to Host0 interrupt.	
26h (10084Ch)	REG10084C	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	HST3TO2_INT	2	Host3 to Host2 interrupt.	
	HST3TO1_INT	1	Host3 to Host1 interrupt.	
	HST3TO0_INT	0	Host3 to Host0 interrupt.	
28h (100850h)	REG100850	7:0	Default : 0x00	Access : RO
	HST0_FIQ_STATUS_GROUP [7:0]	7:0	Bit0 => OR (Host0 FIQ final status[7:0]). Bit1 => OR (Host0 FIQ final status[15:8]). ..... Bit7 => OR (Host0 FIQ final status[63: 56]).	
28h (100851h)	REG100851	7:0	Default : 0x00	Access : RO
	HST0_IRQ_STATUS_GROUP [7:0]	7:0	Bit0 => OR (Host0 IRQ final status[7:0]). Bit1 => OR (Host0 IRQ final status[15:8]).	

INTR_CPUINT Register (Bank = 1008)			
Index (Absolute)	Mnemonic	Bit	Description
			..... Bit7 => OR (Host0 IRQ final status[63: 56]).
29h (100852h)	REG100852	7:0	Default : 0x00 Access : RO
	HST1_FIQ_STATUS_GROUP [7:0]	7:0	Bit0 => OR (Host1 FIQ final status[7:0]). Bit1 => OR (Host1 FIQ final status[15:8]). ..... Bit7 => OR (Host1 FIQ final status[63: 56]).
29h (100853h)	REG100853	7:0	Default : 0x00 Access : RO
	HST1_IRQ_STATUS_GROUP [7:0]	7:0	Bit0 => OR (Host1 IRQ final status[7:0]). Bit1 => OR (Host1 IRQ final status[15:8]). ..... Bit7 => OR (Host1 IRQ final status[63: 56]).
2Ah (100854h)	REG100854	7:0	Default : 0x00 Access : RO
	HST2_FIQ_STATUS_GROUP [7:0]	7:0	Bit0 => OR (Host2 FIQ final status[7:0]). Bit1 => OR (Host2 FIQ final status[15:8]). ..... Bit7 => OR (Host2 FIQ final status[63: 56]).
2Ah (100855h)	REG100855	7:0	Default : 0x00 Access : RO
	HST2_IRQ_STATUS_GROUP [7:0]	7:0	Bit0 => OR (Host2 IRQ final status[7:0]). Bit1 => OR (Host2 IRQ final status[15:8]). ..... Bit7 => OR (Host2 IRQ final status[63: 56]).
2Bh (100856h)	REG100856	7:0	Default : 0x00 Access : RO
	HST3_FIQ_STATUS_GROUP [7:0]	7:0	Bit0 => OR (Host3 FIQ final status[7:0]). Bit1 => OR (Host3 FIQ final status[15:8]). ..... Bit7 => OR (Host3 FIQ final status[63: 56]).
2Bh (100857h)	REG100857	7:0	Default : 0x00 Access : RO
	HST3_IRQ_STATUS_GROUP [7:0]	7:0	Bit0 => OR (Host3 IRQ final status[7:0]). Bit1 => OR (Host3 IRQ final status[15:8]). ..... Bit7 => OR (Host3 IRQ final status[63: 56]).