SSD202D
GPI_INT Module Description

1. REGISTER DESCRIPTION

1.1. GPI_INT Register (Bank = 103D)

GPI_INT Register (Bank = 103D)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (103D00h)	REG103D00	7:0	Default : 0xFF	Access : R/W
	FIQ_MASK_0[7:0]	7:0	Fiq mask enable.	
00h (103D01h)	REG103D01	7:0	Default : 0xFF	Access : R/W
	FIQ_MASK_0[15:8]	7:0	See description of '103D00h'.	
01h (103D02h)	REG103D02	7:0	Default : 0xFF	Access : R/W
	FIQ_MASK_1[7:0]	7:0	Fiq mask enable.	
01h (103D03h)	REG103D03	7:0	Default : 0xFF	Access : R/W
	FIQ_MASK_1[15:8]	7:0	See description of '103D02h'.	
02h (103D04h)	REG103D04	7:0	Default : 0xFF	Access : R/W
	FIQ_MASK_2[7:0]	7:0	Fiq mask enable.	
02h (103D05h)	REG103D05	7:0	Default : 0xFF	Access : R/W
	FIQ_MASK_2[15:8]	7:0	See description of '103D04h'.	
03h (103D06h)	REG103D06	7:0	Default : 0xFF	Access : R/W
	FIQ_MASK_3[7:0]	7:0	Fiq mask enable.	
03h (103D07h)	REG103D07	7:0	Default : 0xFF	Access : R/W
	FIQ_MASK_3[15:8]	7:0	See description of '103D06h'.	
04h (103D08h)	REG103D08	7:0	Default : 0xFF	Access : R/W
	FIQ_MASK_4[7:0]	7:0	Fiq mask enable.	
04h (103D09h)	REG103D09	7:0	Default : 0x0F	Access : R/W
	-	7:4	Reserved.	
	FIQ_MASK_4[11: 8]	3:0	See description of '103D08h'.	
05h (103D0Ah)	REG103D0A	7:0	Default : 0x00	Access : R/W
	FIQ_FORCE[7:0]	7:0	Fiq force enable.	
05h (103D0Bh)	REG103D0B	7:0	Default : 0x00	Access : R/W
	FIQ_FORCE[15:8]	7:0	See description of '103D0Ah'.	
06h (103D0Ch)	REG103D0C	7:0	Default : 0x00	Access : R/W
	FIQ_FORCE[23:16]	7:0	See description of '103D0Ah'.	

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06h (103D0Dh)	REG103D0D	7:0	Default : 0x00	Access : R/W
	FIQ_FORCE[31:24]	7:0	See description of '103D0Ah'.	
07h (103D0Eh)	REG103D0E	7:0	Default : 0x00	Access : R/W
	FIQ_FORCE[39: 32]	7:0	See description of '103D0Ah'.	
07h (103D0Fh)	REG103D0F	7:0	Default : 0x00	Access : R/W
	FIQ_FORCE[47:40]	7:0	See description of '103D0Ah'.	
08h (103D10h)	REG103D10	7:0	Default : 0x00	Access : R/W
	FIQ_FORCE[55:48]	7:0	See description of '103D0Ah'.	
08h (103D11h)	REG103D11	7:0	Default : 0x00	Access : R/W
	FIQ_FORCE[63: 56]	7:0	See description of '103D0Ah'.	
09h (103D12h)	REG103D12	7:0	Default : 0x00	Access : R/W
	FIQ_FORCE[71: 64]	7:0	See description of '103D0Ah'.	
09h (103D13h)	REG103D13	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	FIQ_FORCE[75: 72]	3:0	See description of '103D0Ah'.	
0Ah (103D14h)	REG103D14	7:0	Default : 0x00	Access : WO
	FIQ_CLR[7:0]	7:0	Fiq clear.	
0Ah (103D15h)	REG103D15	7:0	Default : 0x00	Access : WO
	FIQ_CLR[15:8]	7:0	See description of '103D14h'.	
0Bh (103D16h)	REG103D16	7:0	Default : 0x00	Access : WO
	FIQ_CLR[23:16]	7:0	See description of '103D14h'.	
0Bh (103D17h)	REG103D17	7:0	Default : 0x00	Access : WO
	FIQ_CLR[31:24]	7:0	See description of '103D14h'.	
0Ch (103D18h)	REG103D18	7:0	Default : 0x00	Access : WO
	FIQ_CLR[39: 32]	7:0	See description of '103D14h'.	
0Ch (103D19h)	REG103D19	7:0	Default : 0x00	Access : WO
	FIQ_CLR[47:40]	7:0	See description of '103D14h'.	
0Dh (103D1Ah)	REG103D1A	7:0	Default : 0x00	Access : WO
	FIQ_CLR[55:48]	7:0	See description of '103D14h'.	
0Dh (103D1Bh)	REG103D1B	7:0	Default : 0x00	Access : WO
	FIQ_CLR[63: 56]	7:0	See description of '103D14h'.	
0Eh (103D1Ch)	REG103D1C	7:0	Default : 0x00	Access : WO
	FIQ_CLR[71: 64]	7:0	See description of '103D14h'.	

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0Eh (103D1Dh)	REG103D1D	7:0	Default : 0x00	Access : WO
	-	7:4	Reserved.	
	FIQ_CLR[75: 72]	3:0	See description of '103D14h'.	
10h (103D20h)	REG103D20	7:0	Default : 0x00	Access : R/W
	FIQ_POL[7:0]	7:0	Fiq polarity.	
10h (103D21h)	REG103D21	7:0	Default : 0x00	Access : R/W
	FIQ_POL[15:8]	7:0	See description of '103D20h'.	
11h (103D22h)	REG103D22	7:0	Default : 0x00	Access : R/W
	FIQ_POL[23:16]	7:0	See description of '103D20h'.	
11h (103D23h)	REG103D23	7:0	Default : 0x00	Access : R/W
	FIQ_POL[31:24]	7:0	See description of '103D20h'.	
12h (103D24h)	REG103D24	7:0	Default : 0x00	Access : R/W
	FIQ_POL[39: 32]	7:0	See description of '103D20h'.	
12h (103D25h)	REG103D25	7:0	Default : 0x00	Access : R/W
	FIQ_POL[47:40]	7:0	See description of '103D20h'.	
13h (103D26h)	REG103D26	7:0	Default : 0x00	Access : R/W
	FIQ_POL[55:48]	7:0	See description of '103D20h'.	
13h (103D27h)	REG103D27	7:0	Default : 0x00	Access : R/W
	FIQ_POL[63: 56]	7:0	See description of '103D20h'.	
14h (103D28h)	REG103D28	7:0	Default : 0x00	Access : R/W
	FIQ_POL[71: 64]	7:0	See description of '103D20h'.	
14h (103D29h)	REG103D29	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	FIQ_POL[75: 72]	3:0	See description of '103D20h'.	
15h (103D2Ah)	REG103D2A	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	FIQ_RAW_SEL	0	Fiq raw status select.	
20h (103D40h)	REG103D40	7:0	Default : 0xFF	Access : R/W
	IRQ_MASK[7:0]	7:0	Irq mask enable.	
21h (103D42h)	REG103D42	7:0	Default : 0xFF	Access : R/W
	IRQ_FORCE[7:0]	7:0	Irq force enable.	
22h (103D44h)	REG103D44	7:0	Default : 0xFF	Access : R/W
	IRQ_POL[7:0]	7:0	Irq polarity.	

GPI_INT Register (Bank = 103D)				
Index (Absolute)	Mnemonic	Bit	Description	
30h (103D60h)	REG103D60	7:0	Default : 0x00	Access : RO
	FIQ_FINAL_STATUS[7:0]	7:0	FIQ_FINAL_STATUS.	
30h (103D61h)	REG103D61	7:0	Default : 0x00	Access : RO
	FIQ_FINAL_STATUS[15:8]	7:0	See description of '103D60h'.	
31h (103D62h)	REG103D62	7:0	Default : 0x00	Access : RO
	FIQ_FINAL_STATUS[23:16]	7:0	See description of '103D60h'.	
31h (103D63h)	REG103D63	7:0	Default : 0x00	Access : RO
	FIQ_FINAL_STATUS[31:24]	7:0	See description of '103D60h'.	
32h (103D64h)	REG103D64	7:0	Default : 0x00	Access : RO
	FIQ_FINAL_STATUS[39:32]	7:0	See description of '103D60h'.	
32h (103D65h)	REG103D65	7:0	Default : 0x00	Access : RO
	FIQ_FINAL_STATUS[47:40]	7:0	See description of '103D60h'.	
33h (103D66h)	REG103D66	7:0	Default : 0x00	Access : RO
	FIQ_FINAL_STATUS[55:48]	7:0	See description of '103D60h'.	
33h (103D67h)	REG103D67	7:0	Default : 0x00	Access : RO
	FIQ_FINAL_STATUS[63:56]	7:0	See description of '103D60h'.	
34h (103D68h)	REG103D68	7:0	Default : 0x00	Access : RO
	FIQ_FINAL_STATUS[71:64]	7:0	See description of '103D60h'.	
34h (103D69h)	REG103D69	7:0	Default : 0x00	Access : RO
	-	7:4	Reserved.	
	FIQ_FINAL_STATUS[75:72]	3:0	See description of '103D60h'.	
35h (103D6Ah)	REG103D6A	7:0	Default : 0x00	Access : RO
	FIQ_RAW_STATUS[7:0]	7:0	FIQ_RAW_STATUS.	
35h (103D6Bh)	REG103D6B	7:0	Default : 0x00	Access : RO
	FIQ_RAW_STATUS[15:8]	7:0	See description of '103D6Ah'.	
36h (103D6Ch)	REG103D6C	7:0	Default : 0x00	Access : RO
	FIQ_RAW_STATUS[23:16]	7:0	See description of '103D6Ah'.	
36h (103D6Dh)	REG103D6D	7:0	Default : 0x00	Access : RO
	FIQ_RAW_STATUS[31:24]	7:0	See description of '103D6Ah'.	
37h	REG103D6E	7:0	Default : 0x00	Access : RO

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Index (Absolute)	Mnemonic	Bit	Description	
(103D6Eh)	FIQ_RAW_STATUS[39: 32]	7:0	See description of '103D6Ah'.	
37h (103D6Fh)	REG103D6F	7:0	Default : 0x00	Access : RO
	FIQ_RAW_STATUS[47:40]	7:0	See description of '103D6Ah'.	
38h (103D70h)	REG103D70	7:0	Default : 0x00	Access : RO
	FIQ_RAW_STATUS[55:48]	7:0	See description of '103D6Ah'.	
38h (103D71h)	REG103D71	7:0	Default : 0x00	Access : RO
	FIQ_RAW_STATUS[63: 56]	7:0	See description of '103D6Ah'.	
39h (103D72h)	REG103D72	7:0	Default : 0x00	Access : RO
	FIQ_RAW_STATUS[71: 64]	7:0	See description of '103D6Ah'.	
39h (103D73h)	REG103D73	7:0	Default : 0x00	Access : RO
	-	7:4	Reserved.	
	FIQ_RAW_STATUS[75: 72]	3:0	See description of '103D6Ah'.	
3Ah (103D74h)	REG103D74	7:0	Default : 0x00	Access : RO
	IRQ_FINAL_STATUS[7:0]	7:0	IRQ_FINAL_STATUS.	
3Bh (103D76h)	REG103D76	7:0	Default : 0x00	Access : RO
	IRQ_RAW_STATUS[7:0]	7:0	IRQ_RAW_STATUS.	
40h (103D80h)	REG103D80	7:0	Default : 0x00	Access : R/W
	GPI_GLHRM_EN[7:0]	7:0	Gpi glitch remove enable.	
40h (103D81h)	REG103D81	7:0	Default : 0x00	Access : R/W
	GPI_GLHRM_EN[15:8]	7:0	See description of '103D80h'.	
41h (103D82h)	REG103D82	7:0	Default : 0x00	Access : R/W
	GPI_GLHRM_EN[23:16]	7:0	See description of '103D80h'.	
41h (103D83h)	REG103D83	7:0	Default : 0x00	Access : R/W
	GPI_GLHRM_EN[31:24]	7:0	See description of '103D80h'.	
42h (103D84h)	REG103D84	7:0	Default : 0x00	Access : R/W
	GPI_GLHRM_EN[39: 32]	7:0	See description of '103D80h'.	
42h (103D85h)	REG103D85	7:0	Default : 0x00	Access : R/W
	GPI_GLHRM_EN[47:40]	7:0	See description of '103D80h'.	
43h (103D86h)	REG103D86	7:0	Default : 0x00	Access : R/W
	GPI_GLHRM_EN[55:48]	7:0	See description of '103D80h'.	
43h (103D87h)	REG103D87	7:0	Default : 0x00	Access : R/W
	GPI_GLHRM_EN[63: 56]	7:0	See description of '103D80h'.	
44h	REG103D88	7:0	Default : 0x00	Access : R/W

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(103D88h)	GPI_GLHRM_EN[71: 64]	7:0	See description of '103D80h'.	
44h (103D89h)	REG103D89	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	GPI_GLHRM_EN[75: 72]	3:0	See description of '103D80h'.	
45h (103D8Ah)	REG103D8A	7:0	Default : 0x00	Access : R/W
	GPI_GLHRM_NUM[7:0]	7:0	Gpi glitch remove number.	
45h (103D8Bh)	REG103D8B	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	GPI_GLHRM_NUM[10: 8]	2:0	See description of '103D8Ah'.	