SSD202D
INTR_CTRL Module Description

1. REGISTER DESCRIPTION

1.1. INTR_CTRL Register (Bank = 1009)

INTR_CTRL Register (Bank = 1009)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (100900h)	REG100900	7:0	Default : 0x00	Access : R/W
	HST0_FIQ_FORCE_15_0_[7:0]	7:0	Force to issue fiq interrupt[15:0] to hst0; 0/1 : not force/force.	
00h (100901h)	REG100901	7:0	Default : 0x00	Access : R/W
	HST0_FIQ_FORCE_15_0_[15:8]	7:0	See description of '100900h'.	
01h (100902h)	REG100902	7:0	Default : 0x00	Access : R/W
	HST0_FIQ_FORCE_31_16_[7:0]	7:0	Force to issue fiq interrupt[31:16] to hst0; 0/1 : not force/force.	
01h (100903h)	REG100903	7:0	Default : 0x00	Access : R/W
	HST0_FIQ_FORCE_31_16_[15:8]	7:0	See description of '100902h'.	
02h (100904h)	REG100904	7:0	Default : 0x00	Access : R/W
	HST0_FIQ_FORCE_47_32_[7:0]	7:0	Force to issue fiq interrupt[47:32] to hst0; 0/1 : not force/force.	
02h (100905h)	REG100905	7:0	Default : 0x00	Access : R/W
	HST0_FIQ_FORCE_47_32_[15:8]	7:0	See description of '100904h'.	
03h (100906h)	REG100906	7:0	Default : 0xFF	Access : R/W
	HST0_FIQ_FORCE_63_48_[7:0]	7:0	Force to issue fiq interrupt[63: 48] to hst0; 0/1 : not force/force.	
03h (100907h)	REG100907	7:0	Default : 0xFF	Access : R/W
	HST0_FIQ_FORCE_63_48_[15:8]	7:0	See description of '100906h'.	
04h (100908h)	REG100908	7:0	Default : 0xFF	Access : R/W
	HST0_FIQ_MASK_15_0_[7:0]	7:0	Mask fiq interrupt[15:0] for hst0; 0/1: not mask/mask.	
04h (100909h)	REG100909	7:0	Default : 0xFF	Access : R/W
	HST0_FIQ_MASK_15_0_[15	7:0	See description of '100908h'.	

INTR_CTRL Register (Bank = 1009)				
Index (Absolute)	Mnemonic	Bit	Description	
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05h (10090Ah)	REG10090A	7:0	Default : 0xFF	Access : R/W
	HST0_FIQ_MASK_31_16_[7:0]	7:0	Mask fiq interrupt[31:16] for hst0; 0/1: not mask/mask.	
05h (10090Bh)	REG10090B	7:0	Default : 0xFF	Access : R/W
	HST0_FIQ_MASK_31_16_[15:8]	7:0	See description of '10090Ah'.	
06h (10090Ch)	REG10090C	7:0	Default : 0xFF	Access : R/W
	HST0_FIQ_MASK_47_32_[7:0]	7:0	Mask fiq interrupt[47:32] for hst0; 0/1: not mask/mask.	
06h (10090Dh)	REG10090D	7:0	Default : 0xFF	Access : R/W
	HST0_FIQ_MASK_47_32_[15:8]	7:0	See description of '10090Ch'.	
07h (10090Eh)	REG10090E	7:0	Default : 0xFF	Access : R/W
	HST0_FIQ_MASK_63_48_[7:0]	7:0	Mask fiq interrupt[63: 48] for hst0; 0/1: not mask/mask.	
07h (10090Fh)	REG10090F	7:0	Default : 0xFF	Access : R/W
	HST0_FIQ_MASK_63_48_[15:8]	7:0	See description of '10090Eh'.	
08h (100910h)	REG100910	7:0	Default : 0x00	Access : R/W
	HST0_FIQ_POLARITY_15_0_[7:0]	7:0	Reverse fiq interrupt[15:0] polarity for hst0; 0/1: not reverse/reverse.	
08h (100911h)	REG100911	7:0	Default : 0x00	Access : R/W
	HST0_FIQ_POLARITY_15_0_[15:8]	7:0	See description of '100910h'.	
09h (100912h)	REG100912	7:0	Default : 0x00	Access : R/W
	HST0_FIQ_POLARITY_31_16_[7:0]	7:0	Reverse fiq interrupt[31:16] polarity for hst0; 0/1: not reverse/reverse.	
09h (100913h)	REG100913	7:0	Default : 0x00	Access : R/W
	HST0_FIQ_POLARITY_31_16_[15:8]	7:0	See description of '100912h'.	
0Ah (100914h)	REG100914	7:0	Default : 0x00	Access : R/W
	HST0_FIQ_POLARITY_47_32_[7:0]	7:0	Reverse fiq interrupt[47:32] polarity for hst0; 0/1: not reverse/reverse.	
0Ah	REG100915	7:0	Default : 0x00	Access : R/W

INTR_CTRL Register (Bank = 1009)				
Index (Absolute)	Mnemonic	Bit	Description	
(100915h)	HST0_FIQ_POLARITY_47_32_[15:8]	7:0	See description of '100914h'.	
0Bh (100916h)	REG100916	7:0	Default : 0x00	Access : R/W
	HST0_FIQ_POLARITY_63_48_[7:0]	7:0	Reverse fiq interrupt[63: 48] polarity for hst0; 0/1: not reverse/reverse.	
0Bh (100917h)	REG100917	7:0	Default : 0x00	Access : R/W
	HST0_FIQ_POLARITY_63_48_[15:8]	7:0	See description of '100916h'.	
0Ch (100918h)	REG100918	7:0	Default : 0x00	Access : R/W
	HST0_FIQ_STATUS_15_0_[7:0]	7:0	Read for the status of fiq interrupt[15:0] for hst0; Write 1 to clear fiq interrupt[15:0] of hst0.	
0Ch (100919h)	REG100919	7:0	Default : 0x00	Access : R/W
	HST0_FIQ_STATUS_15_0_[15:8]	7:0	See description of '100918h'.	
0Dh (10091Ah)	REG10091A	7:0	Default : 0x00	Access : R/W
	HST0_FIQ_STATUS_31_16_[7:0]	7:0	Read for the status of fiq interrupt[31:16] for hst0; Write 1 to clear fiq interrupt[31:16] of hst0.	
0Dh (10091Bh)	REG10091B	7:0	Default : 0x00	Access : R/W
	HST0_FIQ_STATUS_31_16_[15:8]	7:0	See description of '10091Ah'.	
0Eh (10091Ch)	REG10091C	7:0	Default : 0x00	Access : R/W
	HST0_FIQ_STATUS_47_32_[7:0]	7:0	Read for the status of fiq interrupt[47:32] for hst0; Write 1 to clear fiq interrupt[47:32] of hst0.	
0Eh (10091Dh)	REG10091D	7:0	Default : 0x00	Access : R/W
	HST0_FIQ_STATUS_47_32_[15:8]	7:0	See description of '10091Ch'.	
0Fh (10091Eh)	REG10091E	7:0	Default : 0x00	Access : R/W
	HST0_FIQ_STATUS_63_48_[7:0]	7:0	Read for the status of fiq interrupt[63: 48] for hst0; Write 1 to clear fiq interrupt[63: 48] of hst0.	
0Fh (10091Fh)	REG10091F	7:0	Default : 0x00	Access : R/W
	HST0_FIQ_STATUS_63_48_[15:8]	7:0	See description of '10091Eh'.	
10h (100920h)	REG100920	7:0	Default : 0x00	Access : R/W
	HST0_IRQ_FORCE_15_0_[7:0]	7:0	Force to issue irq interrupt[15:0] to hst0; 0/1 : not force/force.	

INTR_CTRL Register (Bank = 1009)				
Index (Absolute)	Mnemonic	Bit	Description	
10h (100921h)	REG100921	7:0	Default : 0x00	Access : R/W
	HST0_IRQ_FORCE_15_0_[15:8]	7:0	See description of '100920h'.	
11h (100922h)	REG100922	7:0	Default : 0x00	Access : R/W
	HST0_IRQ_FORCE_31_16_[7:0]	7:0	Force to issue irq interrupt[31:16] to hst0; 0/1 : not force/force.	
11h (100923h)	REG100923	7:0	Default : 0x00	Access : R/W
	HST0_IRQ_FORCE_31_16_[15:8]	7:0	See description of '100922h'.	
12h (100924h)	REG100924	7:0	Default : 0x00	Access : R/W
	HST0_IRQ_FORCE_47_32_[7:0]	7:0	Force to issue irq interrupt[47:32] to hst0; 0/1 : not force/force.	
12h (100925h)	REG100925	7:0	Default : 0x00	Access : R/W
	HST0_IRQ_FORCE_47_32_[15:8]	7:0	See description of '100924h'.	
13h (100926h)	REG100926	7:0	Default : 0xFF	Access : R/W
	HST0_IRQ_FORCE_63_48_[7:0]	7:0	Force to issue irq interrupt[63: 48] to hst0; 0/1 : not force/force.	
13h (100927h)	REG100927	7:0	Default : 0xFF	Access : R/W
	HST0_IRQ_FORCE_63_48_[15:8]	7:0	See description of '100926h'.	
14h (100928h)	REG100928	7:0	Default : 0xFF	Access : R/W
	HST0_IRQ_MASK_15_0_[7:0]	7:0	Mask irq interrupt[15:0] for hst0; 0/1: not mask/mask.	
14h (100929h)	REG100929	7:0	Default : 0xFF	Access : R/W
	HST0_IRQ_MASK_15_0_[15:8]	7:0	See description of '100928h'.	
15h (10092Ah)	REG10092A	7:0	Default : 0xFF	Access : R/W
	HST0_IRQ_MASK_31_16_[7:0]	7:0	Mask irq interrupt[31:16] for hst0; 0/1: not mask/mask.	
15h (10092Bh)	REG10092B	7:0	Default : 0xFF	Access : R/W
	HST0_IRQ_MASK_31_16_[15:8]	7:0	See description of '10092Ah'.	
16h (10092Ch)	REG10092C	7:0	Default : 0xFF	Access : R/W
	HST0_IRQ_MASK_47_32_[7	7:0	Mask irq interrupt[47:32] for hst0; 0/1: not mask/mask.	

INTR_CTRL Register (Bank = 1009)				
Index (Absolute)	Mnemonic	Bit	Description	
	:0]			
16h (10092Dh)	REG10092D	7:0	Default : 0xFF	Access : R/W
	HST0_IRQ_MASK_47_32_[15:8]	7:0	See description of '10092Ch'.	
17h (10092Eh)	REG10092E	7:0	Default : 0xFF	Access : R/W
	HST0_IRQ_MASK_63_48_[7:0]	7:0	Mask irq interrupt[63: 48] for hst0; 0/1: not mask/mask.	
17h (10092Fh)	REG10092F	7:0	Default : 0xFF	Access : R/W
	HST0_IRQ_MASK_63_48_[15:8]	7:0	See description of '10092Eh'.	
18h (100930h)	REG100930	7:0	Default : 0x00	Access : R/W
	HST0_IRQ_POLARITY_15_0_[7:0]	7:0	Reverse irq interrupt[15:0] polarity for hst0; 0/1: not reverse/reverse.	
18h (100931h)	REG100931	7:0	Default : 0x00	Access : R/W
	HST0_IRQ_POLARITY_15_0_[15:8]	7:0	See description of '100930h'.	
19h (100932h)	REG100932	7:0	Default : 0x00	Access : R/W
	HST0_IRQ_POLARITY_31_16_[7:0]	7:0	Reverse irq interrupt[31:16] polarity for hst0; 0/1: not reverse/reverse.	
19h (100933h)	REG100933	7:0	Default : 0x00	Access : R/W
	HST0_IRQ_POLARITY_31_16_[15:8]	7:0	See description of '100932h'.	
1Ah (100934h)	REG100934	7:0	Default : 0x00	Access : R/W
	HST0_IRQ_POLARITY_47_32_[7:0]	7:0	Reverse irq interrupt[47:32] polarity for hst0; 0/1: not reverse/reverse.	
1Ah (100935h)	REG100935	7:0	Default : 0x00	Access : R/W
	HST0_IRQ_POLARITY_47_32_[15:8]	7:0	See description of '100934h'.	
1Bh (100936h)	REG100936	7:0	Default : 0x00	Access : R/W
	HST0_IRQ_POLARITY_63_48_[7:0]	7:0	Reverse irq interrupt[63: 48] polarity for hst0; 0/1: not reverse/reverse.	
1Bh (100937h)	REG100937	7:0	Default : 0x00	Access : R/W
	HST0_IRQ_POLARITY_63_48_[15:8]	7:0	See description of '100936h'.	
1Ch	REG100938	7:0	Default : 0x00	Access : RO

INTR_CTRL Register (Bank = 1009)				
Index (Absolute)	Mnemonic	Bit	Description	
(100938h)	HST0_IRQ_STATUS_15_0_[7:0]	7:0	Read for the status of irq interrupt[15:0] for hst0;	
1Ch (100939h)	REG100939	7:0	Default : 0x00	Access : RO
	HST0_IRQ_STATUS_15_0_[15:8]	7:0	See description of '100938h'.	
1Dh (10093Ah)	REG10093A	7:0	Default : 0x00	Access : RO
	HST0_IRQ_STATUS_31_16_[7:0]	7:0	Read for the status of irq interrupt[31:16] for hst0;	
1Dh (10093Bh)	REG10093B	7:0	Default : 0x00	Access : RO
	HST0_IRQ_STATUS_31_16_[15:8]	7:0	See description of '10093Ah'.	
1Eh (10093Ch)	REG10093C	7:0	Default : 0x00	Access : RO
	HST0_IRQ_STATUS_47_32_[7:0]	7:0	Read for the status of irq interrupt[47:32] for hst0;	
1Eh (10093Dh)	REG10093D	7:0	Default : 0x00	Access : RO
	HST0_IRQ_STATUS_47_32_[15:8]	7:0	See description of '10093Ch'.	
1Fh (10093Eh)	REG10093E	7:0	Default : 0x00	Access : RO
	HST0_IRQ_STATUS_63_48_[7:0]	7:0	Read for the status of irq interrupt[63: 48] for hst0;	
1Fh (10093Fh)	REG10093F	7:0	Default : 0x00	Access : RO
	HST0_IRQ_STATUS_63_48_[15:8]	7:0	See description of '10093Eh'.	
20h (100940h)	REG100940	7:0	Default : 0x00	Access : R/W
	HST1_FIQ_FORCE_15_0_[7:0]	7:0	Force to issue fiq interrupt[15:0] to hst1; 0/1 : not force/force.	
20h (100941h)	REG100941	7:0	Default : 0x00	Access : R/W
	HST1_FIQ_FORCE_15_0_[15:8]	7:0	See description of '100940h'.	
21h (100942h)	REG100942	7:0	Default : 0x00	Access : R/W
	HST1_FIQ_FORCE_31_16_[7:0]	7:0	Force to issue fiq interrupt[31:16] to hst1; 0/1 : not force/force.	
21h (100943h)	REG100943	7:0	Default : 0x00	Access : R/W
	HST1_FIQ_FORCE_31_16_[15:8]	7:0	See description of '100942h'.	

INTR_CTRL Register (Bank = 1009)				
Index (Absolute)	Mnemonic	Bit	Description	
22h (100944h)	REG100944	7:0	Default : 0x00	Access : R/W
	HST1_FIQ_FORCE_47_32_[7:0]	7:0	Force to issue fiq interrupt[47:32] to hst1; 0/1 : not force/force.	
22h (100945h)	REG100945	7:0	Default : 0x00	Access : R/W
	HST1_FIQ_FORCE_47_32_[15:8]	7:0	See description of '100944h'.	
23h (100946h)	REG100946	7:0	Default : 0xFF	Access : R/W
	HST1_FIQ_FORCE_63_48_[7:0]	7:0	Force to issue fiq interrupt[63: 48] to hst1; 0/1 : not force/force.	
23h (100947h)	REG100947	7:0	Default : 0xFF	Access : R/W
	HST1_FIQ_FORCE_63_48_[15:8]	7:0	See description of '100946h'.	
24h (100948h)	REG100948	7:0	Default : 0xFF	Access : R/W
	HST1_FIQ_MASK_15_0_[7:0]	7:0	Mask fiq interrupt[15:0] for hst1; 0/1: not mask/mask.	
24h (100949h)	REG100949	7:0	Default : 0xFF	Access : R/W
	HST1_FIQ_MASK_15_0_[15:8]	7:0	See description of '100948h'.	
25h (10094Ah)	REG10094A	7:0	Default : 0xFF	Access : R/W
	HST1_FIQ_MASK_31_16_[7:0]	7:0	Mask fiq interrupt[31:16] for hst1; 0/1: not mask/mask.	
25h (10094Bh)	REG10094B	7:0	Default : 0xFF	Access : R/W
	HST1_FIQ_MASK_31_16_[15:8]	7:0	See description of '10094Ah'.	
26h (10094Ch)	REG10094C	7:0	Default : 0xFF	Access : R/W
	HST1_FIQ_MASK_47_32_[7:0]	7:0	Mask fiq interrupt[47:32] for hst1; 0/1: not mask/mask.	
26h (10094Dh)	REG10094D	7:0	Default : 0xFF	Access : R/W
	HST1_FIQ_MASK_47_32_[15:8]	7:0	See description of '10094Ch'.	
27h (10094Eh)	REG10094E	7:0	Default : 0xFF	Access : R/W
	HST1_FIQ_MASK_63_48_[7:0]	7:0	Mask fiq interrupt[63: 48] for hst1; 0/1: not mask/mask.	
27h (10094Fh)	REG10094F	7:0	Default : 0xFF	Access : R/W
	HST1_FIQ_MASK_63_48_[1	7:0	See description of '10094Eh'.	

INTR_CTRL Register (Bank = 1009)				
Index (Absolute)	Mnemonic	Bit	Description	
	5:8]			
28h (100950h)	REG100950	7:0	Default : 0x00	Access : R/W
	HST1_FIQ_POLARITY_15_0_[7:0]	7:0	Reverse fiq interrupt[15:0] polarity for hst1; 0/1: not reverse/reverse.	
28h (100951h)	REG100951	7:0	Default : 0x00	Access : R/W
	HST1_FIQ_POLARITY_15_0_[15:8]	7:0	See description of '100950h'.	
29h (100952h)	REG100952	7:0	Default : 0x00	Access : R/W
	HST1_FIQ_POLARITY_31_16_[7:0]	7:0	Reverse fiq interrupt[31:16] polarity for hst1; 0/1: not reverse/reverse.	
29h (100953h)	REG100953	7:0	Default : 0x00	Access : R/W
	HST1_FIQ_POLARITY_31_16_[15:8]	7:0	See description of '100952h'.	
2Ah (100954h)	REG100954	7:0	Default : 0x00	Access : R/W
	HST1_FIQ_POLARITY_47_32_[7:0]	7:0	Reverse fiq interrupt[47:32] polarity for hst1; 0/1: not reverse/reverse.	
2Ah (100955h)	REG100955	7:0	Default : 0x00	Access : R/W
	HST1_FIQ_POLARITY_47_32_[15:8]	7:0	See description of '100954h'.	
2Bh (100956h)	REG100956	7:0	Default : 0x00	Access : R/W
	HST1_FIQ_POLARITY_63_48_[7:0]	7:0	Reverse fiq interrupt[63: 48] polarity for hst1; 0/1: not reverse/reverse.	
2Bh (100957h)	REG100957	7:0	Default : 0x00	Access : R/W
	HST1_FIQ_POLARITY_63_48_[15:8]	7:0	See description of '100956h'.	
2Ch (100958h)	REG100958	7:0	Default : 0x00	Access : R/W
	HST1_FIQ_STATUS_15_0_[7:0]	7:0	Read for the status of fiq interrupt[15:0] for hst1; Write 1 to clear fiq interrupt[15:0] of hst1.	
2Ch (100959h)	REG100959	7:0	Default : 0x00	Access : R/W
	HST1_FIQ_STATUS_15_0_[15:8]	7:0	See description of '100958h'.	
2Dh (10095Ah)	REG10095A	7:0	Default : 0x00	Access : R/W
	HST1_FIQ_STATUS_31_16_[7:0]	7:0	Read for the status of fiq interrupt[31:16] for hst1; Write 1 to clear fiq interrupt[31:16] of hst1.	
2Dh	REG10095B	7:0	Default : 0x00	Access : R/W

INTR_CTRL Register (Bank = 1009)			
Index (Absolute)	Mnemonic	Bit	Description
(10095Bh)	HST1_FIQ_STATUS_31_16_[15:8]	7:0	See description of '10095Ah'.
2Eh (10095Ch)	REG10095C	7:0	Default : 0x00 Access : R/W
	HST1_FIQ_STATUS_47_32_[7:0]	7:0	Read for the status of fiq interrupt[47:32] for hst1; Write 1 to clear fiq interrupt[47:32] of hst1.
2Eh (10095Dh)	REG10095D	7:0	Default : 0x00 Access : R/W
	HST1_FIQ_STATUS_47_32_[15:8]	7:0	See description of '10095Ch'.
2Fh (10095Eh)	REG10095E	7:0	Default : 0x00 Access : R/W
	HST1_FIQ_STATUS_63_48_[7:0]	7:0	Read for the status of fiq interrupt[63: 48] for hst1; Write 1 to clear fiq interrupt[63: 48] of hst1.
2Fh (10095Fh)	REG10095F	7:0	Default : 0x00 Access : R/W
	HST1_FIQ_STATUS_63_48_[15:8]	7:0	See description of '10095Eh'.
30h (100960h)	REG100960	7:0	Default : 0x00 Access : R/W
	HST1_IRQ_FORCE_15_0_[7:0]	7:0	Force to issue irq interrupt[15:0] to hst1; 0/1 : not force/force.
30h (100961h)	REG100961	7:0	Default : 0x00 Access : R/W
	HST1_IRQ_FORCE_15_0_[15:8]	7:0	See description of '100960h'.
31h (100962h)	REG100962	7:0	Default : 0x00 Access : R/W
	HST1_IRQ_FORCE_31_16_[7:0]	7:0	Force to issue irq interrupt[31:16] to hst1; 0/1 : not force/force.
31h (100963h)	REG100963	7:0	Default : 0x00 Access : R/W
	HST1_IRQ_FORCE_31_16_[15:8]	7:0	See description of '100962h'.
32h (100964h)	REG100964	7:0	Default : 0x00 Access : R/W
	HST1_IRQ_FORCE_47_32_[7:0]	7:0	Force to issue irq interrupt[47:32] to hst1; 0/1 : not force/force.
32h (100965h)	REG100965	7:0	Default : 0x00 Access : R/W
	HST1_IRQ_FORCE_47_32_[15:8]	7:0	See description of '100964h'.
33h (100966h)	REG100966	7:0	Default : 0xFF Access : R/W
	HST1_IRQ_FORCE_63_48_[7:0]	7:0	Force to issue irq interrupt[63: 48] to hst1; 0/1 : not force/force.

INTR_CTRL Register (Bank = 1009)				
Index (Absolute)	Mnemonic	Bit	Description	
33h (100967h)	REG100967	7:0	Default : 0xFF	Access : R/W
	HST1_IRQ_FORCE_63_48_[15:8]	7:0	See description of '100966h'.	
34h (100968h)	REG100968	7:0	Default : 0xFF	Access : R/W
	HST1_IRQ_MASK_15_0_[7:0]	7:0	Mask irq interrupt[15:0] for hst1; 0/1: not mask/mask.	
34h (100969h)	REG100969	7:0	Default : 0xFF	Access : R/W
	HST1_IRQ_MASK_15_0_[15:8]	7:0	See description of '100968h'.	
35h (10096Ah)	REG10096A	7:0	Default : 0xFF	Access : R/W
	HST1_IRQ_MASK_31_16_[7:0]	7:0	Mask irq interrupt[31:16] for hst1; 0/1: not mask/mask.	
35h (10096Bh)	REG10096B	7:0	Default : 0xFF	Access : R/W
	HST1_IRQ_MASK_31_16_[15:8]	7:0	See description of '10096Ah'.	
36h (10096Ch)	REG10096C	7:0	Default : 0xFF	Access : R/W
	HST1_IRQ_MASK_47_32_[7:0]	7:0	Mask irq interrupt[47:32] for hst1; 0/1: not mask/mask.	
36h (10096Dh)	REG10096D	7:0	Default : 0xFF	Access : R/W
	HST1_IRQ_MASK_47_32_[15:8]	7:0	See description of '10096Ch'.	
37h (10096Eh)	REG10096E	7:0	Default : 0xFF	Access : R/W
	HST1_IRQ_MASK_63_48_[7:0]	7:0	Mask irq interrupt[63: 48] for hst1; 0/1: not mask/mask.	
37h (10096Fh)	REG10096F	7:0	Default : 0xFF	Access : R/W
	HST1_IRQ_MASK_63_48_[15:8]	7:0	See description of '10096Eh'.	
38h (100970h)	REG100970	7:0	Default : 0x00	Access : R/W
	HST1_IRQ_POLARITY_15_0_[7:0]	7:0	Reverse irq interrupt[15:0] polarity for hst1; 0/1: not reverse/reverse.	
38h (100971h)	REG100971	7:0	Default : 0x00	Access : R/W
	HST1_IRQ_POLARITY_15_0_[15:8]	7:0	See description of '100970h'.	
39h (100972h)	REG100972	7:0	Default : 0x00	Access : R/W
	HST1_IRQ_POLARITY_31_1	7:0	Reverse irq interrupt[31:16] polarity for hst1; 0/1: not	

INTR_CTRL Register (Bank = 1009)				
Index (Absolute)	Mnemonic	Bit	Description	
	6_[7:0]		reverse/reverse.	
39h (100973h)	REG100973	7:0	Default : 0x00	Access : R/W
	HST1_IRQ_POLARITY_31_16_[15:8]	7:0	See description of '100972h'.	
3Ah (100974h)	REG100974	7:0	Default : 0x00	Access : R/W
	HST1_IRQ_POLARITY_47_32_[7:0]	7:0	Reverse irq interrupt[47:32] polarity for hst1; 0/1: not reverse/reverse.	
3Ah (100975h)	REG100975	7:0	Default : 0x00	Access : R/W
	HST1_IRQ_POLARITY_47_32_[15:8]	7:0	See description of '100974h'.	
3Bh (100976h)	REG100976	7:0	Default : 0x00	Access : R/W
	HST1_IRQ_POLARITY_63_48_[7:0]	7:0	Reverse irq interrupt[63: 48] polarity for hst1; 0/1: not reverse/reverse.	
3Bh (100977h)	REG100977	7:0	Default : 0x00	Access : R/W
	HST1_IRQ_POLARITY_63_48_[15:8]	7:0	See description of '100976h'.	
3Ch (100978h)	REG100978	7:0	Default : 0x00	Access : RO
	HST1_IRQ_STATUS_15_0_[7:0]	7:0	Read for the status of irq interrupt[15:0] for hst1;	
3Ch (100979h)	REG100979	7:0	Default : 0x00	Access : RO
	HST1_IRQ_STATUS_15_0_[15:8]	7:0	See description of '100978h'.	
3Dh (10097Ah)	REG10097A	7:0	Default : 0x00	Access : RO
	HST1_IRQ_STATUS_31_16_[7:0]	7:0	Read for the status of irq interrupt[31:16] for hst1;	
3Dh (10097Bh)	REG10097B	7:0	Default : 0x00	Access : RO
	HST1_IRQ_STATUS_31_16_[15:8]	7:0	See description of '10097Ah'.	
3Eh (10097Ch)	REG10097C	7:0	Default : 0x00	Access : RO
	HST1_IRQ_STATUS_47_32_[7:0]	7:0	Read for the status of irq interrupt[47:32] for hst1;	
3Eh (10097Dh)	REG10097D	7:0	Default : 0x00	Access : RO
	HST1_IRQ_STATUS_47_32_[15:8]	7:0	See description of '10097Ch'.	
3Fh	REG10097E	7:0	Default : 0x00	Access : RO

INTR_CTRL Register (Bank = 1009)			
Index (Absolute)	Mnemonic	Bit	Description
(10097Eh)	HST1_IRQ_STATUS_63_48_[7:0]	7:0	Read for the status of irq interrupt[63: 48] for hst1;
3Fh (10097Fh)	REG10097F	7:0	Default : 0x00 Access : RO
	HST1_IRQ_STATUS_63_48_[15:8]	7:0	See description of '10097Eh'.
40h (100980h)	REG100980	7:0	Default : 0x00 Access : R/W
	HST2_FIQ_FORCE_15_0_[7:0]	7:0	Force to issue fiq interrupt[15:0] to hst2; 0/1 : not force/force.
40h (100981h)	REG100981	7:0	Default : 0x00 Access : R/W
	HST2_FIQ_FORCE_15_0_[15:8]	7:0	See description of '100980h'.
41h (100982h)	REG100982	7:0	Default : 0x00 Access : R/W
	HST2_FIQ_FORCE_31_16_[7:0]	7:0	Force to issue fiq interrupt[31:16] to hst2; 0/1 : not force/force.
41h (100983h)	REG100983	7:0	Default : 0x00 Access : R/W
	HST2_FIQ_FORCE_31_16_[15:8]	7:0	See description of '100982h'.
42h (100984h)	REG100984	7:0	Default : 0x00 Access : R/W
	HST2_FIQ_FORCE_47_32_[7:0]	7:0	Force to issue fiq interrupt[47:32] to hst2; 0/1 : not force/force.
42h (100985h)	REG100985	7:0	Default : 0x00 Access : R/W
	HST2_FIQ_FORCE_47_32_[15:8]	7:0	See description of '100984h'.
43h (100986h)	REG100986	7:0	Default : 0xFF Access : R/W
	HST2_FIQ_FORCE_63_48_[7:0]	7:0	Force to issue fiq interrupt[63: 48] to hst2; 0/1 : not force/force.
43h (100987h)	REG100987	7:0	Default : 0xFF Access : R/W
	HST2_FIQ_FORCE_63_48_[15:8]	7:0	See description of '100986h'.
44h (100988h)	REG100988	7:0	Default : 0xFF Access : R/W
	HST2_FIQ_MASK_15_0_[7:0]	7:0	Mask fiq interrupt[15:0] for hst2; 0/1: not mask/mask.
44h (100989h)	REG100989	7:0	Default : 0xFF Access : R/W
	HST2_FIQ_MASK_15_0_[15:8]	7:0	See description of '100988h'.

INTR_CTRL Register (Bank = 1009)				
Index (Absolute)	Mnemonic	Bit	Description	
45h (10098Ah)	REG10098A	7:0	Default : 0xFF	Access : R/W
	HST2_FIQ_MASK_31_16_[7:0]	7:0	Mask fiq interrupt[31:16] for hst2; 0/1: not mask/mask.	
45h (10098Bh)	REG10098B	7:0	Default : 0xFF	Access : R/W
	HST2_FIQ_MASK_31_16_[15:8]	7:0	See description of '10098Ah'.	
46h (10098Ch)	REG10098C	7:0	Default : 0xFF	Access : R/W
	HST2_FIQ_MASK_47_32_[7:0]	7:0	Mask fiq interrupt[47:32] for hst2; 0/1: not mask/mask.	
46h (10098Dh)	REG10098D	7:0	Default : 0xFF	Access : R/W
	HST2_FIQ_MASK_47_32_[15:8]	7:0	See description of '10098Ch'.	
47h (10098Eh)	REG10098E	7:0	Default : 0xFF	Access : R/W
	HST2_FIQ_MASK_63_48_[7:0]	7:0	Mask fiq interrupt[63: 48] for hst2; 0/1: not mask/mask.	
47h (10098Fh)	REG10098F	7:0	Default : 0xFF	Access : R/W
	HST2_FIQ_MASK_63_48_[15:8]	7:0	See description of '10098Eh'.	
48h (100990h)	REG100990	7:0	Default : 0x00	Access : R/W
	HST2_FIQ_POLARITY_15_0_[7:0]	7:0	Reverse fiq interrupt[15:0] polarity for hst2; 0/1: not reverse/reverse.	
48h (100991h)	REG100991	7:0	Default : 0x00	Access : R/W
	HST2_FIQ_POLARITY_15_0_[15:8]	7:0	See description of '100990h'.	
49h (100992h)	REG100992	7:0	Default : 0x00	Access : R/W
	HST2_FIQ_POLARITY_31_16_[7:0]	7:0	Reverse fiq interrupt[31:16] polarity for hst2; 0/1: not reverse/reverse.	
49h (100993h)	REG100993	7:0	Default : 0x00	Access : R/W
	HST2_FIQ_POLARITY_31_16_[15:8]	7:0	See description of '100992h'.	
4Ah (100994h)	REG100994	7:0	Default : 0x00	Access : R/W
	HST2_FIQ_POLARITY_47_32_[7:0]	7:0	Reverse fiq interrupt[47:32] polarity for hst2; 0/1: not reverse/reverse.	
4Ah (100995h)	REG100995	7:0	Default : 0x00	Access : R/W
	HST2_FIQ_POLARITY_47_3	7:0	See description of '100994h'.	

INTR_CTRL Register (Bank = 1009)				
Index (Absolute)	Mnemonic	Bit	Description	
	2_[15:8]			
4Bh (100996h)	REG100996	7:0	Default : 0x00	Access : R/W
	HST2_FIQ_POLARITY_63_48_[7:0]	7:0	Reverse fiq interrupt[63: 48] polarity for hst2; 0/1: not reverse/reverse.	
4Bh (100997h)	REG100997	7:0	Default : 0x00	Access : R/W
	HST2_FIQ_POLARITY_63_48_[15:8]	7:0	See description of '100996h'.	
4Ch (100998h)	REG100998	7:0	Default : 0x00	Access : R/W
	HST2_FIQ_STATUS_15_0_[7:0]	7:0	Read for the status of fiq interrupt[15:0] for hst2; Write 1 to clear fiq interrupt[15:0] of hst2.	
4Ch (100999h)	REG100999	7:0	Default : 0x00	Access : R/W
	HST2_FIQ_STATUS_15_0_[15:8]	7:0	See description of '100998h'.	
4Dh (10099Ah)	REG10099A	7:0	Default : 0x00	Access : R/W
	HST2_FIQ_STATUS_31_16_[7:0]	7:0	Read for the status of fiq interrupt[31:16] for hst2; Write 1 to clear fiq interrupt[31:16] of hst2.	
4Dh (10099Bh)	REG10099B	7:0	Default : 0x00	Access : R/W
	HST2_FIQ_STATUS_31_16_[15:8]	7:0	See description of '10099Ah'.	
4Eh (10099Ch)	REG10099C	7:0	Default : 0x00	Access : R/W
	HST2_FIQ_STATUS_47_32_[7:0]	7:0	Read for the status of fiq interrupt[47:32] for hst2; Write 1 to clear fiq interrupt[47:32] of hst2.	
4Eh (10099Dh)	REG10099D	7:0	Default : 0x00	Access : R/W
	HST2_FIQ_STATUS_47_32_[15:8]	7:0	See description of '10099Ch'.	
4Fh (10099Eh)	REG10099E	7:0	Default : 0x00	Access : R/W
	HST2_FIQ_STATUS_63_48_[7:0]	7:0	Read for the status of fiq interrupt[63: 48] for hst2; Write 1 to clear fiq interrupt[63: 48] of hst2.	
4Fh (10099Fh)	REG10099F	7:0	Default : 0x00	Access : R/W
	HST2_FIQ_STATUS_63_48_[15:8]	7:0	See description of '10099Eh'.	
50h (1009A0h)	REG1009A0	7:0	Default : 0x00	Access : R/W
	HST2_IRQ_FORCE_15_0_[7:0]	7:0	Force to issue irq interrupt[15:0] to hst2; 0/1 : not force/force.	
50h	REG1009A1	7:0	Default : 0x00	Access : R/W

INTR_CTRL Register (Bank = 1009)			
Index (Absolute)	Mnemonic	Bit	Description
(1009A1h)	HST2_IRQ_FORCE_15_0_[15:8]	7:0	See description of '1009A0h'.
51h (1009A2h)	REG1009A2	7:0	Default : 0x00 Access : R/W
	HST2_IRQ_FORCE_31_16_[7:0]	7:0	Force to issue irq interrupt[31:16] to hst2; 0/1 : not force/force.
51h (1009A3h)	REG1009A3	7:0	Default : 0x00 Access : R/W
	HST2_IRQ_FORCE_31_16_[15:8]	7:0	See description of '1009A2h'.
52h (1009A4h)	REG1009A4	7:0	Default : 0x00 Access : R/W
	HST2_IRQ_FORCE_47_32_[7:0]	7:0	Force to issue irq interrupt[47:32] to hst2; 0/1 : not force/force.
52h (1009A5h)	REG1009A5	7:0	Default : 0x00 Access : R/W
	HST2_IRQ_FORCE_47_32_[15:8]	7:0	See description of '1009A4h'.
53h (1009A6h)	REG1009A6	7:0	Default : 0xFF Access : R/W
	HST2_IRQ_FORCE_63_48_[7:0]	7:0	Force to issue irq interrupt[63: 48] to hst2; 0/1 : not force/force.
53h (1009A7h)	REG1009A7	7:0	Default : 0xFF Access : R/W
	HST2_IRQ_FORCE_63_48_[15:8]	7:0	See description of '1009A6h'.
54h (1009A8h)	REG1009A8	7:0	Default : 0xFF Access : R/W
	HST2_IRQ_MASK_15_0_[7:0]	7:0	Mask irq interrupt[15:0] for hst2; 0/1: not mask/mask.
54h (1009A9h)	REG1009A9	7:0	Default : 0xFF Access : R/W
	HST2_IRQ_MASK_15_0_[15:8]	7:0	See description of '1009A8h'.
55h (1009AAh)	REG1009AA	7:0	Default : 0xFF Access : R/W
	HST2_IRQ_MASK_31_16_[7:0]	7:0	Mask irq interrupt[31:16] for hst2; 0/1: not mask/mask.
55h (1009ABh)	REG1009AB	7:0	Default : 0xFF Access : R/W
	HST2_IRQ_MASK_31_16_[15:8]	7:0	See description of '1009AAh'.
56h (1009ACh)	REG1009AC	7:0	Default : 0xFF Access : R/W
	HST2_IRQ_MASK_47_32_[7:0]	7:0	Mask irq interrupt[47:32] for hst2; 0/1: not mask/mask.

INTR_CTRL Register (Bank = 1009)				
Index (Absolute)	Mnemonic	Bit	Description	
56h (1009ADh)	REG1009AD	7:0	Default : 0xFF	Access : R/W
	HST2_IRQ_MASK_47_32_[15:8]	7:0	See description of '1009ACh'.	
57h (1009AEh)	REG1009AE	7:0	Default : 0xFF	Access : R/W
	HST2_IRQ_MASK_63_48_[7:0]	7:0	Mask irq interrupt[63: 48] for hst2; 0/1: not mask/mask.	
57h (1009AFh)	REG1009AF	7:0	Default : 0xFF	Access : R/W
	HST2_IRQ_MASK_63_48_[15:8]	7:0	See description of '1009AEh'.	
58h (1009B0h)	REG1009B0	7:0	Default : 0x00	Access : R/W
	HST2_IRQ_POLARITY_15_0_[7:0]	7:0	Reverse irq interrupt[15:0] polarity for hst2; 0/1: not reverse/reverse.	
58h (1009B1h)	REG1009B1	7:0	Default : 0x00	Access : R/W
	HST2_IRQ_POLARITY_15_0_[15:8]	7:0	See description of '1009B0h'.	
59h (1009B2h)	REG1009B2	7:0	Default : 0x00	Access : R/W
	HST2_IRQ_POLARITY_31_16_[7:0]	7:0	Reverse irq interrupt[31:16] polarity for hst2; 0/1: not reverse/reverse.	
59h (1009B3h)	REG1009B3	7:0	Default : 0x00	Access : R/W
	HST2_IRQ_POLARITY_31_16_[15:8]	7:0	See description of '1009B2h'.	
5Ah (1009B4h)	REG1009B4	7:0	Default : 0x00	Access : R/W
	HST2_IRQ_POLARITY_47_32_[7:0]	7:0	Reverse irq interrupt[47:32] polarity for hst2; 0/1: not reverse/reverse.	
5Ah (1009B5h)	REG1009B5	7:0	Default : 0x00	Access : R/W
	HST2_IRQ_POLARITY_47_32_[15:8]	7:0	See description of '1009B4h'.	
5Bh (1009B6h)	REG1009B6	7:0	Default : 0x00	Access : R/W
	HST2_IRQ_POLARITY_63_48_[7:0]	7:0	Reverse irq interrupt[63: 48] polarity for hst2; 0/1: not reverse/reverse.	
5Bh (1009B7h)	REG1009B7	7:0	Default : 0x00	Access : R/W
	HST2_IRQ_POLARITY_63_48_[15:8]	7:0	See description of '1009B6h'.	
5Ch (1009B8h)	REG1009B8	7:0	Default : 0x00	Access : RO
	HST2_IRQ_STATUS_15_0_[	7:0	Read for the status of irq interrupt[15:0] for hst2;	

INTR_CTRL Register (Bank = 1009)				
Index (Absolute)	Mnemonic	Bit	Description	
	7:0]			
5Ch (1009B9h)	REG1009B9	7:0	Default : 0x00	Access : RO
	HST2_IRQ_STATUS_15_0_[15:8]	7:0	See description of '1009B8h'.	
5Dh (1009BAh)	REG1009BA	7:0	Default : 0x00	Access : RO
	HST2_IRQ_STATUS_31_16_[7:0]	7:0	Read for the status of irq interrupt[31:16] for hst2;	
5Dh (1009BBh)	REG1009BB	7:0	Default : 0x00	Access : RO
	HST2_IRQ_STATUS_31_16_[15:8]	7:0	See description of '1009BAh'.	
5Eh (1009BCh)	REG1009BC	7:0	Default : 0x00	Access : RO
	HST2_IRQ_STATUS_47_32_[7:0]	7:0	Read for the status of irq interrupt[47:32] for hst2;	
5Eh (1009BDh)	REG1009BD	7:0	Default : 0x00	Access : RO
	HST2_IRQ_STATUS_47_32_[15:8]	7:0	See description of '1009BCh'.	
5Fh (1009BEh)	REG1009BE	7:0	Default : 0x00	Access : RO
	HST2_IRQ_STATUS_63_48_[7:0]	7:0	Read for the status of irq interrupt[63: 48] for hst2;	
5Fh (1009BFh)	REG1009BF	7:0	Default : 0x00	Access : RO
	HST2_IRQ_STATUS_63_48_[15:8]	7:0	See description of '1009BEh'.	
60h (1009C0h)	REG1009C0	7:0	Default : 0x00	Access : R/W
	HST3_FIQ_FORCE_15_0_[7:0]	7:0	Force to issue fiq interrupt[15:0] to hst3; 0/1 : not force/force.	
60h (1009C1h)	REG1009C1	7:0	Default : 0x00	Access : R/W
	HST3_FIQ_FORCE_15_0_[15:8]	7:0	See description of '1009C0h'.	
61h (1009C2h)	REG1009C2	7:0	Default : 0x00	Access : R/W
	HST3_FIQ_FORCE_31_16_[7:0]	7:0	Force to issue fiq interrupt[31:16] to hst3; 0/1 : not force/force.	
61h (1009C3h)	REG1009C3	7:0	Default : 0x00	Access : R/W
	HST3_FIQ_FORCE_31_16_[15:8]	7:0	See description of '1009C2h'.	
62h	REG1009C4	7:0	Default : 0x00	Access : R/W

INTR_CTRL Register (Bank = 1009)			
Index (Absolute)	Mnemonic	Bit	Description
(1009C4h)	HST3_FIQ_FORCE_47_32_[7:0]	7:0	Force to issue fiq interrupt[47:32] to hst3; 0/1 : not force/force.
62h (1009C5h)	REG1009C5	7:0	Default : 0x00 Access : R/W
	HST3_FIQ_FORCE_47_32_[15:8]	7:0	See description of '1009C4h'.
63h (1009C6h)	REG1009C6	7:0	Default : 0xFF Access : R/W
	HST3_FIQ_FORCE_63_48_[7:0]	7:0	Force to issue fiq interrupt[63: 48] to hst3; 0/1 : not force/force.
63h (1009C7h)	REG1009C7	7:0	Default : 0xFF Access : R/W
	HST3_FIQ_FORCE_63_48_[15:8]	7:0	See description of '1009C6h'.
64h (1009C8h)	REG1009C8	7:0	Default : 0xFF Access : R/W
	HST3_FIQ_MASK_15_0_[7:0]	7:0	Mask fiq interrupt[15:0] for hst3; 0/1: not mask/mask.
64h (1009C9h)	REG1009C9	7:0	Default : 0xFF Access : R/W
	HST3_FIQ_MASK_15_0_[15:8]	7:0	See description of '1009C8h'.
65h (1009CAh)	REG1009CA	7:0	Default : 0xFF Access : R/W
	HST3_FIQ_MASK_31_16_[7:0]	7:0	Mask fiq interrupt[31:16] for hst3; 0/1: not mask/mask.
65h (1009CBh)	REG1009CB	7:0	Default : 0xFF Access : R/W
	HST3_FIQ_MASK_31_16_[15:8]	7:0	See description of '1009CAh'.
66h (1009CCh)	REG1009CC	7:0	Default : 0xFF Access : R/W
	HST3_FIQ_MASK_47_32_[7:0]	7:0	Mask fiq interrupt[47:32] for hst3; 0/1: not mask/mask.
66h (1009CDh)	REG1009CD	7:0	Default : 0xFF Access : R/W
	HST3_FIQ_MASK_47_32_[15:8]	7:0	See description of '1009CCh'.
67h (1009CEh)	REG1009CE	7:0	Default : 0xFF Access : R/W
	HST3_FIQ_MASK_63_48_[7:0]	7:0	Mask fiq interrupt[63: 48] for hst3; 0/1: not mask/mask.
67h (1009CFh)	REG1009CF	7:0	Default : 0xFF Access : R/W
	HST3_FIQ_MASK_63_48_[15:8]	7:0	See description of '1009CEh'.

INTR_CTRL Register (Bank = 1009)				
Index (Absolute)	Mnemonic	Bit	Description	
68h (1009D0h)	REG1009D0	7:0	Default : 0x00	Access : R/W
	HST3_FIQ_POLARITY_15_0_[7:0]	7:0	Reverse fiq interrupt[15:0] polarity for hst3; 0/1: not reverse/reverse.	
68h (1009D1h)	REG1009D1	7:0	Default : 0x00	Access : R/W
	HST3_FIQ_POLARITY_15_0_[15:8]	7:0	See description of '1009D0h'.	
69h (1009D2h)	REG1009D2	7:0	Default : 0x00	Access : R/W
	HST3_FIQ_POLARITY_31_16_[7:0]	7:0	Reverse fiq interrupt[31:16] polarity for hst3; 0/1: not reverse/reverse.	
69h (1009D3h)	REG1009D3	7:0	Default : 0x00	Access : R/W
	HST3_FIQ_POLARITY_31_16_[15:8]	7:0	See description of '1009D2h'.	
6Ah (1009D4h)	REG1009D4	7:0	Default : 0x00	Access : R/W
	HST3_FIQ_POLARITY_47_32_[7:0]	7:0	Reverse fiq interrupt[47:32] polarity for hst3; 0/1: not reverse/reverse.	
6Ah (1009D5h)	REG1009D5	7:0	Default : 0x00	Access : R/W
	HST3_FIQ_POLARITY_47_32_[15:8]	7:0	See description of '1009D4h'.	
6Bh (1009D6h)	REG1009D6	7:0	Default : 0x00	Access : R/W
	HST3_FIQ_POLARITY_63_48_[7:0]	7:0	Reverse fiq interrupt[63: 48] polarity for hst3; 0/1: not reverse/reverse.	
6Bh (1009D7h)	REG1009D7	7:0	Default : 0x00	Access : R/W
	HST3_FIQ_POLARITY_63_48_[15:8]	7:0	See description of '1009D6h'.	
6Ch (1009D8h)	REG1009D8	7:0	Default : 0x00	Access : R/W
	HST3_FIQ_STATUS_15_0_[7:0]	7:0	Read for the status of fiq interrupt[15:0] for hst3; Write 1 to clear fiq interrupt[15:0] of hst3.	
6Ch (1009D9h)	REG1009D9	7:0	Default : 0x00	Access : R/W
	HST3_FIQ_STATUS_15_0_[15:8]	7:0	See description of '1009D8h'.	
6Dh (1009DAh)	REG1009DA	7:0	Default : 0x00	Access : R/W
	HST3_FIQ_STATUS_31_16_[7:0]	7:0	Read for the status of fiq interrupt[31:16] for hst3; Write 1 to clear fiq interrupt[31:16] of hst3.	
6Dh (1009DBh)	REG1009DB	7:0	Default : 0x00	Access : R/W
	HST3_FIQ_STATUS_31_16_	7:0	See description of '1009DAh'.	

INTR_CTRL Register (Bank = 1009)				
Index (Absolute)	Mnemonic	Bit	Description	
	[15:8]			
6Eh (1009DCh)	REG1009DC	7:0	Default : 0x00	Access : R/W
	HST3_FIQ_STATUS_47_32_[7:0]	7:0	Read for the status of fiq interrupt[47:32] for hst3; Write 1 to clear fiq interrupt[47:32] of hst3.	
6Eh (1009DDh)	REG1009DD	7:0	Default : 0x00	Access : R/W
	HST3_FIQ_STATUS_47_32_[15:8]	7:0	See description of '1009DCh'.	
6Fh (1009DEh)	REG1009DE	7:0	Default : 0x00	Access : R/W
	HST3_FIQ_STATUS_63_48_[7:0]	7:0	Read for the status of fiq interrupt[63: 48] for hst3; Write 1 to clear fiq interrupt[63: 48] of hst3.	
6Fh (1009DFh)	REG1009DF	7:0	Default : 0x00	Access : R/W
	HST3_FIQ_STATUS_63_48_[15:8]	7:0	See description of '1009DEh'.	
70h (1009E0h)	REG1009E0	7:0	Default : 0x00	Access : R/W
	HST3_IRQ_FORCE_15_0_[7:0]	7:0	Force to issue irq interrupt[15:0] to hst3; 0/1 : not force/force.	
70h (1009E1h)	REG1009E1	7:0	Default : 0x00	Access : R/W
	HST3_IRQ_FORCE_15_0_[15:8]	7:0	See description of '1009E0h'.	
71h (1009E2h)	REG1009E2	7:0	Default : 0x00	Access : R/W
	HST3_IRQ_FORCE_31_16_[7:0]	7:0	Force to issue irq interrupt[31:16] to hst3; 0/1 : not force/force.	
71h (1009E3h)	REG1009E3	7:0	Default : 0x00	Access : R/W
	HST3_IRQ_FORCE_31_16_[15:8]	7:0	See description of '1009E2h'.	
72h (1009E4h)	REG1009E4	7:0	Default : 0x00	Access : R/W
	HST3_IRQ_FORCE_47_32_[7:0]	7:0	Force to issue irq interrupt[47:32] to hst3; 0/1 : not force/force.	
72h (1009E5h)	REG1009E5	7:0	Default : 0x00	Access : R/W
	HST3_IRQ_FORCE_47_32_[15:8]	7:0	See description of '1009E4h'.	
73h (1009E6h)	REG1009E6	7:0	Default : 0xFF	Access : R/W
	HST3_IRQ_FORCE_63_48_[7:0]	7:0	Force to issue irq interrupt[63: 48] to hst3; 0/1 : not force/force.	
73h	REG1009E7	7:0	Default : 0xFF	Access : R/W

INTR_CTRL Register (Bank = 1009)				
Index (Absolute)	Mnemonic	Bit	Description	
(1009E7h)	HST3_IRQ_FORCE_63_48_[15:8]	7:0	See description of '1009E6h'.	
74h (1009E8h)	REG1009E8	7:0	Default : 0xFF	Access : R/W
	HST3_IRQ_MASK_15_0_[7:0]	7:0	Mask irq interrupt[15:0] for hst3; 0/1: not mask/mask.	
74h (1009E9h)	REG1009E9	7:0	Default : 0xFF	Access : R/W
	HST3_IRQ_MASK_15_0_[15:8]	7:0	See description of '1009E8h'.	
75h (1009EAh)	REG1009EA	7:0	Default : 0xFF	Access : R/W
	HST3_IRQ_MASK_31_16_[7:0]	7:0	Mask irq interrupt[31:16] for hst3; 0/1: not mask/mask.	
75h (1009EBh)	REG1009EB	7:0	Default : 0xFF	Access : R/W
	HST3_IRQ_MASK_31_16_[15:8]	7:0	See description of '1009EAh'.	
76h (1009ECh)	REG1009EC	7:0	Default : 0xFF	Access : R/W
	HST3_IRQ_MASK_47_32_[7:0]	7:0	Mask irq interrupt[47:32] for hst3; 0/1: not mask/mask.	
76h (1009EDh)	REG1009ED	7:0	Default : 0xFF	Access : R/W
	HST3_IRQ_MASK_47_32_[15:8]	7:0	See description of '1009ECh'.	
77h (1009EEh)	REG1009EE	7:0	Default : 0xFF	Access : R/W
	HST3_IRQ_MASK_63_48_[7:0]	7:0	Mask irq interrupt[63: 48] for hst3; 0/1: not mask/mask.	
77h (1009EFh)	REG1009EF	7:0	Default : 0xFF	Access : R/W
	HST3_IRQ_MASK_63_48_[15:8]	7:0	See description of '1009EEh'.	
78h (1009F0h)	REG1009F0	7:0	Default : 0x00	Access : R/W
	HST3_IRQ_POLARITY_15_0_[7:0]	7:0	Reverse irq interrupt[15:0] polarity for hst3; 0/1: not reverse/reverse.	
78h (1009F1h)	REG1009F1	7:0	Default : 0x00	Access : R/W
	HST3_IRQ_POLARITY_15_0_[15:8]	7:0	See description of '1009F0h'.	
79h (1009F2h)	REG1009F2	7:0	Default : 0x00	Access : R/W
	HST3_IRQ_POLARITY_31_16_[7:0]	7:0	Reverse irq interrupt[31:16] polarity for hst3; 0/1: not reverse/reverse.	

INTR_CTRL Register (Bank = 1009)				
Index (Absolute)	Mnemonic	Bit	Description	
79h (1009F3h)	REG1009F3	7:0	Default : 0x00	Access : R/W
	HST3_IRQ_POLARITY_31_16_[15:8]	7:0	See description of '1009F2h'.	
7Ah (1009F4h)	REG1009F4	7:0	Default : 0x00	Access : R/W
	HST3_IRQ_POLARITY_47_32_[7:0]	7:0	Reverse irq interrupt[47:32] polarity for hst3; 0/1: not reverse/reverse.	
7Ah (1009F5h)	REG1009F5	7:0	Default : 0x00	Access : R/W
	HST3_IRQ_POLARITY_47_32_[15:8]	7:0	See description of '1009F4h'.	
7Bh (1009F6h)	REG1009F6	7:0	Default : 0x00	Access : R/W
	HST3_IRQ_POLARITY_63_48_[7:0]	7:0	Reverse irq interrupt[63: 48] polarity for hst3; 0/1: not reverse/reverse.	
7Bh (1009F7h)	REG1009F7	7:0	Default : 0x00	Access : R/W
	HST3_IRQ_POLARITY_63_48_[15:8]	7:0	See description of '1009F6h'.	
7Ch (1009F8h)	REG1009F8	7:0	Default : 0x00	Access : RO
	HST3_IRQ_STATUS_15_0_[7:0]	7:0	Read for the status of irq interrupt[15:0] for hst3;	
7Ch (1009F9h)	REG1009F9	7:0	Default : 0x00	Access : RO
	HST3_IRQ_STATUS_15_0_[15:8]	7:0	See description of '1009F8h'.	
7Dh (1009FAh)	REG1009FA	7:0	Default : 0x00	Access : RO
	HST3_IRQ_STATUS_31_16_[7:0]	7:0	Read for the status of irq interrupt[31:16] for hst3;	
7Dh (1009FBh)	REG1009FB	7:0	Default : 0x00	Access : RO
	HST3_IRQ_STATUS_31_16_[15:8]	7:0	See description of '1009FAh'.	
7Eh (1009FCh)	REG1009FC	7:0	Default : 0x00	Access : RO
	HST3_IRQ_STATUS_47_32_[7:0]	7:0	Read for the status of irq interrupt[47:32] for hst3;	
7Eh (1009FDh)	REG1009FD	7:0	Default : 0x00	Access : RO
	HST3_IRQ_STATUS_47_32_[15:8]	7:0	See description of '1009FCh'.	
7Fh (1009FEh)	REG1009FE	7:0	Default : 0x00	Access : RO
	HST3_IRQ_STATUS_63_48	7:0	Read for the status of irq interrupt[63: 48] for hst3;	

INTR_CTRL Register (Bank = 1009)				
Index (Absolute)	Mnemonic	Bit	Description	
	_[7:0]			
7Fh (1009FFh)	REG1009FF	7:0	Default : 0x00	Access : RO
	HST3_IRQ_STATUS_63_48_[15:8]	7:0	See description of '1009FEh'.	