SSD202D
TIMER Module Description

1. MODULE DESCRIPTION

1.1. Overview

The Timer module is implemented for the counting function. It not only helps CPU get time correctly, but also serves as general counting operation. Three timers are provided in this system.

1.2. Function Description

The Timer has the following features:

- 32-bit counter
- 8-bit divider can be set to enhance precision
- Supports counting for one time or rolling again and again
- Can read current count value
- Interrupt asserted when timer hits the max value

1.3. Operating Flow

1. Set divide register for timer counter frequency.
2. Set timer max for maximum value of timer.
3. Enable interrupt, if needed.
4. Trigger timer (counting from 0 to max):
   - set enable register to count and roll.
   - set trigger register to enable counting for one time.
5. Read comp register for the current timer value.
   - read LSB first if your system is not 32-bit.

2. REGISTER DESCRIPTION

2.1. TIMER0 Register (Bank = 30)

TIMER0 Register (Bank = 30)				
Index (Absolute)	Mnemonic	Bit	Description	
10h (3020h)	REG3020	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	TIMER_TRIG	1	Set: Enable timer to count one time (from 0 to max, then stop). Clear: By resetting itself or by setting reg_timer_en.	
	TIMER_EN	0	Set: Enable timer counting to be rolled (from 0 to max, then rolled). Clear: By resetting itself or by setting reg_timer_trig.	
10h (3021h)	REG3021	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	TIMER_INT_EN	0	Set: Enable interrupt. Clear: By resetting itself.	
11h (3022h)	REG3022	7:0	Default : 0x00	Access : RO
	-	7:1	Reserved.	
	TIMER_HIT	0	Assert: When counter is enabled and matches reg_timer_max. Deassert: By writing 1 or by setting reg_timer_en, reg_timer_once, and reg_timer_max.	
12h (3024h)	REG3024	7:0	Default : 0xFF	Access : R/W
	TIMER_MAX[7:0]	7:0	Timer maximum value.	
12h (3025h)	REG3025	7:0	Default : 0xFF	Access : R/W
	TIMER_MAX[15:8]	7:0	See description of '3024h'.	
13h (3026h)	REG3026	7:0	Default : 0xFF	Access : R/W
	TIMER_MAX[23:16]	7:0	See description of '3024h'.	
13h (3027h)	REG3027	7:0	Default : 0xFF	Access : R/W
	TIMER_MAX[31:24]	7:0	See description of '3024h'.	
14h (3028h)	REG3028	7:0	Default : 0x00	Access : RO
	TIMER_CAP[7:0]	7:0	Timer current value. Note: With non-32-bit-data system, please read from LSB.	

TIMER0 Register (Bank = 30)				
Index (Absolute)	Mnemonic	Bit	Description	
14h (3029h)	REG3029	7:0	Default : 0x00	Access : RO
	TIMER_CAP[15:8]	7:0	See description of '3028h'.	
15h (302Ah)	REG302A	7:0	Default : 0x00	Access : RO
	TIMER_CAP[23:16]	7:0	See description of '3028h'.	
15h (302Bh)	REG302B	7:0	Default : 0x00	Access : RO
	TIMER_CAP[31:24]	7:0	See description of '3028h'.	
16h (302Ch)	REG302C	7:0	Default : 0x00	Access : R/W
	TIMER_DEVIDE[7:0]	7:0	Timer divide counter number. Default = 12M (216(clk_xiu)/18). 8'b0000: timer counter = clk_xiu/1. 8'b0001: timer counter = clk_xiu/2. 8'b0010: timer counter = clk_xiu/3. ... 8'b1111: timer counter = clk_xiu/16.	

2.2. TIMER1 Register (Bank = 30)

TIMER1 Register (Bank = 30)				
Index (Absolute)	Mnemonic	Bit	Description	
20h (3040h)	REG3040	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	TIMER_TRIG	1	Set: Enable timer to count one time (from 0 to max, then stop). Clear: By resetting itself or by setting reg_timer_en.	
	TIMER_EN	0	Set: Enable timer counting to be rolled (from 0 to max, then rolled). Clear: By resetting itself or by setting reg_timer_trig.	
20h (3041h)	REG3041	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	TIMER_INT_EN	0	Set: Enable interrupt. Clear: By resetting itself.	
21h (3042h)	REG3042	7:0	Default : 0x00	Access : RO
	-	7:1	Reserved.	
	TIMER_HIT	0	Assert: When counter is enabled and matches reg_timer_max. Deassert: By writing 1 or by setting reg_timer_en,	

TIMER1 Register (Bank = 30)				
Index (Absolute)	Mnemonic	Bit	Description	
			reg_timer_once, and reg_timer_max.	
22h (3044h)	REG3044	7:0	Default : 0xFF	Access : R/W
	TIMER_MAX[7:0]	7:0	Timer maximum value.	
22h (3045h)	REG3045	7:0	Default : 0xFF	Access : R/W
	TIMER_MAX[15:8]	7:0	See description of '3044h'.	
23h (3046h)	REG3046	7:0	Default : 0xFF	Access : R/W
	TIMER_MAX[23:16]	7:0	See description of '3044h'.	
23h (3047h)	REG3047	7:0	Default : 0xFF	Access : R/W
	TIMER_MAX[31:24]	7:0	See description of '3044h'.	
24h (3048h)	REG3048	7:0	Default : 0x00	Access : RO
	TIMER_CAP[7:0]	7:0	Timer current value. Note: With non-32-bit-data system, please read from LSB.	
24h (3049h)	REG3049	7:0	Default : 0x00	Access : RO
	TIMER_CAP[15:8]	7:0	See description of '3048h'.	
25h (304Ah)	REG304A	7:0	Default : 0x00	Access : RO
	TIMER_CAP[23:16]	7:0	See description of '3048h'.	
25h (304Bh)	REG304B	7:0	Default : 0x00	Access : RO
	TIMER_CAP[31:24]	7:0	See description of '3048h'.	
26h (304Ch)	REG304C	7:0	Default : 0x00	Access : R/W
	TIMER_DEVIDE[7:0]	7:0	Timer divide counter number. Default = 12M (216(clk_xiu)/18). 8'b0000: timer counter = clk_xiu/1. 8'b0001: timer counter = clk_xiu/2. 8'b0010: timer counter = clk_xiu/3. ... 8'b1111: timer counter = clk_xiu/16.	

2.3. TIMER2 Register (Bank = 30)

TIMER2 Register (Bank = 30)				
Index (Absolute)	Mnemonic	Bit	Description	
30h (3060h)	REG3060	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	TIMER_TRIG	1	Set: Enable timer to count one time (from 0 to max, then stop).	

TIMER2 Register (Bank = 30)				
Index (Absolute)	Mnemonic	Bit	Description	
			Clear: By resetting itself or by setting reg_timer_en.	
	TIMER_EN	0	Set: Enable timer counting to be rolled (from 0 to max, then rolled). Clear: By resetting itself or by setting reg_timer_trig.	
30h (3061h)	REG3061	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	TIMER_INT_EN	0	Set: Enable interrupt. Clear: By resetting itself.	
31h (3062h)	REG3062	7:0	Default : 0x00	Access : RO
	-	7:1	Reserved.	
	TIMER_HIT	0	Assert: When counter is enabled and matches reg_timer_max. Deassert: By writing 1 or by setting reg_timer_en, reg_timer_once, and reg_timer_max.	
32h (3064h)	REG3064	7:0	Default : 0xFF	Access : R/W
	TIMER_MAX[7:0]	7:0	Timer maximum value.	
32h (3065h)	REG3065	7:0	Default : 0xFF	Access : R/W
	TIMER_MAX[15:8]	7:0	See description of '3064h'.	
33h (3066h)	REG3066	7:0	Default : 0xFF	Access : R/W
	TIMER_MAX[23:16]	7:0	See description of '3064h'.	
33h (3067h)	REG3067	7:0	Default : 0xFF	Access : R/W
	TIMER_MAX[31:24]	7:0	See description of '3064h'.	
34h (3068h)	REG3068	7:0	Default : 0x00	Access : RO
	TIMER_CAP[7:0]	7:0	Timer current value. Note: With non-32-bit-data system, please read from LSB.	
34h (3069h)	REG3069	7:0	Default : 0x00	Access : RO
	TIMER_CAP[15:8]	7:0	See description of '3068h'.	
35h (306Ah)	REG306A	7:0	Default : 0x00	Access : RO
	TIMER_CAP[23:16]	7:0	See description of '3068h'.	
35h (306Bh)	REG306B	7:0	Default : 0x00	Access : RO
	TIMER_CAP[31:24]	7:0	See description of '3068h'.	
36h (306Ch)	REG306C	7:0	Default : 0x00	Access : R/W
	TIMER_DEVIDE[7:0]	7:0	Timer divide counter number. Default = 12M (216(clk_xiu)/18). 8'b0000: timer counter = clk_xiu/1.	

TIMER2 Register (Bank = 30)			
Index (Absolute)	Mnemonic	Bit	Description
			8'b0001: timer counter = clk_xiu/2. 8'b0010: timer counter = clk_xiu/3. ... 8'b1111: timer counter = clk_xiu/16.