SSD202D
PWM Module Description

1. MODULE DESCRIPTION

1.1. Overview

The PWM function is used to generate the pulse width waveform. This ASIC supports four sync-mode PWMs.

1.2. Function Description

The PWM module has the following features:

- Working range is from (OSC clk/2) to (OSC clk/2^34) – for example, if OSC clk = 12MHz, the range is 6MHz ~ 0.007Hz
- Supports 1MHz, 1.5MHz, 3MHz, 6MHz, 8MHz, 12MHz and 86MHz clock source
- Supports double buffer to avoid generating wrong waveform
- Supports 1~4 multiple pulses in one PWM (double buffer should be set in this mode)
- Supports N round mode
- Supports Hold mode
- Supports Stop mode
- Supports Sync mode

1.3. Operating Mode and Guideline

PWM settings could be double buffered to prevent wrong waveform from being generated.

1. Set DBEN = 1 to enable normal double buffer. The newly inputted value will be loaded only when a current PWM has been completely generated. See Figure 1-1 below.
2. Wrong PWM pulse could be prevented if VDBEN_SW is pulled low while registers are set, as shown in Figure 1-2.

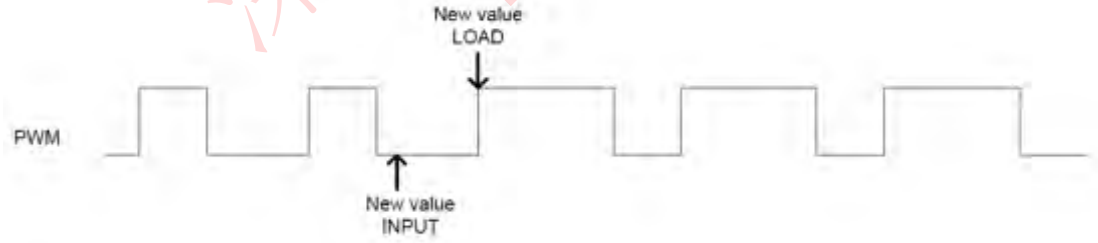


Figure 1-1: PWM Normal Double Buffer Function

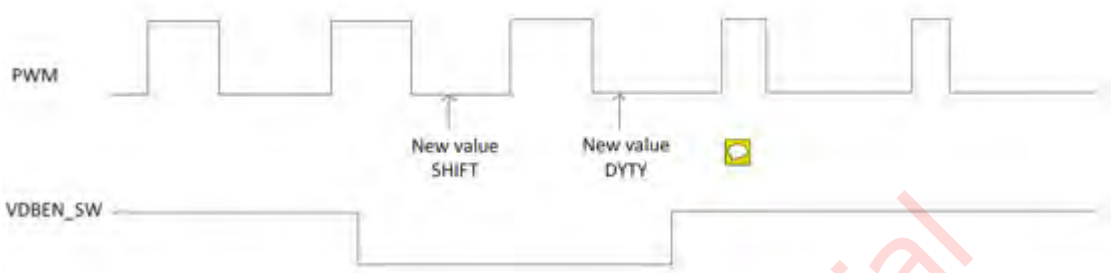


Figure 1-2: PWM SW Double Buffer Function (VDBEN_SW = ctrl H/L)

A PWM could be shifted to a phase different from that of other PWMs.
For example, suppose PWM0 and PWM1 are both 120Hz with duty cycle of 25%, but PWM1 is phase shifted 180° as opposed to PMW0. You can set the following values, and modify the shift value (rise edge) and duty value (fall edge) for PWM1 to shift.

PWM0: period value = 12000000/120 = 0x186A0
Duty value = 1/4 * period = 0x61A8
PWM1: period value = 12000000/120 = 0x186A0
Shift value = 0x186A0 * 180/360 = 0xC350
Duty value = 0xC350 + 0x61A8 = 0x124F8

The waveform will then be as shown in Figure 1-3 below.

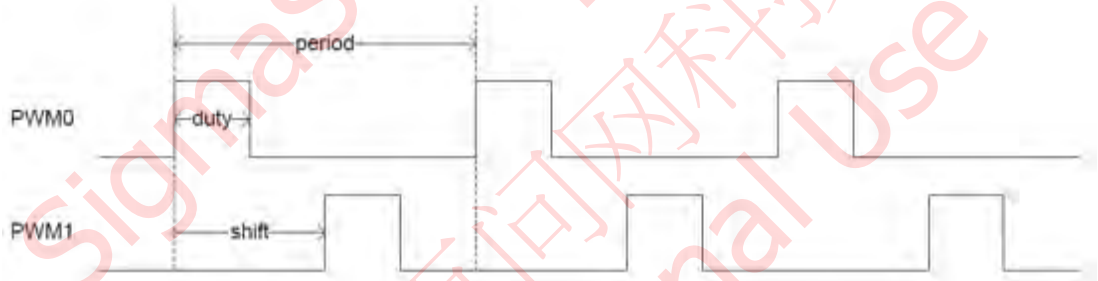


Figure 1-3: PWM Shift Function

According to the above discussion, we can generate four different pulses in a period by setting shift 1~4 and duty 1~4. For this purpose, reg_diff_p_en should be high.

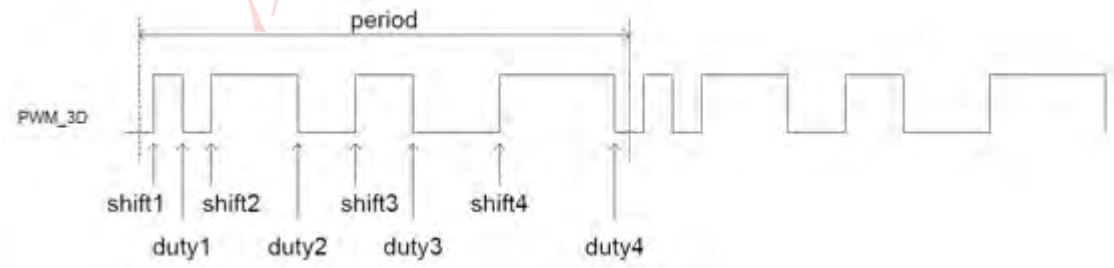
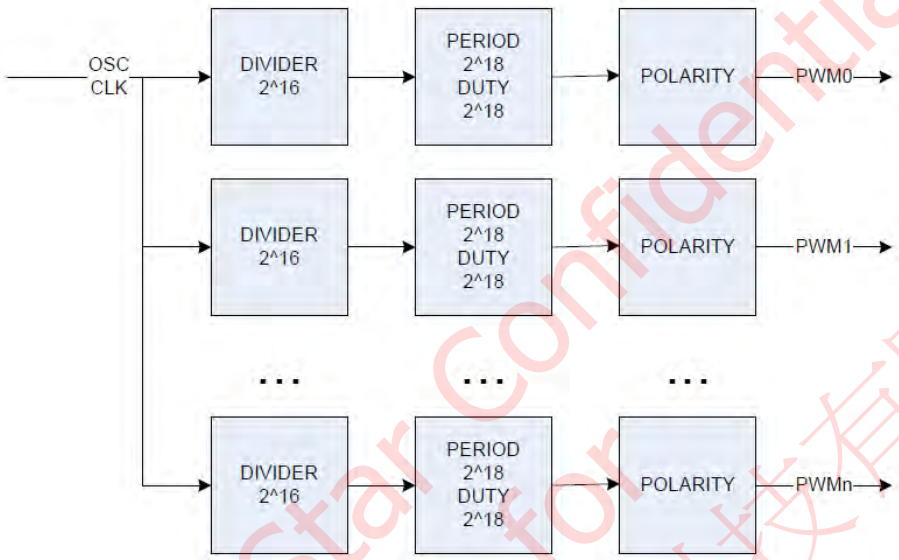


Figure 1-4: PWM Multiple Pulse Function

Period and Divider setting:

For those applications to which accuracy is imperative, please use period/duty bits instead of divider bits. For example, if you need a 150Hz PWM frequency, set period = 80000 (1387Fh) instead of setting divider = 100 (63h) and period = 800 (31Fh). The reason is that, if you need to fine tune to 150.1Hz, you just need to change the period to 79947 (1384Ah) to get the result of 150.099Hz. But if you use the divider option, you will need to change the period to 799, to get a less precise result of 150.188Hz.



1.4. Sync Mode Description and Interrupt Function

In order to sync PWM, each group need to have the same period and div setting if the PWM sync mode is enabled. Delay counter will start counting after it is enabled for each group. Group0 controls PWM0~3. When sync mode is enabled, only hold mode, N round mode and stop mode are supported.

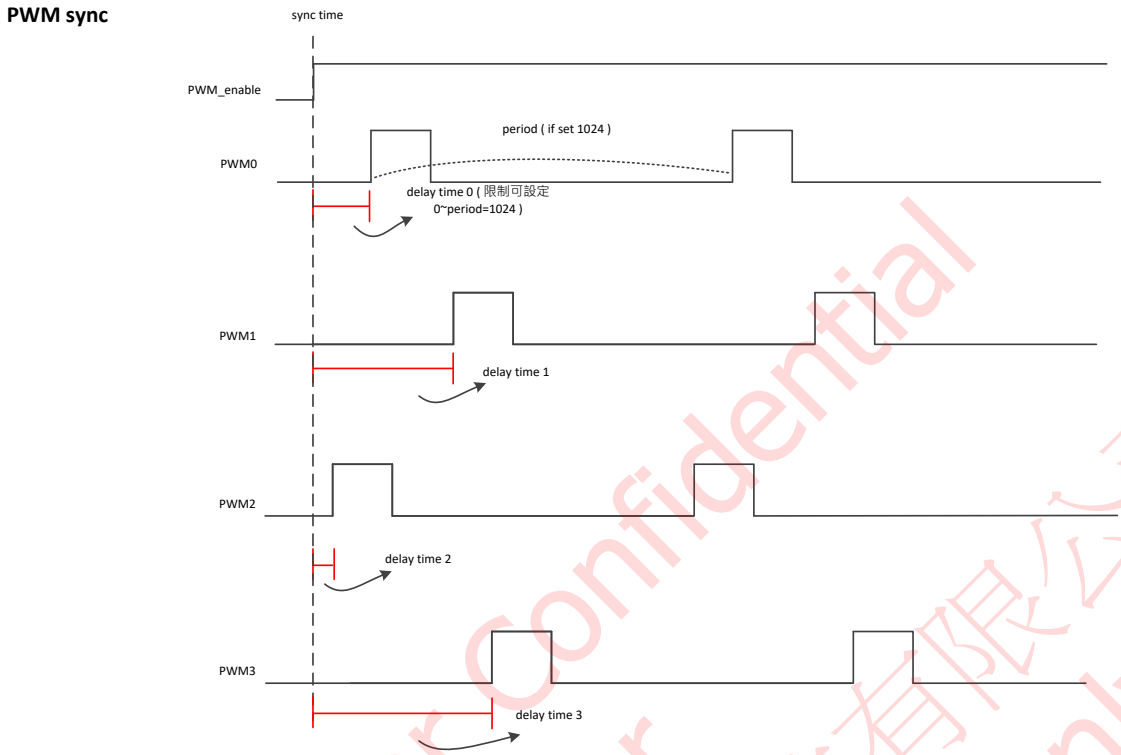


Figure 1-5: PWM Sync Mode

1.5. Hold Mode 0 Description

Hold mode will hold the PWM value after current period is finished. Users can change the PWM setting after getting PWM hold interrupt. PWM will restart with the new setting after group hold mode is disabled.

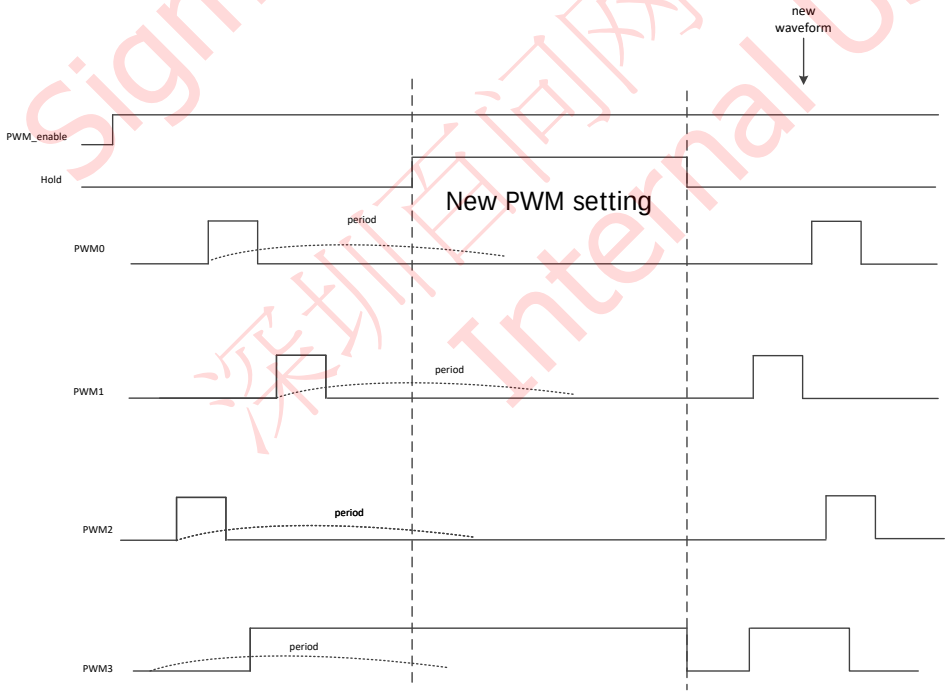


Figure 1-6: PWM Hold Mode

1.6. Hold Mode 1 Description

Hold mode 1 is the same as Hold mode 0, except that it will set PWM value = 0 after the current period is finished. All you need to do is to enable reg_pwm_hold_mode1.

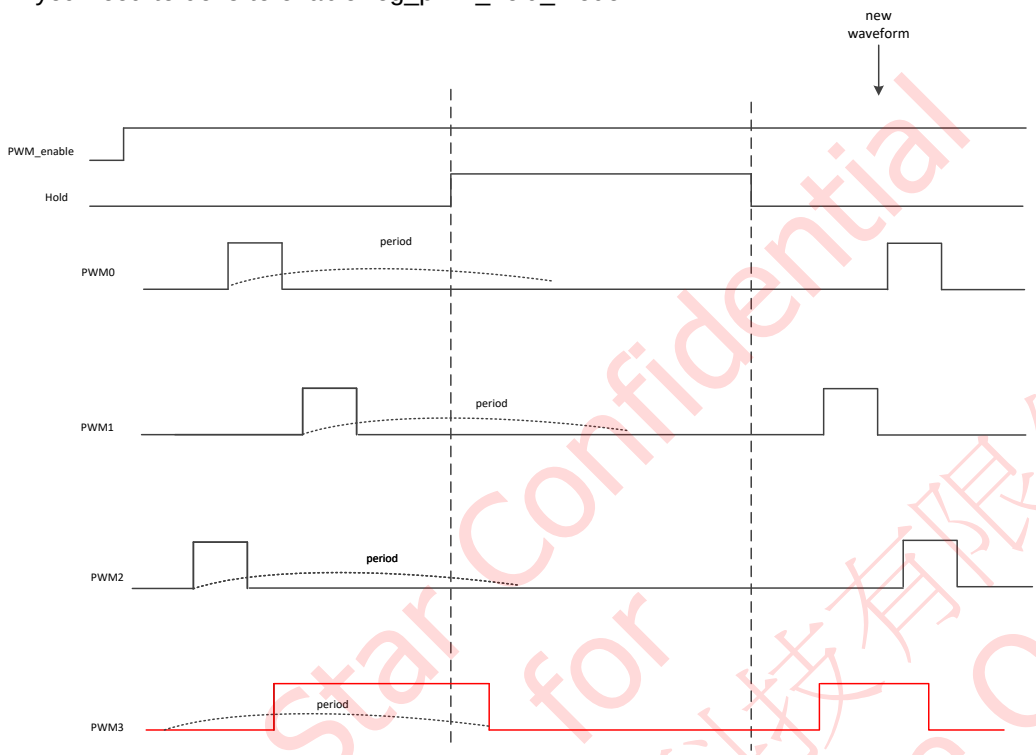


Figure 1-7: PWM Hold Mode

1.7. Stop Mode Description

Stop mode will cause the PWM to stop immediately with no restart availability. So it is used in urgent cases only. To restart PWM after it has been stopped through the Stop mode, use software reset.

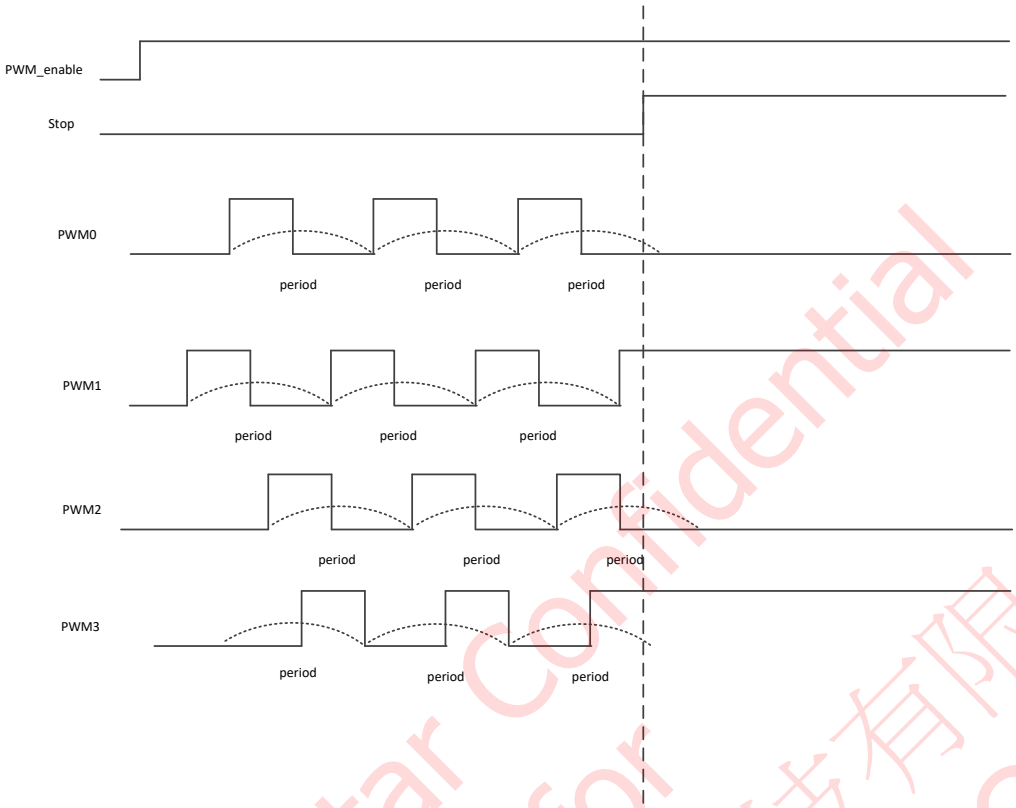


Figure 1-8: PWM Stop Mode

1.8. N Round Mode Description

N round mode can generate the number of pulses required by setting the corresponding parameter. If the parameter is set to 0, PWM will generate pulses continuously. You can restart PWM through group enable after receiving PWM interrupt.

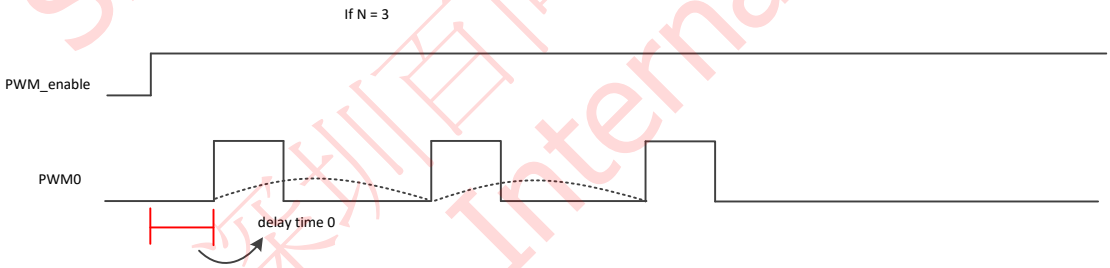


Figure 1-9: PWM N Round Mode

2. REGISTER DESCRIPTION

2.1. PWM Register (Bank = 1A)

PWM Register (Bank = 1A)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (1A00h)	REG1A00	7:0	Default : 0x00	Access : R/W
	PWM0_SHIFT[7:0]	7:0	PWM0 rising point shift counter.	
00h (1A01h)	REG1A01	7:0	Default : 0x00	Access : R/W
	PWM0_SHIFT[15:8]	7:0	See description of '1A00h'.	
01h (1A02h)	REG1A02	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	PWM0_SHIFT[17:16]	1:0	See description of '1A00h'.	
02h (1A04h)	REG1A04	7:0	Default : 0x00	Access : R/W
	PWM0_DUTY[7:0]	7:0	PWM0 duty.	
02h (1A05h)	REG1A05	7:0	Default : 0x00	Access : R/W
	PWM0_DUTY[15:8]	7:0	See description of '1A04h'.	
03h (1A06h)	REG1A06	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	PWM0_DUTY[17:16]	1:0	See description of '1A04h'.	
04h (1A08h)	REG1A08	7:0	Default : 0x00	Access : R/W
	PWM0_PERIOD[7:0]	7:0	PWM0 period.	
04h (1A09h)	REG1A09	7:0	Default : 0x00	Access : R/W
	PWM0_PERIOD[15:8]	7:0	See description of '1A08h'.	
05h (1A0Ah)	REG1A0A	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	PWM0_PERIOD[17:16]	1:0	See description of '1A08h'.	
06h (1A0Ch)	REG1A0C	7:0	Default : 0x00	Access : R/W
	PWM0_DIV[7:0]	7:0	PWM0 divider.	
06h (1A0Dh)	REG1A0D	7:0	Default : 0x00	Access : R/W
	PWM0_DIV[15:8]	7:0	See description of '1A0Ch'.	
07h (1A0Eh)	REG1A0E	7:0	Default : 0x01	Access : R/W
	-	7:5	Reserved.	
	PWM0_POLARITY	4	PWM0 polarity.	

PWM Register (Bank = 1A)				
Index (Absolute)	Mnemonic	Bit	Description	
	PWM0_SHIFT_GAT	3	PWM0 enable shift counter gating.	
	PWM0_DIFF_P_EN	2	Enable multiple differential pulse width mode.	
	PWM0_DBEN	1	PWM0 double buffer enable.	
	PWM0_VDBEN_SW	0	PWM0 double buffer enable by software. 1: Enable, 0: Disable.	
08h (1A10h)	REG1A10	7:0	Default : 0xFF	Access : R/W
	PWM0_SHIFT2[7:0]	7:0	PWM0 rising point shift2 counter.	
08h (1A11h)	REG1A11	7:0	Default : 0xFF	Access : R/W
	PWM0_SHIFT2[15:8]	7:0	See description of '1A10h'.	
09h (1A12h)	REG1A12	7:0	Default : 0xFF	Access : R/W
	PWM0_DUTY2[7:0]	7:0	PWM0 duty2.	
09h (1A13h)	REG1A13	7:0	Default : 0xFF	Access : R/W
	PWM0_DUTY2[15:8]	7:0	See description of '1A12h'.	
0Ah (1A14h)	REG1A14	7:0	Default : 0xFF	Access : R/W
	PWM0_SHIFT3[7:0]	7:0	PWM0 rising point shift3 counter.	
0Ah (1A15h)	REG1A15	7:0	Default : 0xFF	Access : R/W
	PWM0_SHIFT3[15:8]	7:0	See description of '1A14h'.	
0Bh (1A16h)	REG1A16	7:0	Default : 0xFF	Access : R/W
	PWM0_DUTY3[7:0]	7:0	PWM0 duty3.	
0Bh (1A17h)	REG1A17	7:0	Default : 0xFF	Access : R/W
	PWM0_DUTY3[15:8]	7:0	See description of '1A16h'.	
0Ch (1A18h)	REG1A18	7:0	Default : 0xFF	Access : R/W
	PWM0_SHIFT4[7:0]	7:0	PWM0 rising point shift4 counter.	
0Ch (1A19h)	REG1A19	7:0	Default : 0xFF	Access : R/W
	PWM0_SHIFT4[15:8]	7:0	See description of '1A18h'.	
0Dh (1A1Ah)	REG1A1A	7:0	Default : 0xFF	Access : R/W
	PWM0_DUTY4[7:0]	7:0	PWM0 duty4.	
0Dh (1A1Bh)	REG1A1B	7:0	Default : 0xFF	Access : R/W
	PWM0_DUTY4[15:8]	7:0	See description of '1A1Ah'.	
10h (1A20h)	REG1A20	7:0	Default : 0x00	Access : R/W
	GROUP0_ROUND_NUMBER[7:0]	7:0	Round number for group0.	
10h	REG1A21	7:0	Default : 0x00	Access : R/W

PWM Register (Bank = 1A)				
Index (Absolute)	Mnemonic	Bit	Description	
(1A21h)	GROUP0_ROUND_NUMBER[15:8]	7:0	See description of '1A20h'.	
11h (1A22h)	REG1A22	7:0	Default : 0x00	Access : R/W
	GROUP0_PWM0_DELAY_COUNT[7:0]	7:0	GROUP0_PWM0_DELAY_COUNT.	
11h (1A23h)	REG1A23	7:0	Default : 0x00	Access : R/W
	GROUP0_PWM0_DELAY_COUNT[15:8]	7:0	See description of '1A22h'.	
12h (1A24h)	REG1A24	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	GROUP0_PWM0_DELAY_COUNT[17:16]	1:0	See description of '1A22h'.	
13h (1A26h)	REG1A26	7:0	Default : 0x00	Access : R/W
	GROUP0_PWM1_DELAY_COUNT[7:0]	7:0	GROUP0_PWM1_DELAY_COUNT.	
13h (1A27h)	REG1A27	7:0	Default : 0x00	Access : R/W
	GROUP0_PWM1_DELAY_COUNT[15:8]	7:0	See description of '1A26h'.	
14h (1A28h)	REG1A28	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	GROUP0_PWM1_DELAY_COUNT[17:16]	1:0	See description of '1A26h'.	
15h (1A2Ah)	REG1A2A	7:0	Default : 0x00	Access : R/W
	GROUP0_PWM2_DELAY_COUNT[7:0]	7:0	GROUP0_PWM2_DELAY_COUNT.	
15h (1A2Bh)	REG1A2B	7:0	Default : 0x00	Access : R/W
	GROUP0_PWM2_DELAY_COUNT[15:8]	7:0	See description of '1A2Ah'.	
16h (1A2Ch)	REG1A2C	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	GROUP0_PWM2_DELAY_COUNT[17:16]	1:0	See description of '1A2Ah'.	
17h (1A2Eh)	REG1A2E	7:0	Default : 0x00	Access : R/W
	GROUP0_PWM3_DELAY_COUNT[7:0]	7:0	GROUP0_PWM3_DELAY_COUNT.	

PWM Register (Bank = 1A)				
Index (Absolute)	Mnemonic	Bit	Description	
17h (1A2Fh)	REG1A2F	7:0	Default : 0x00	Access : R/W
	GROUP0_PWM3_DELAY_COUNT[15:8]	7:0	See description of '1A2Eh'.	
18h (1A30h)	REG1A30	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	GROUP0_PWM3_DELAY_COUNT[17:16]	1:0	See description of '1A2Eh'.	
20h (1A40h)	REG1A40	7:0	Default : 0x00	Access : R/W
	PWM1_SHIFT[7:0]	7:0	PWM1 rising point shift counter.	
20h (1A41h)	REG1A41	7:0	Default : 0x00	Access : R/W
	PWM1_SHIFT[15:8]	7:0	See description of '1A40h'.	
21h (1A42h)	REG1A42	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	PWM1_SHIFT[17:16]	1:0	See description of '1A40h'.	
22h (1A44h)	REG1A44	7:0	Default : 0x00	Access : R/W
	PWM1_DUTY[7:0]	7:0	PWM1 duty.	
22h (1A45h)	REG1A45	7:0	Default : 0x00	Access : R/W
	PWM1_DUTY[15:8]	7:0	See description of '1A44h'.	
23h (1A46h)	REG1A46	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	PWM1_DUTY[17:16]	1:0	See description of '1A44h'.	
24h (1A48h)	REG1A48	7:0	Default : 0x00	Access : R/W
	PWM1_PERIOD[7:0]	7:0	PWM1 period.	
24h (1A49h)	REG1A49	7:0	Default : 0x00	Access : R/W
	PWM1_PERIOD[15:8]	7:0	See description of '1A48h'.	
25h (1A4Ah)	REG1A4A	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	PWM1_PERIOD[17:16]	1:0	See description of '1A48h'.	
26h (1A4Ch)	REG1A4C	7:0	Default : 0x00	Access : R/W
	PWM1_DIV[7:0]	7:0	PWM1 divider.	
26h (1A4Dh)	REG1A4D	7:0	Default : 0x00	Access : R/W
	PWM1_DIV[15:8]	7:0	See description of '1A4Ch'.	
27h	REG1A4E	7:0	Default : 0x01	Access : R/W

PWM Register (Bank = 1A)				
Index (Absolute)	Mnemonic	Bit	Description	
(1A4Eh)	-	7:5	Reserved.	
	PWM1_POLARITY	4	PWM1 polarity.	
	PWM1_SHIFT_GAT	3	PWM1 enable shift counter gating.	
	PWM1_DIFF_P_EN	2	Enable multiple differential pulse width mode.	
	PWM1_DBEN	1	PWM1 double buffer enable.	
	PWM1_VDBEN_SW	0	PWM1 double buffer enable by software. 1: Enable, 0: Disable.	
28h (1A50h)	REG1A50	7:0	Default : 0xFF	Access : R/W
	PWM1_SHIFT2[7:0]	7:0	PWM1 rising point shift2 counter.	
28h (1A51h)	REG1A51	7:0	Default : 0xFF	Access : R/W
	PWM1_SHIFT2[15:8]	7:0	See description of '1A50h'.	
29h (1A52h)	REG1A52	7:0	Default : 0xFF	Access : R/W
	PWM1_DUTY2[7:0]	7:0	PWM1 duty2.	
29h (1A53h)	REG1A53	7:0	Default : 0xFF	Access : R/W
	PWM1_DUTY2[15:8]	7:0	See description of '1A52h'.	
2Ah (1A54h)	REG1A54	7:0	Default : 0xFF	Access : R/W
	PWM1_SHIFT3[7:0]	7:0	PWM1 rising point shift3 counter.	
2Ah (1A55h)	REG1A55	7:0	Default : 0xFF	Access : R/W
	PWM1_SHIFT3[15:8]	7:0	See description of '1A54h'.	
2Bh (1A56h)	REG1A56	7:0	Default : 0xFF	Access : R/W
	PWM1_DUTY3[7:0]	7:0	PWM1 duty3.	
2Bh (1A57h)	REG1A57	7:0	Default : 0xFF	Access : R/W
	PWM1_DUTY3[15:8]	7:0	See description of '1A56h'.	
2Ch (1A58h)	REG1A58	7:0	Default : 0xFF	Access : R/W
	PWM1_SHIFT4[7:0]	7:0	PWM1 rising point shift4 counter.	
2Ch (1A59h)	REG1A59	7:0	Default : 0xFF	Access : R/W
	PWM1_SHIFT4[15:8]	7:0	See description of '1A58h'.	
2Dh (1A5Ah)	REG1A5A	7:0	Default : 0xFF	Access : R/W
	PWM1_DUTY4[7:0]	7:0	PWM1 duty4.	
2Dh (1A5Bh)	REG1A5B	7:0	Default : 0xFF	Access : R/W
	PWM1_DUTY4[15:8]	7:0	See description of '1A5Ah'.	
30h (1A60h)	REG1A60	7:0	Default : 0x00	Access : R/W
	GROUP1_ROUND_NUMBER[	7:0	Round number for group1.	

PWM Register (Bank = 1A)				
Index (Absolute)	Mnemonic	Bit	Description	
	7:0]			
30h (1A61h)	REG1A61	7:0	Default : 0x00	Access : R/W
	GROUP1_ROUND_NUMBER[15:8]	7:0	See description of '1A60h'.	
31h (1A62h)	REG1A62	7:0	Default : 0x00	Access : R/W
	GROUP1_PWM0_DELAY_COUNT[7:0]	7:0	GROUP1_PWM0_DELAY_COUNT.	
31h (1A63h)	REG1A63	7:0	Default : 0x00	Access : R/W
	GROUP1_PWM0_DELAY_COUNT[15:8]	7:0	See description of '1A62h'.	
32h (1A64h)	REG1A64	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	GROUP1_PWM0_DELAY_COUNT[17:16]	1:0	See description of '1A62h'.	
33h (1A66h)	REG1A66	7:0	Default : 0x00	Access : R/W
	GROUP1_PWM1_DELAY_COUNT[7:0]	7:0	GROUP1_PWM1_DELAY_COUNT.	
33h (1A67h)	REG1A67	7:0	Default : 0x00	Access : R/W
	GROUP1_PWM1_DELAY_COUNT[15:8]	7:0	See description of '1A66h'.	
34h (1A68h)	REG1A68	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	GROUP1_PWM1_DELAY_COUNT[17:16]	1:0	See description of '1A66h'.	
35h (1A6Ah)	REG1A6A	7:0	Default : 0x00	Access : R/W
	GROUP1_PWM2_DELAY_COUNT[7:0]	7:0	GROUP1_PWM2_DELAY_COUNT.	
35h (1A6Bh)	REG1A6B	7:0	Default : 0x00	Access : R/W
	GROUP1_PWM2_DELAY_COUNT[15:8]	7:0	See description of '1A6Ah'.	
36h (1A6Ch)	REG1A6C	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	GROUP1_PWM2_DELAY_COUNT[17:16]	1:0	See description of '1A6Ah'.	
37h	REG1A6E	7:0	Default : 0x00	Access : R/W

PWM Register (Bank = 1A)				
Index (Absolute)	Mnemonic	Bit	Description	
(1A6Eh)	GROUP1_PWM3_DELAY_COUNT[7:0]	7:0	GROUP1_PWM3_DELAY_COUNT.	
37h (1A6Fh)	REG1A6F	7:0	Default : 0x00	Access : R/W
	GROUP1_PWM3_DELAY_COUNT[15:8]	7:0	See description of '1A6Eh'.	
38h (1A70h)	REG1A70	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	GROUP1_PWM3_DELAY_COUNT[17:16]	1:0	See description of '1A6Eh'.	
40h (1A80h)	REG1A80	7:0	Default : 0x00	Access : R/W
	PWM2_SHIFT[7:0]	7:0	PWM2 rising point shift counter.	
40h (1A81h)	REG1A81	7:0	Default : 0x00	Access : R/W
	PWM2_SHIFT[15:8]	7:0	See description of '1A80h'.	
41h (1A82h)	REG1A82	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	PWM2_SHIFT[17:16]	1:0	See description of '1A80h'.	
42h (1A84h)	REG1A84	7:0	Default : 0x00	Access : R/W
	PWM2_DUTY[7:0]	7:0	PWM2 duty.	
42h (1A85h)	REG1A85	7:0	Default : 0x00	Access : R/W
	PWM2_DUTY[15:8]	7:0	See description of '1A84h'.	
43h (1A86h)	REG1A86	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	PWM2_DUTY[17:16]	1:0	See description of '1A84h'.	
44h (1A88h)	REG1A88	7:0	Default : 0x00	Access : R/W
	PWM2_PERIOD[7:0]	7:0	PWM2 period.	
44h (1A89h)	REG1A89	7:0	Default : 0x00	Access : R/W
	PWM2_PERIOD[15:8]	7:0	See description of '1A88h'.	
45h (1A8Ah)	REG1A8A	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	PWM2_PERIOD[17:16]	1:0	See description of '1A88h'.	
46h (1A8Ch)	REG1A8C	7:0	Default : 0x00	Access : R/W
	PWM2_DIV[7:0]	7:0	PWM2 divider.	
46h (1A8Dh)	REG1A8D	7:0	Default : 0x00	Access : R/W
	PWM2_DIV[15:8]	7:0	See description of '1A8Ch'.	

PWM Register (Bank = 1A)				
Index (Absolute)	Mnemonic	Bit	Description	
47h (1A8Eh)	REG1A8E	7:0	Default : 0x01	Access : R/W
	-	7:5	Reserved.	
	PWM2_POLARITY	4	PWM2 polarity.	
	PWM2_SHIFT_GAT	3	PWM2 enable shift counter gating.	
	PWM2_DIFF_P_EN	2	Enable multiple differential pulse width mode.	
	PWM2_DBEN	1	PWM2 double buffer enable.	
	PWM2_VDBEN_SW	0	PWM2 double buffer enable by software. 1: Enable, 0: Disable.	
48h (1A90h)	REG1A90	7:0	Default : 0xFF	Access : R/W
	PWM2_SHIFT2[7:0]	7:0	PWM2 rising point shift2 counter.	
48h (1A91h)	REG1A91	7:0	Default : 0xFF	Access : R/W
	PWM2_SHIFT2[15:8]	7:0	See description of '1A90h'.	
49h (1A92h)	REG1A92	7:0	Default : 0xFF	Access : R/W
	PWM2_DUTY2[7:0]	7:0	PWM2 duty2.	
49h (1A93h)	REG1A93	7:0	Default : 0xFF	Access : R/W
	PWM2_DUTY2[15:8]	7:0	See description of '1A92h'.	
4Ah (1A94h)	REG1A94	7:0	Default : 0xFF	Access : R/W
	PWM2_SHIFT3[7:0]	7:0	PWM2 rising point shift3 counter.	
4Ah (1A95h)	REG1A95	7:0	Default : 0xFF	Access : R/W
	PWM2_SHIFT3[15:8]	7:0	See description of '1A94h'.	
4Bh (1A96h)	REG1A96	7:0	Default : 0xFF	Access : R/W
	PWM2_DUTY3[7:0]	7:0	PWM2 duty3.	
4Bh (1A97h)	REG1A97	7:0	Default : 0xFF	Access : R/W
	PWM2_DUTY3[15:8]	7:0	See description of '1A96h'.	
4Ch (1A98h)	REG1A98	7:0	Default : 0xFF	Access : R/W
	PWM2_SHIFT4[7:0]	7:0	PWM2 rising point shift4 counter.	
4Ch (1A99h)	REG1A99	7:0	Default : 0xFF	Access : R/W
	PWM2_SHIFT4[15:8]	7:0	See description of '1A98h'.	
4Dh (1A9Ah)	REG1A9A	7:0	Default : 0xFF	Access : R/W
	PWM2_DUTY4[7:0]	7:0	PWM2 duty4.	
4Dh (1A9Bh)	REG1A9B	7:0	Default : 0xFF	Access : R/W
	PWM2_DUTY4[15:8]	7:0	See description of '1A9Ah'.	
50h	REG1AA0	7:0	Default : 0x00	Access : R/W

PWM Register (Bank = 1A)				
Index (Absolute)	Mnemonic	Bit	Description	
(1AA0h)	GROUP2_ROUND_NUMBER[7:0]	7:0	Round number for group2.	
50h (1AA1h)	REG1AA1	7:0	Default : 0x00	Access : R/W
	GROUP2_ROUND_NUMBER[15:8]	7:0	See description of '1AA0h'.	
51h (1AA2h)	REG1AA2	7:0	Default : 0x00	Access : R/W
	GROUP2_PWM0_DELAY_COUNT[7:0]	7:0	GROUP2_PWM0_DELAY_COUNT.	
51h (1AA3h)	REG1AA3	7:0	Default : 0x00	Access : R/W
	GROUP2_PWM0_DELAY_COUNT[15:8]	7:0	See description of '1AA2h'.	
52h (1AA4h)	REG1AA4	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	GROUP2_PWM0_DELAY_COUNT[17:16]	1:0	See description of '1AA2h'.	
53h (1AA6h)	REG1AA6	7:0	Default : 0x00	Access : R/W
	GROUP2_PWM1_DELAY_COUNT[7:0]	7:0	GROUP2_PWM1_DELAY_COUNT.	
53h (1AA7h)	REG1AA7	7:0	Default : 0x00	Access : R/W
	GROUP2_PWM1_DELAY_COUNT[15:8]	7:0	See description of '1AA6h'.	
54h (1AA8h)	REG1AA8	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	GROUP2_PWM1_DELAY_COUNT[17:16]	1:0	See description of '1AA6h'.	
55h (1AAAh)	REG1AAA	7:0	Default : 0x00	Access : R/W
	GROUP2_PWM2_DELAY_COUNT[7:0]	7:0	GROUP2_PWM2_DELAY_COUNT.	
55h (1AABh)	REG1AAB	7:0	Default : 0x00	Access : R/W
	GROUP2_PWM2_DELAY_COUNT[15:8]	7:0	See description of '1AAAh'.	
56h (1AACh)	REG1AAC	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	GROUP2_PWM2_DELAY_COUNT[17:16]	1:0	See description of '1AAAh'.	

PWM Register (Bank = 1A)				
Index (Absolute)	Mnemonic	Bit	Description	
60h (1AC0h)	REG1AC0	7:0	Default : 0x00	Access : R/W
	PWM3_SHIFT[7:0]	7:0	PWM3 rising point shift counter.	
60h (1AC1h)	REG1AC1	7:0	Default : 0x00	Access : R/W
	PWM3_SHIFT[15:8]	7:0	See description of '1AC0h'.	
61h (1AC2h)	REG1AC2	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	PWM3_SHIFT[17:16]	1:0	See description of '1AC0h'.	
62h (1AC4h)	REG1AC4	7:0	Default : 0x00	Access : R/W
	PWM3_DUTY[7:0]	7:0	PWM3 duty.	
62h (1AC5h)	REG1AC5	7:0	Default : 0x00	Access : R/W
	PWM3_DUTY[15:8]	7:0	See description of '1AC4h'.	
63h (1AC6h)	REG1AC6	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	PWM3_DUTY[17:16]	1:0	See description of '1AC4h'.	
64h (1AC8h)	REG1AC8	7:0	Default : 0x00	Access : R/W
	PWM3_PERIOD[7:0]	7:0	PWM3 period.	
64h (1AC9h)	REG1AC9	7:0	Default : 0x00	Access : R/W
	PWM3_PERIOD[15:8]	7:0	See description of '1AC8h'.	
65h (1ACAh)	REG1ACA	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	PWM3_PERIOD[17:16]	1:0	See description of '1AC8h'.	
66h (1ACCh)	REG1ACC	7:0	Default : 0x00	Access : R/W
	PWM3_DIV[7:0]	7:0	PWM3 divider.	
66h (1ACDh)	REG1ACD	7:0	Default : 0x00	Access : R/W
	PWM3_DIV[15:8]	7:0	See description of '1ACCh'.	
67h (1ACEh)	REG1ACE	7:0	Default : 0x01	Access : R/W
	-	7:5	Reserved.	
	PWM3_POLARITY	4	PWM3 polarity.	
	PWM3_SHIFT_GAT	3	PWM3 enable shift counter gating.	
	PWM3_DIFF_P_EN	2	Enable multiple differential pulse width mode.	
	PWM3_DBEN	1	PWM3 double buffer enable.	
	PWM3_VDBEN_SW	0	PWM3 double buffer enable by software. 1: Enable, 0: Disable.	

PWM Register (Bank = 1A)				
Index (Absolute)	Mnemonic	Bit	Description	
68h (1AD0h)	REG1AD0	7:0	Default : 0xFF	Access : R/W
	PWM3_SHIFT2[7:0]	7:0	PWM3 rising point shift2 counter.	
68h (1AD1h)	REG1AD1	7:0	Default : 0xFF	Access : R/W
	PWM3_SHIFT2[15:8]	7:0	See description of '1AD0h'.	
69h (1AD2h)	REG1AD2	7:0	Default : 0xFF	Access : R/W
	PWM3_DUTY2[7:0]	7:0	PWM3 duty2.	
69h (1AD3h)	REG1AD3	7:0	Default : 0xFF	Access : R/W
	PWM3_DUTY2[15:8]	7:0	See description of '1AD2h'.	
6Ah (1AD4h)	REG1AD4	7:0	Default : 0xFF	Access : R/W
	PWM3_SHIFT3[7:0]	7:0	PWM3 rising point shift3 counter.	
6Ah (1AD5h)	REG1AD5	7:0	Default : 0xFF	Access : R/W
	PWM3_SHIFT3[15:8]	7:0	See description of '1AD4h'.	
6Bh (1AD6h)	REG1AD6	7:0	Default : 0xFF	Access : R/W
	PWM3_DUTY3[7:0]	7:0	PWM3 duty3.	
6Bh (1AD7h)	REG1AD7	7:0	Default : 0xFF	Access : R/W
	PWM3_DUTY3[15:8]	7:0	See description of '1AD6h'.	
6Ch (1AD8h)	REG1AD8	7:0	Default : 0xFF	Access : R/W
	PWM3_SHIFT4[7:0]	7:0	PWM3 rising point shift4 counter.	
6Ch (1AD9h)	REG1AD9	7:0	Default : 0xFF	Access : R/W
	PWM3_SHIFT4[15:8]	7:0	See description of '1AD8h'.	
6Dh (1ADAh)	REG1ADA	7:0	Default : 0xFF	Access : R/W
	PWM3_DUTY4[7:0]	7:0	PWM3 duty4.	
6Dh (1ADBh)	REG1ADB	7:0	Default : 0xFF	Access : R/W
	PWM3_DUTY4[15:8]	7:0	See description of '1ADAh'.	
71h (1AE2h)	REG1AE2	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	HOLD_MODE[2:0]	2:0	[0] 1: Group0 hold mode enable. 0: Group0 hold mode disable. [1] 1: Group1 hold mode enable. 0: Group1 hold mode disable. [2] 1: Group2 hold mode enable. 0: Group2 hold mode disable.	
72h (1AE4h)	REG1AE4	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	

PWM Register (Bank = 1A)				
Index (Absolute)	Mnemonic	Bit	Description	
	STOP_MODE[2:0]	2:0	[0] 1: Group0 stop mode enable. 0: Group0 stop mode disable. [1] 1: Group1 stop mode enable. 0: Group1 stop mode disable. [2] 1: Group2 stop mode enable. 0: Group2 stop mode disable.	
73h (1AE6h)	REG1AE6	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	PWM_ENABLE[2:0]	2:0	[0] 1: PWM group0 enable, 0: group0 disable. [1] 1: PWM group1 enable, 0: group1 disable. [2] 1: PWM group2 enable, 0: group2 disable.	
74h (1AE8h)	REG1AE8	7:0	Default : 0x00	Access : R/W
	SYNC_MODE_EN[7:0]	7:0	[0] 1: PWM0 sync mode enable. [1] 1: PWM1 sync mode enable. ... [10] 1: PWM10 sync mode enable. for PWM10~0.	
74h (1AE9h)	REG1AE9	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	SYNC_MODE_EN[10:8]	2:0	See description of '1AE8h'.	
75h (1AEAh)	REG1AEA	7:0	Default : 0x00	Access : RO
	-	7:2	Reserved.	
	PWM_INT[1:0]	1:0	[0]: PWM group0 hold int. [1]: PWM group0 round int.	
7Eh (1AFCh)	REG1AFC	7:0	Default : 0x00	Access : RO
	PWM_OUT[7:0]	7:0	PWM output.	
7Eh (1AFDh)	REG1AFD	7:0	Default : 0x00	Access : RO
	-	7:3	Reserved.	
	PWM_OUT[10:8]	2:0	See description of '1AFCh'.	
7Fh (1AFEh)	REG1AFE	7:0	Default : 0x00	Access : R/W
	PWM7_SW_RST	7	PWM7 software reset.	
	PWM6_SW_RST	6	PWM6 software reset.	
	PWM5_SW_RST	5	PWM5 software reset.	
	PWM4_SW_RST	4	PWM4 software reset.	
	PWM3_SW_RST	3	PWM3 software reset.	

PWM Register (Bank = 1A)				
Index (Absolute)	Mnemonic	Bit	Description	
	PWM2_SW_RST	2	PWM2 software reset.	
	PWM1_SW_RST	1	PWM1 software reset.	
	PWM0_SW_RST	0	PWM0 software reset.	
7Fh (1AFFh)	REG1AFF	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	GROUP2_SW_RST	5	Group2 software reset.	
	GROUP1_SW_RST	4	Group1 software reset.	
	GROUP0_SW_RST	3	Group0 software reset.	
	PWM10_SW_RST	2	PWM10 software reset.	
	PWM9_SW_RST	1	PWM9 software reset.	
	PWM8_SW_RST	0	PWM8 software reset.	