SSD202D
CLKGEN Module Description

1. REGISTER DESCRIPTION

1.1. CLKGEN Register (Bank = 1038)

CLKGEN Register (Bank = 1038)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (103800h)	REG103800	7:0	Default : 0x00	Access : R/W
	CKG_XTALI_SC_GP[3:0]	7:4	Xtali clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: select clock source. 00: 12MHz (xtali). others: No clocks.	
	CKG_XTALI[3:0]	3:0	Xtali clock setting (only for HEMCU). [0]: Disable clock. [1]: Invert clock. [3:2]: select clock source. 00: 12MHz (xtali). others: No clocks.	
00h (103801h)	REG103801	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	CKG_LIVE[3:0]	3:0	Live clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: select clock source. 00: 12MHz (xtali). others: No clocks.	
01h (103802h)	REG103802	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	CKG_MCU[5:0]	5:0	Clk_mcu clock setting. [0]: Disable clock. [1]: Invert clock. [4: 2]: select clock source. 000: 216MHz. 001: 172MHz. 010: 144HMz. 011: 54MHz.	

CLKGEN Register (Bank = 1038)				
Index (Absolute)	Mnemonic	Bit	Description	
			100: 432MHz. 101: 384MHz. 110: 320MHz. 111:108MHz. [5]: Glitch free select. 0: 12MHz (xtali). 1: Select the output according to CKG_MCU[4: 2].	
01h (103803h)	REG103803	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	CKG_RIUBRDG[3:0]	3:0	Clk_riubrdg clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: select clock source. 00: Select clk_mcu_p according to reg_ckg_mcu. others: No clocks.	
02h (103804h)	REG103804	7:0	Default : 0x01	Access : R/W
	-	7:4	Reserved.	
	CKG_BIST[3:0]	3:0	Clk_bist_p clock setting. [0]: Disable clock. [1]: Reserved. [3:2]: select clock source. 00: 172MHz. 01: 108MHz. 10: 54MHz. 11: 12MHz (xtali).	
03h (103806h)	REG103806	7:0	Default : 0x01	Access : R/W
	-	7:4	Reserved.	
	CKG_BIST_SC_GP[3:0]	3:0	Clk_bist_sc_gp_p clock setting. [0]: Disable clock. [1]: Reserved. [3:2]: select clock source. 00: 172MHz. 01: 108MHz. 10: 54MHz. 11: 12MHz (xtali)).	
04h (103808h)	REG103808	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	CKG_PWR_CTL[3:0]	3:0	Clk_pwr_ctl clock setting.	

CLKGEN Register (Bank = 1038)				
Index (Absolute)	Mnemonic	Bit	Description	
			[0]: Disable clock. [1]: Invert clock. [3:2]: select clock source. 00: 750KHz. 01: 1.5MHz. 10: 12MHz. 11: Reserved.	
08h (103810h)	REG103810	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	CKG_BOOT[3:0]	3:0	Clk_boot_p clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: select clock source. 00: 12MHz (xtali). 01: Reserved. 10: Reserved. 11: Reserved.	
17h (10382Eh)	REG10382E	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CKG_MIU[4:0]	4:0	Clk_miu clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: select clock source. 00: Clk_miu from ddrpll (internal bus frequency can be the same as external DRAM). 01: 1'b0. 10: Clk_miu from miupll (internal bus frequency can be different from external DRAM). 11: 216MHz. [4]: Glitch free select. 0: 12MHz (xtali). 1: Select the output according to CKG_MIU[3:2].	
18h (103830h)	REG103830	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	CKG_MIU_REC[3:0]	3:0	Clk_miu_rec clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: select clock source. 00: 1.5MHz (xtali div 8).	

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Index (Absolute)	Mnemonic	Bit	Description	
			01: 750KHz (xtali div 16). 10: 187.5KHz (xtali div 64). 11: 93.75KHz (xtali div 128).	
19h (103832h)	REG103832	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	CKG_DDR_SYN[3:0]	3:0	Clk_ddr_syn clock setting. [1:0]: select clock source. 00: 432MHz. 01: 216MHz. 10: 12MHz (xtali). 11: No clock.	
20h (103840h)	REG103840	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	CKG_MIU_BOOT[2:0]	2:0	[0]: Reserved. [1]: Reserved. [2]: Select clock source. 0: Select BOOT clock 12MHz (xtali). 1: Select the output according to reg_ckg_miu[4:0].	
31h (103862h)	REG103862	7:0	Default : 0x01	Access : R/W
	-	7:4	Reserved.	
	CKG_UART0[3:0]	3:0	Clk_uart1 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: select clock source. 00: 172MHz. 01: 144MHz. 10: 12MHz(xtali). 11: No clock.	
31h (103863h)	REG103863	7:0	Default : 0x11	Access : R/W
	CKG_UART2[3:0]	7:4	Clk_uart2 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: select clock source. 00: 172MHz. 01: 144MHz. 10: 12MHz (xtali). 11: No clock.	
	CKG_UART1[3:0]	3:0	Clk_uart1 clock setting.	

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Index (Absolute)	Mnemonic	Bit	Description	
			[0]: Disable clock. [1]: Invert clock. [3:2]: select clock source. 00: 172MHz. 01: 144MHz. 10: 12MHz (xtali). 11: No clock.	
32h (103864h)	REG103864	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	CKG_SPI[5:0]	5:0	Clk_spi clock setting. [0]: Gate. [1]: Inv; [4: 2]: select clock source. 000: 216MHz. 001: 108MHz. 010: 86MHz. 011: 72MHz. 100: Clk_miu (must select this one). [5]: Select BOOT clock source (See reg_ckg_boot) (glitch free). 0: Select BOOT clock 12MHz (xtali). 1: Select the output according to CKG_SPI[4: 2].	
33h (103866h)	REG103866	7:0	Default : 0x01	Access : R/W
	-	7:4	Reserved.	
	CKG_MSPI0[3:0]	3:0	Clk_mspi0 clock setting. [0]: Gate; [1]: Inv; [3:2]: select clock source. 00: 108MHz. 01: 54MHz. 10: 12MHz (xtali). 11: 144MHz.	
33h (103867h)	REG103867	7:0	Default : 0x11	Access : R/W
	CKG_MSPI[3:0]	7:4	Clk_mspi0 clock setting. [0]: Gate; [1]: Inv; [3:2]: select clock source. 00: Clk_mspi0. 01: Clk_mspi1.	

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	CKG_MSPI1[3:0]	3:0	Clk_mspi1 clock setting. [0]: Gate; [1]: Inv; [3:2]: select clock source. 00: 108MHz. 01: 54MHz. 10: 12MHz (xtali). 11: 144MHz.	
34h (103868h)	REG103868	7:0	Default : 0x11	Access : R/W
	CKG_FUART0_SYNTH_IN[3:0]	7:4	Clk_fast_uart_syn clock setting (modem). [0]: Disable clock. [1]: Invert clock. [3:2]: select clock source. 00: 432MHz. 01: 216MHz. others: No clock.	
	CKG_FUART[3:0]	3:0	Clk_fast_uart clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: select clock source. 00: 172MHz. 01: 144MHz. 10: 12MHz (xtali). 11: Clk_fast_uart from synthesizer.	
34h (103869h)	REG103869	7:0	Default : 0x02	Access : R/W
	-	7:2	Reserved.	
	UART_STNTHESIZER_SW_RSTZ	1	FAST UART SW resetz.	
	UART_STNTHESIZER_ENABLE	0	FAST UART enable signal.	
35h (10386Ah)	REG10386A	7:0	Default : 0xA9	Access : R/W
	UART_STNTHESIZER_FIX_NF_FREQ[7:0]	7:0	FAST UART synthesizer config.	
35h (10386Bh)	REG10386B	7:0	Default : 0x45	Access : R/W
	UART_STNTHESIZER_FIX_NF_FREQ[15:8]	7:0	See description of '10386Ah'.	
36h (10386Ch)	REG10386C	7:0	Default : 0x00	Access : R/W
	UART_STNTHESIZER_FIX_NF	7:0	See description of '10386Ah'.	

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Index (Absolute)	Mnemonic	Bit	Description	
	_FREQ[23:16]			
36h (10386Dh)	REG10386D	7:0	Default : 0x00	Access : R/W
	UART_STNTHESIZER_FIX_NF_FREQ[31:24]	7:0	See description of '10386Ah'.	
37h (10386Eh)	REG10386E	7:0	Default : 0x01	Access : R/W
	-	7:4	Reserved.	
	CKG_MIIC0[3:0]	3:0	Clk_miic0 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: select clock source. 00: 72MHz. 01: 54MHz. 10: 12MHz (xtali). 11: No clock.	
37h (10386Fh)	REG10386F	7:0	Default : 0x01	Access : R/W
	-	7:4	Reserved.	
	CKG_MIIC1[3:0]	3:0	Clk_miic1 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: select clock source. 00: 72MHz. 01: 54MHz. 10: 12MHz (xtali). 11: No clock.	
42h (103884h)	REG103884	7:0	Default : 0x01	Access : R/W
	-	7:4	Reserved.	
	CKG_EMAC_AHB[3:0]	3:0	Clk_emac_ahb clock setting. [0]: Disable clock. [1]: Invert clock. [2]: Select clock source. 00: 144MHz. 01: 123MHz. 10: 86MHz. 11: Clk_emac_ahb from lan_atop.	
45h (10388Ah)	REG10388A	7:0	Default : 0x01	Access : R/W
	-	7:5	Reserved.	
	CKG_SDIO[4:0]	4:0	Clk_sdio clock setting.	

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Index (Absolute)	Mnemonic	Bit	Description	
			[0]: Disable clock. [1]: Invert clock. [4: 2]: select clock source. 000: 48MHz. 001: 43MHz. 010: 40MHz. 011: 36MHZ. 100: 32MHz. 101: 20MHz. 110: 12MHz (xtali). 111: 300MHz (xtali).	
51h (1038A2h)	REG1038A2	7:0	Default : 0x01	Access : R/W
	-	7:5	Reserved.	
	CKG_GE[4:0]	4:0	Clk_ge clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: select clock source. 000: Clk_miu. 001: 216MHz. 010: 172MHz. 011: 144MHz. 100: 320MHz. 101: 384MHz. 110: 432MHz.	
52h (1038A4h)	REG1038A4	7:0	Default : 0x01	Access : R/W
	-	7:5	Reserved.	
	CKG_DIP[4:0]	4:0	Clk_bdma clock setting. [0]: Disable clock. [1]: Invert clock. [4: 2]: select clock source. 000: 320MHz. 001: 384MHz. 010: 216MHz. 011: 192MHZ. 100: 172MHz. 101: 160MHz. .	
53h (1038A6h)	REG1038A6	7:0	Default : 0x01	Access : R/W
	-	7:4	Reserved.	

CLKGEN Register (Bank = 1038)				
Index (Absolute)	Mnemonic	Bit	Description	
	CKG_DISP_432[3:0]	3:0	Clk_disp_432 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: select clock source. 00: 432MHz.	
53h (1038A7h)	REG1038A7	7:0	Default : 0x01	Access : R/W
	-	7:4	Reserved.	
	CKG_DISP_216[3:0]	3:0	Clk_disp_216 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: select clock source. 00: 216MHz. 01: 108MHz.	
54h (1038A8h)	REG1038A8	7:0	Default : 0x01	Access : R/W
	-	7:4	Reserved.	
	CKG_MOP[3:0]	3:0	Clk_mop clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: select clock source. 00: 320MHz. 01: 384MHz. 10: 288MHz. 11: Clk_miu.	
55h (1038AAh)	REG1038AA	7:0	Default : 0x01	Access : R/W
	-	7:4	Reserved.	
	CKG_DEC_PCLK[3:0]	3:0	Clk_dec_pclk clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: select clock source. 00: 216MHz. 01: 144MHz. 10: 108MHz.	
55h (1038ABh)	REG1038AB	7:0	Default : 0x01	Access : R/W
	-	7:4	Reserved.	
	CKG_DEC_ACLK[3:0]	3:0	Clk_dec_aclk clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: select clock source.	

CLKGEN Register (Bank = 1038)				
Index (Absolute)	Mnemonic	Bit	Description	
			00: 432MHz. 01: 320MHz. 10: 216MHz.	
57h (1038AEh)	REG1038AE	7:0	Default : 0x01	Access : R/W
	-	7:4	Reserved.	
	CKG_BIST_DEC_GP[3:0]	3:0	Clk_bist_dec_gp_p clock setting. [0]: Disable clock. [1]: Reserved. [3:2]: select clock source. 00: 216MHz. 01: 172MHz. 10: 108MHz. 11: 54MHz.	
60h (1038C0h)	REG1038C0	7:0	Default : 0x01	Access : R/W
	-	7:5	Reserved.	
	CKG_BDMA[4:0]	4:0	Clk_bdma clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: select clock source. 0: Select clk_miu_p according to reg_ckg_miu. 1~3: no clocks. [4]: Select BOOT clock source (See reg_ckg_boot) (glitch free). 0: Select BOOT clock 12MHz (xtali). 1: Select BDMA clock source.	
61h (1038C2h)	REG1038C2	7:0	Default : 0x01	Access : R/W
	-	7:5	Reserved.	
	CKG_AESDMA[4:0]	4:0	Clk_aesdma clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: select clock source. 00: 86MHz. 01: 172MHz. others: No clocks. [4]: Gltich free select. 0: 12MHz (xtai). 1: Select the output according to CKG_AESDMA[3:2].	
63h	REG1038C6	7:0	Default : 0x09	Access : R/W

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Index (Absolute)	Mnemonic	Bit	Description	
(1038C6h)	-	7:6	Reserved.	
	CKG_SC_PIXEL[5:0]	5:0	Clk_sc_pixel clock setting. [0]: Disable clock. [1]: Invert clock. [5:2]: select clock source. 0000: 240MHz. 0001: 216MHz. 0010: 192MHz. 0011: 172MHz. 0100: 144MHz. 0101: 123MHz. 0110: 108MHz. 0111: 86MHz. 1000: 72MHz. 1001: 54MHz. 1010: Lpll_clk.	
6Ah (1038D4h)	REG1038D4	7:0	Default : 0x01	Access : R/W
	-	7:5	Reserved.	
	CKG_JPE[4:0]	4:0	Clk_jpe clock setting. [0]: Disable clock. [1]: Invert clock. [4: 2]: select clock source. 000: 480Mhz. 001: 216MHz. 010: 54MHz. 011: 27MHz. 100: 320MHz. 101: 384MHz. 110: 288MHz.	
6Dh (1038DAh)	REG1038DA	7:0	Default : 0x3D	Access : R/W
	-	7:6	Reserved.	
	CKG_86M_2DIGPM	5	86m clock to digpm setting, default off. [0]: Disable clock.	
	CKG_123M_2DIGPM	4	123m clock to digpm setting, default off. [0]: Disable clock.	
	CKG_144M_2DIGPM	3	144m clock to digpm setting, default off. [0]: Disable clock.	
	CKG_172M_2DIGPM	2	172m clock to digpm setting, default off.	

CLKGEN Register (Bank = 1038)				
Index (Absolute)	Mnemonic	Bit	Description	
			[0]: Disable clock.	
	CKG_216M_2DIGPM	1	216m clock to digpm setting, default on. [0]: Disable clock.	
	CKG_HEMCU_216M	0	Clk_hemcu_216m_p clock setting. [0]: Disable clock.	
6Fh (1038DEh)	REG1038DE	7:0	Default : 0x01	Access : R/W
	-	7:5	Reserved.	
	CKG_MIPI_TX_DSI[4:0]	4:0	Clk_mipi_tx_dsi clock setting. [0]: Disable clock. [1]: Invert clock. [4: 2]: select clock source. 000: Lpll_clk. 001: 160MHz(utmi). 010: 144MHz. 011:108MHz. 100: 216MHz. 101: 240MHz.	
70h (1038E0h)	REG1038E0	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	PLL_GATER_FORCE_OFF_LOCK	1	One way register to lock all force off registers.	
	PLL_GATER_FORCE_ON_LOCK	0	One way register to lock all force on registers.	
71h (1038E2h)	REG1038E2	7:0	Default : 0xFF	Access : R/W
	MPLL_345_FORCE_ON	7	MPLL_345_FORCE_ON.	
	MPLL_432_FORCE_ON	6	MPLL_432_FORCE_ON.	
	UTMI_480_FORCE_ON	5	UTMI_480_FORCE_ON.	
	UTMI_240_FORCE_ON	4	UTMI_240_FORCE_ON.	
	UTMI_192_FORCE_ON	3	UTMI_192_FORCE_ON.	
	UTMI_160_FORCE_ON	2	UTMI_160_FORCE_ON.	
	UPLL_320_FORCE_ON	1	UPLL_320_FORCE_ON.	
	UPLL_384_FORCE_ON	0	UPLL_384_FORCE_ON.	
71h (1038E3h)	REG1038E3	7:0	Default : 0xFF	Access : R/W
	PLL_RV1_FORCE_ON	7	PLL_RV1_FORCE_ON.	
	MPLL_86_FORCE_ON	6	MPLL_86_FORCE_ON.	
	MPLL_124_FORCE_ON	5	MPLL_124_FORCE_ON.	

CLKGEN Register (Bank = 1038)				
Index (Absolute)	Mnemonic	Bit	Description	
	MPLL_123_FORCE_ON	4	MPLL_123_FORCE_ON.	
	MPLL_144_FORCE_ON	3	MPLL_144_FORCE_ON.	
	MPLL_172_FORCE_ON	2	MPLL_172_FORCE_ON.	
	MPLL_216_FORCE_ON	1	MPLL_216_FORCE_ON.	
	MPLL_288_FORCE_ON	0	MPLL_288_FORCE_ON.	
72h (1038E4h)	REG1038E4	7:0	Default : 0x00	Access : R/W
	MPLL_345_FORCE_OFF	7	MPLL_345_FORCE_OFF.	
	MPLL_432_FORCE_OFF	6	MPLL_432_FORCE_OFF.	
	UTMI_480_FORCE_OFF	5	UTMI_480_FORCE_OFF.	
	UTMI_240_FORCE_OFF	4	UTMI_240_FORCE_OFF.	
	UTMI_192_FORCE_OFF	3	UTMI_192_FORCE_OFF.	
	UTMI_160_FORCE_OFF	2	UTMI_160_FORCE_OFF.	
	UPLL_320_FORCE_OFF	1	UPLL_320_FORCE_OFF.	
	UPLL_384_FORCE_OFF	0	UPLL_384_FORCE_OFF.	
72h (1038E5h)	REG1038E5	7:0	Default : 0x00	Access : R/W
	PLL_RV1_FORCE_OFF	7	PLL_RV1_FORCE_OFF.	
	MPLL_86_FORCE_OFF	6	MPLL_86_FORCE_OFF.	
	MPLL_124_FORCE_OFF	5	MPLL_124_FORCE_OFF.	
	MPLL_123_FORCE_OFF	4	MPLL_123_FORCE_OFF.	
	MPLL_144_FORCE_OFF	3	MPLL_144_FORCE_OFF.	
	MPLL_172_FORCE_OFF	2	MPLL_172_FORCE_OFF.	
	MPLL_216_FORCE_OFF	1	MPLL_216_FORCE_OFF.	
	MPLL_288_FORCE_OFF	0	MPLL_288_FORCE_OFF.	
73h (1038E6h)	REG1038E6	7:0	Default : 0x00	Access : RO
	MPLL_345_EN_RD	7	Read back mpll_345_en.	
	MPLL_432_EN_RD	6	Read back mpll_432_en.	
	UTMI_480_EN_RD	5	Read back utmi_480_en.	
	UTMI_240_EN_RD	4	Read back utmi_240_en.	
	UTMI_192_EN_RD	3	Read back utmi_192_en.	
	UTMI_160_EN_RD	2	Read back utmi_160_en.	
	UPLL_320_EN_RD	1	Read back upll_320_en.	
	UPLL_384_EN_RD	0	Read back upll_384_en.	
73h	REG1038E7	7:0	Default : 0x00	Access : RO

CLKGEN Register (Bank = 1038)				
Index (Absolute)	Mnemonic	Bit	Description	
(1038E7h)	-	7	Reserved.	
	MPLL_86_EN_RD	6	Read back mpll_86_en.	
	MPLL_124_EN_RD	5	Read back mpll_124_en.	
	MPLL_123_EN_RD	4	Read back mpll_123_en.	
	MPLL_144_EN_RD	3	Read back mpll_144_en.	
	MPLL_172_EN_RD	2	Read back mpll_172_en.	
	MPLL_216_EN_RD	1	Read back mpll_216_en.	
	MPLL_288_EN_RD	0	Read back mpll_288_en.	
7Eh (1038FCh)	REG1038FC	7:0	Default : 0x01	Access : R/W
	CLKGEN0_RESERVED0[7:0]	7:0	Clk_dec_bclk clock setting. [0]: Disable clk_dec_bclk clock. [1]: Invert clk_dec_bclk clock. [4: 2]: select clk_dec_bclk clock source. 000: 288MHz. 001: 320MHz. 010: 216MHz. 011: 172MHz. 100: 86MHz. 101: 54MHz. . Clk_dec_cclk clock setting. [8]: Disable clk_dec_bclk clock. [9]: Invert clk_dec_bclk clock. [12:10]: select clk_dec_bclk clock source. 000: 384MHz. 001: 432MHz. 010: 288MHz. 011: 216MHz. 100: 108MHz. 101: 54MHz.	
7Eh (1038FDh)	REG1038FD	7:0	Default : 0x01	Access : R/W
	CLKGEN0_RESERVED0[15:8]	7:0	See description of '1038FCh'.	
7Fh (1038FEh)	REG1038FE	7:0	Default : 0xFF	Access : R/W
	CLKGEN0_RESERVED1[7:0]	7:0	Reserved Registers.	
7Fh (1038FFh)	REG1038FF	7:0	Default : 0xFF	Access : R/W
	CLKGEN0_RESERVED1[15:8]	7:0	See description of '1038FEh'.	