

SSD202D UART/FUART Module Description







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1. MODULE DESCRIPTION

1.1. Overview

The UART module provides UART protocol to different devices. This ASIC provides two UART engines and one fast UART engine.

1.2. Function Description

The UART module has the following features:

- Supports 32-byte FIFO for read and write respectively
- Supports interrupt
- Supports auto flow control

1.3. Operating Mode

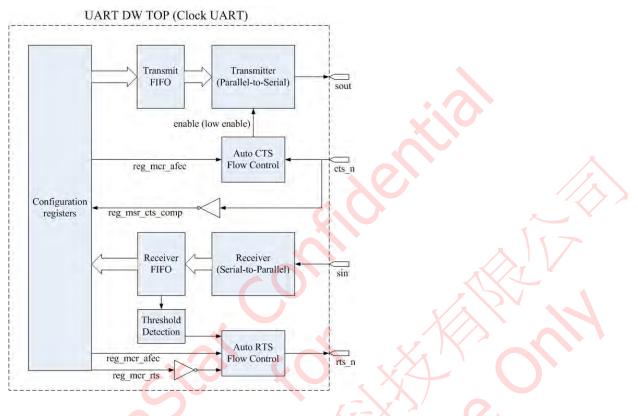
UART Protocol:

A character is composed of start bit (1 bit), data bit (5-8 bits), parity bit (1 or none) and stop bit (1, 1.5 or 2 bits).

Serial Data
Bit time
Start
Data Bits
S - 8
Parity
Stop
1, 1.5, 2
One Character



Block Diagram:



1.3.1 UART Initialization

- Set interrupt control register
- Set FIFO control register
- Set line control register
- Set auto flow control (optional)
- Set baud rate

1.3.2 UART Transmit or TX

- Write data to specified register to transmit characters
- Check line status register
- Get interrupt _____

1.3.3 UART Receive or RX

- Read data from specified register to get received characters
- Check line status register
- Get interrupt

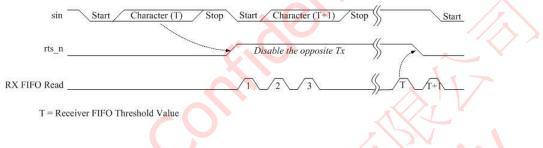
Note:

Auto Flow Control:

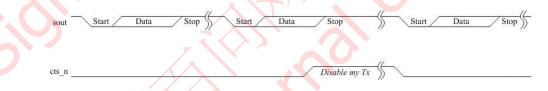
The "UART DW" can be configured to realize 16750-compatible Auto RTS/CTS serial data flow control mode.



- Auto RTS:
 - 1. Enable registers
 - 2. Timing:
 - a. The "rts_n" output is pulled high (inactive) when the RX FIFO level reaches the threshold; this will keep the opposite UART from sending data.
 - b. The "rts_n" output is pulled low (active) when the RX FIFO becomes empty by reading RBR; this will signal the opposite UART to continue sending data.
 - c. Character (T+1) may be received because "rts_n" (high) was not detected before it entered the opposite UART's transmitter.



- Auto CTS:
 - 1. Enable registers
 - 2. Timing:
 - a. The "cts_n" input is pulled high (inactive); this will keep the transmitter from sending data.
 - b. The "cts_n" input is pulled low (active); this will enable the transmission to resume.
 - c. If "cts_n" input is not pulled high before the middle of the last "stop" bit, another character may be transmitted before the transmitter is disabled.
 - d. While the transmitter is disabled, the TX FIFO can still be written and even become overflowed.



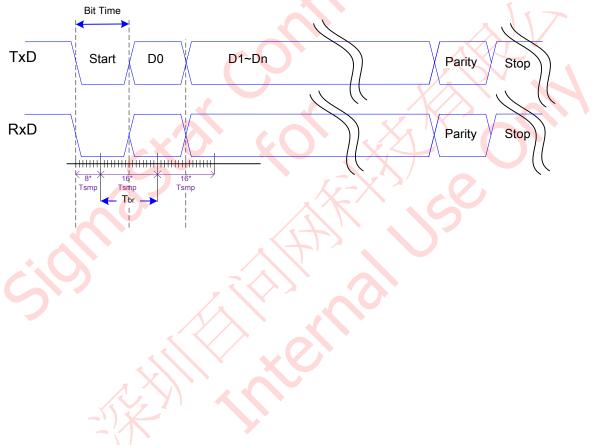


2. AC/DC SPECIFICATION

2.1. AC Characteristics

| Parameter | Symbol | Min Typ | Max | Unit |
|----------------------|--------|---------|-----|------|
| Baud Rate Period | Tbr | 115200 | | bps |
| UART Sampling Period | Tsmp | 1/16 | | Tbr |

2.2. TxD/RxD Timing





3. REGISTER DESCRIPTION

3.1. FUART Register (Bank = 1102)

| FUART Regi | ster (Bank = 1102) | | |
|----------------------|--------------------|-----|---|
| l ndex (Absolute) | Mnemonic | Bit | Description |
| 00h | REG110200 | 7:0 | Default : 0x00 Access : R/W |
| (110200h) | THR_RBR_DLL[7:0] | 7:0 | When "reg_lcr_dl_access" = 0. Write: Transmitter Holding Register. Write transmit FIFO; note that writing data to a full FIFO results in the write data being lost. Read: Receiver Buffer. Read receive FIFO; note that any incoming data are lost when FIFO is full and an overrun error occurs. When "reg_lcr_dl_access" = 1. Divisor Latch LSB. |
| 02h | REG110204 | 7:0 | Default : 0x00 Access : R/W |
| (110204h) | IER_DLH[7:0] | 7:0 | When "reg_lcr_dl_access" = 0. Interrupt Enable Registers (IER); 1: enabled. Bit [0]: Received Data Available Interrupt and Character Timeout Interrupt. Bit [1]: Transmitter Holding Register Empty Interrupt. Bit [2]: Receiver Line Status Interrupt. Bit [3]: Modem Status interrupt. Bit [7]: Programmable THRE Interrupt. When "reg_lcr_dl_access" = 1. Divisor Latch MSB. Baud rate = (serial clock freq.) / (16 * divisor). |
| 04h | REG110208 | 7:0 | Default : 0x00 Access : R/W |
| (110208h) | FCR_IIR[7:0] | 7:0 | Write. FIFO Control Register (FCR). Bit [0]: FIFO enable. Bit [1]: write "1" to clear RX FIFO. Bit [2]: write "1" to clear TX FIFO. Bit [5:4]: Transmit FIFO Empty trigger level. "00": FIFO empty; "01": 2 characters in the FIFO; "10": FIFO 1/4 full; "11": FIFO 1/2 full. |



| FUART Regi | ster (Bank = 1102) | | | |
|---------------------|---------------------|-----|--|--|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | | 5 | Bit [7:6]: Receiver FIFO Interrupt trigger level. "00": 1 character in the FIFO; "01": FIFO 1/4 full; "10": FIFO 1/2 full; "11": FIFO 2 less than full. 2. Read. Interrupt Identification Registers (IIR). Bit [0]: 1: no interrupt is pending. Bit [3:1]: interrupt identified. "110": character timeout. "011": Receiver Line Status. "010": Receiver Data Available. "001": Transmitter Holding Register empty. "000": Modem Status. | |
| 06h | REG11020C | 7:0 | Default : 0x03 Access : R/W | |
| - | LCR_DL_ACCESS | 7 | Divisor Latch Access. 1: The divisor latches can be accessed. | |
| | LCR_BREAK_CTRL | 6 | Break control bit. | |
| | | 5 | Reserved. | |
| | LCR_EVEN_PARITY_SEL | 4 | 1: Select even parity. | |
| •. C | LCR_PARITY_EN | 3 | 1: Generate parity bit on serial out. | |
| 5 | LCR_STOP_BITS | 2 | Specify the number of stop bits. "0": 1 stop bit; "1": 1.5 stop bits when 5-bit character length is selected and 2 bits otherwise. | |
| | LCR_CHAR_BITS[1:0] | 1:0 | Select number of bits in each character. "00": 5 bits; "01": 6 bits; "10": 7 bits; "11": 8 bits. | |
| 08h | REG110210 | 7:0 | Default : 0x00 Access : R/W | |
| (110210h) | / | 7:6 | Reserved. | |
| | MCR_AFCE | 5 | Auto Flow Control Enable; 1: enable. | |
| | MCR_LOOPBACK | 4 | 1: Loopback mode. SOUT -> SIN (pad "STX_PAD_O" will be set to "1"). DTR -> DSR. RTS-> CTS. Out1 -> RI. Out2 -> DCD. | |
| | MCR_OUT2 | 3 | In loopback mode, connect to Data Carrier Detect (DCD) signal input. | |



| FUART Regi | ster (Bank = 1102) | | |
|---------------------|--------------------|-----|--|
| Index (Absolute) | Mnemonic | Bit | Description |
| | MCR_OUT1 | 2 | In loopback mode, connect to Ring Indicator (RI) signal input. |
| | MCR_RTS | 1 | Request To Send (RTS) signal control. "0": RTS is "1"; "1": RTS is "0". |
| | MCR_DTR | 0 | Data Terminal Ready (DTR) signal control. "0": DTR is "1"; "1": DTR is "0". |
| 0Ah | REG110214 | 7:0 | Default : 0x00 Access : R0 |
| (110214h) | LSR_ERROR | 7 | Receiver FIFO Error bit. |
| | LSR_TX_EMPTY | 6 | 1: Transmitter (tx FIFO and shift registers) Empty indicator. Clear after writing data into tx FIFO. |
| | LSR_TXFIFO_EMPTY | 5 | 1: Transmit FIFO is empty. Clear after writing data into tx FIFO. Generate a Transmitter Holding Register Empty interrupt. |
| | LSR_BI | 4 | Break Interrupt bit. |
| | LSR_FE | 3 | 1: Framing Error indicator. Clear when reading. Generate a Receiver Line Status interrupt. |
| -iC | LSR_PE | 2 | 1: Parity Error indicator. Clear when reading. Generate a Receiver Line Status interrupt. |
| | LSR_OE | 1 | 1: RX Overrun Error indicator. Clear when reading. Generate a Receiver Line Status interrupt. |
| | LSR_DR | 0 | 1: Received Data Ready indicator. |
| 0Ch | REG110218 | 7:0 | Default : 0x00 Access : R0 |
| (110218h) | MSR_DCD_COMP | 7 | Complement of "DCD" or equal to "OUT2" in loopback. |
| | MSR_RI_COMP | 6 | Complement of "RI" or equal to "OUT1" in loopback. |
| | MSR_DSR_COMP | 5 | Complement of "DSR" or equal to "DTR" in loopback. |
| | MSR_CTS_COMP | 4 | Complement of "CTS" or equal to "RTS" in loopback. |
| | MSR_DDCD | 3 | Delta Data Carrier Detect (DDCD) indicator. "1": the "DCD" line has changed its state. Clear when reading. |
| | MSR_TERI | 2 | Trailing Edge of Ring Indictor (TERI) detector. The "RI" line has changed its state from low to high. Clear when reading. |



| FUART Regi | FUART Register (Bank = 1102) | | | | |
|---------------------|------------------------------|-----|--|--|--|
| Index (Absolute) | Mnemonic | Bit | Description | | |
| | MSR_DDSR | 1 | Delta Data Set Ready (DDSR) indicator. "1": the "DSR" line has changed its state. Clear when reading. | | |
| | MSR_DCTS | 0 | Delta Clear To Send (DCTS) indicator. "1": the "CTS" line has changed its state. Clear when reading. | | |
| OEh | REG11021C | 7:0 | Default : 0x00 Access : R0 | | |
| (11021Ch) | - | 7:5 | Reserved. | | |
| | USR_RFF | 4 | Rx FIFO Full. | | |
| | USR_RFNE | 3 | Rx FIFO Not Empty. | | |
| | USR_TFE | 2 | Tx FIFO Empty. | | |
| | USR_TFNF | 1 | Tx FIFO Not Full. | | |
| | USR_BUSY | 0 | UART Busy. | | |
| 10h | REG110220 | 7:0 | Default : 0x00 Access : RO | | |
| (110220h) | - | 7:6 | Reserved. | | |
| | TFL[5:0] | 5:0 | Tx FIFO level. | | |
| 12h | REG110224 | 7:0 | Default : 0x00 Access : RO | | |
| (110224h) | | 7:6 | Reserved. | | |
| | RFL[5:0] | 5:0 | Rx FIFO level. | | |

3.2. UARTO Register (Bank = 1108)

| UARTO Regi | UARTO Register (Bank = 1108) | | | | |
|---------------------|------------------------------|-----|--|---|--|
| Index (Absolute) | Mnemonic | Bit | Description | | |
| 00h | REG110800 | 7:0 | Default : 0x00 | Access : R/W | |
| (110800h) | THR_RBR_DLL[7:0] | 7:0 | FIFO results in the write Read: Receiver Buffer. Read receive FIFO; note | ng Register. e that writing data to a full data being lost. that any incoming data are d an overrun error occurs. | |
| 02h | REG110804 | 7:0 | Default : 0x00 | Access : R/W | |



| UARTO Regi | ster (Bank = 1108) | | |
|---------------------|--------------------|-----|--|
| Index (Absolute) | Mnemonic | Bit | Description |
| (110804h) | IER_DLH[7:0] | 7:0 | When "reg_lcr_dl_access" = 0. Interrupt Enable Registers (IER); 1: enabled. Bit [0]: Received Data Available Interrupt and Character Timeout Interrupt. Bit [1]: Transmitter Holding Register Empty Interrupt. Bit [2]: Receiver Line Status Interrupt. Bit [3]: Modem Status interrupt. Bit [3]: Modem Status interrupt. Bit [7]: Programmable THRE Interrupt. When "reg_lcr_dl_access" = 1. Divisor Latch MSB. Baud rate = (serial clock freq.) / (16 * divisor). |
| 04h | REG110808 | 7:0 | Default : 0x00 Access : R/W |
| (110808h) | FCR_IIR[7:0] | 7:0 | Write. FIFO Control Register (FCR). Bit [0]: FIFO enable. Bit [1]: write "1" to clear RX FIFO. Bit [2]: write "1" to clear TX FIFO. Bit [2]: write "1" to clear TX FIFO. Bit [5:4]: Transmit FIFO Empty trigger level. "00": FIFO empty: "01": 2 characters in the FIFO; "10": FIFO 1/4 full; "11": FIFO 1/2 full. Bit [7:6]: Receiver FIFO Interrupt trigger level. "00": 1 character in the FIFO; "01": FIFO 1/4 full; "10": FIFO 1/4 full; "10": FIFO 1/4 full; "10": FIFO 1/2 full. Bit [7:6]: Receiver FIFO Interrupt trigger level. "00": 1 character in the FIFO; "01": FIFO 1/2 full; "11": FIFO 1/2 full; "11": FIFO 2 less than full. 2. Read. Interrupt Identification Registers (IIR). Bit [0]: 1: no interrupt is pending. Bit [3:1]: interrupt identified. "10": Receiver Line Status. "01": Receiver Data Available. "001": Transmitter Holding Register empty. "000": Modem Status. "00": Modem Status. "0" "0" "0" "0" "0" "0" "0" "0" "0" "0" "0" "0" " |
| 06h | REG11080C | 7:0 | Default : 0x03 Access : R/W |
| (11080Ch) | LCR_DL_ACCESS | 7 | Divisor Latch Access; 1: The divisor latches can be accessed. |
| | LCR_BREAK_CTRL | 6 | Break control bit. |



| UARTO Regi | ster (Bank = 1108) | | |
|---------------------|---------------------|-----|---|
| Index (Absolute) | Mnemonic | Bit | Description |
| | - | 5 | Reserved. |
| | LCR_EVEN_PARITY_SEL | 4 | 1: Select even parity. |
| | LCR_PARITY_EN | | 1: Generate parity bit on serial out. |
| | LCR_STOP_BITS | 2 | Specify the number of stop bits. "0": 1 stop bit; "1": 1.5 stop bits when 5-bit character length is selected and 2 bits otherwise. |
| | LCR_CHAR_BITS[1:0] | 1:0 | Select number of bits in each character. "00": 5 bits; "01": 6 bits; "10": 7 bits; "11": 8 bits. |
| 08h | REG110810 | 7:0 | Default : 0x00 Access : R/W |
| (110810h) | - | 7:6 | Reserved. |
| | MCR_AFCE | 5 | Auto Flow Control Enable; 1: enable. |
| Ν | MCR_LOOPBACK | 4 | 1: Loopback mode. SOUT -> SIN (pad "STX_PAD_O" will be set to "1"). DTR -> DSR. RTS-> CTS. Out1 -> RI. Out2 -> DCD. |
| | MCR_OUT2 | 3 | In loopback mode, connect to Data Carrier Detect (DCD) signal input. |
| cil | MCR_OUT1 | 2 | In loopback mode, connect to Ring Indicator (RI) signal input. |
| | MCR_RTS | 1 | Request To Send (RTS) signal control. "0": RTS is "1"; "1": RTS is "0". |
| | MCR_DTR | 0 | Data Terminal Ready (DTR) signal control. "0": DTR is "1"; "1": DTR is "0". |
| 0Ah | REG110814 | 7:0 | Default : 0x00 Access : R0 |
| (110814h) | LSR_ERROR | 7 | Receiver FIFO Error bit. |
| | LSR_TX_EMPTY | 6 | 1: Transmitter (tx FIFO and shift registers) Empty indicator. Clear after writing data into tx FIFO. |
| | LSR_TXFIFO_EMPTY | 5 | 1: Transmit FIFO is empty. Clear after writing data into tx FIFO. Generate a Transmitter Holding Register Empty interrupt. |
| | LSR_BI | 4 | Break Interrupt bit. |
| | LSR_FE | 3 | 1: Framing Error indicator. |



| UARTO Regi | ster (Bank = 1108) | , | r | |
|---------------------|--------------------|---|--|--|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | | | Clear when reading. | |
| | | | Generate a Receiver Line Status interrupt. | |
| | LSR_PE | 2 | 1: Parity Error indicator. Clear when reading. Generate a Receiver Line Status interrupt. | |
| | LSR_OE | 1 | 1: RX Overrun Error indicator. Clear when reading. Generate a Receiver Line Status interrupt. | |
| | LSR_DR | 0 | 1: Received Data Ready indicator. | |
| OCh | REG110818 | 7:0 | Default : 0x00 Access : R0 | |
| (110818h) | MSR_DCD_COMP | 7 | Complement of "DCD" or equal to "OUT2" in loopback. | |
| | MSR_RI_COMP | 6 | Complement of "RI" or equal to "OUT1" in loopback. | |
| | MSR_DSR_COMP | 5 | Complement of "DSR" or equal to "DTR" in loopback. | |
| | MSR_CTS_COMP | 4 | Complement of "CTS" or equal to "RTS" in loopback. | |
| - | MSR_DDCD | 3 | Delta Data Carrier Detect (DDCD) indicator. "1": the "DCD" line has changed its state. Clear when reading. | |
| | MSR_TERI | 2 | Trailing Edge of Ring Indicator (TERI) detector. The "RI" line has changed its state from low to high. Clear when reading. | |
| | MSR_DDSR | | Delta Data Set Ready (DDSR) indicator. "1": the "DSR" line has changed its state. Clear when reading. | |
| | MSR_DCTS | 0 | Delta Clear To Send (DCTS) indicator. "1": the "CTS" line has changed its state. Clear when reading. | |
| OEh | REG11081C | 7:0 | Default : 0x00 Access : RO | |
| (11081Ch) | / | 7:5 | Reserved. | |
| | USR_RFF | 4 | Rx FIFO Full. | |
| | USR_RFNE | 3 | Rx FIFO Not Empty. | |
| | USR_TFE | 2 | Tx FIFO Empty. | |
| | USR_TFNF | 1 | Tx FIFO Not Full. | |
| | USR_BUSY | 0 | UART Busy. | |
| 10h | REG110820 | 7:0 | Default : 0x00 Access : RO | |
| (110820h) | - | 7:6 | Reserved. | |
| | TFL[5:0] | 5:0 | Tx FIFO level. | |



| UARTO Regi | UARTO Register (Bank = 1108) | | | | | |
|---------------------|------------------------------|-----|----------------|-------------|--|--|
| Index (Absolute) | Mnemonic | Bit | Description | | | |
| 12h | REG110824 | 7:0 | Default : 0x00 | Access : RO | | |
| (110824h) | - | 7:6 | Reserved. | | | |
| | RFL[5:0] | 5:0 | Rx FIFO level. | | | |

3.3. UART1 Register (Bank = 1109)

| UART1 Regi | ster (Bank = 1109) | | | |
|---------------------|--------------------|-----|--|--|
| Index (Absolute) | Mnemonic | Bit | Description | |
| 00h | REG110900 | 7:0 | Default : 0x00 | Access : R/W |
| (110900h) | THR_RBR_DLL[7:0] | 7:0 | FIFO results in the write Read: Receiver Buffer. Read receive FIFO; note lost when FIFO is full and | ng Register. e that writing data to a full data being lost. that any incoming data are d an overrun error occurs. |
| | 2 | | 2. When "reg_lcr_dl_access Divisor Latch LSB. | " = 1. |
| 02h | REG110904 | 7:0 | Default : 0x00 | Access : R/W |
| (110904h) | IER_DLH[7:0] | 7:0 | When "reg_lcr_dl_access Interrupt Enable Register Bit [0]: Received Data Av Character Timeout Interr Bit [1]: Transmitter Holdi Bit [2]: Receiver Line Sta Bit [3]: Modem Status in Bit [7]: Programmable Th 2. When "reg_lcr_dl_access Divisor Latch MSB. Baud rate = (serial clock | rs (IER); 1: enabled. vailable Interrupt and upt. ing Register Empty Interrupt. tus Interrupt. terrupt. HRE Interrupt. " = 1. |
| 04h | REG110908 | 7:0 | Default : 0x00 | Access : R/W |
| (110908h) | FCR_IIR[7:0] | 7:0 | Write. FIFO Control Register (FOBit [0]: FIFO enable. Bit [1]: write "1" to clear Bit [2]: write "1" to clear Bit [5:4]: Transmit FIFO "00": FIFO empty; | RX FIFO. TX FIFO. |



| UART1 Regi | ster (Bank = 1109) | r | r | | |
|---------------------|---------------------|-------------|--|--|--|
| Index (Absolute) | Mnemonic | Bit | Description | | |
| | | 9 9 8 | "01": 2 characters in the FIFO; "10": FIFO 1/4 full; "11": FIFO 1/2 full. Bit [7:6]: Receiver FIFO Interrupt trigger level. "00": 1 character in the FIFO; "01": FIFO 1/4 full; "10": FIFO 1/2 full; "11": FIFO 2 less than full. 2. Read. Interrupt Identification Registers (IIR). Bit [0]: 1: no interrupt is pending. Bit [3:1]: interrupt identified. "11": Receiver Line Status. "010": Receiver Data Available. "00": Modem Status. | | |
| 06h | REG11090C | 7:0 | Default : 0x03 Access : R/W | | |
| (110000) | LCR_DL_ACCESS | 7 | Divisor Latch Access. 1: The divisor latches can be accessed. | | |
| | LCR_BREAK_CTRL | 6 | Break control bit. | | |
| | | 5 | Reserved. | | |
| 5 | LCR_EVEN_PARITY_SEL | 4 | 1: Select even parity. | | |
| | LCR_PARITY_EN | 3 | 1: Generate parity bit on serial out. | | |
| | LCR_STOP_BITS | 2 | Specify the number of stop bits. "0": 1 stop bit; "1": 1.5 stop bits when 5-bit character length is selected and 2 bits otherwise. | | |
| | LCR_CHAR_BITS[1:0] | 1:0 | Select number of bits in each character. "00": 5 bits; "01": 6 bits; "10": 7 bits; "11": 8 bits. | | |
| 08h | REG110910 | 7:0 | Default : 0x00 Access : R/W | | |
| (110910h) | - | 7:6 | Reserved. | | |
| | MCR_AFCE | 5 | Auto Flow Control Enable; 1: enable. | | |
| | MCR_LOOPBACK | 4 | 1: Loopback mode. SOUT -> SIN (pad "STX_PAD_O" will be set to "1"). DTR -> DSR. RTS-> CTS. Out1 -> RI. | | |



| UART1 Regi | ister (Bank = 1109) | | | | |
|--|---------------------|--|--|--|--|
| Index (Absolute) | Mnemonic | Bit | Description | | |
| | | | Out2 -> DCD. | | |
| | MCR_OUT2 | 3 | In loopback mode, connect to Data Carrier Detect (DCD) signal input. | | |
| | MCR_OUT1 | 2 | In loopback mode, connect to Ring Indicator (RI) signal input. | | |
| | MCR_RTS | 1 | Request To Send (RTS) signal control. "0": RTS is "1"; "1": RTS is "0". | | |
| MCR_DTR 0 Data Terminal Ready (DTR) signal co "0": DTR is "1"; "1": DTR is "0". | | Data Terminal Ready (DTR) signal control. "0": DTR is "1"; "1": DTR is "0". | | | |
| 0Ah | REG110914 | 7:0 | Default : 0x00 Access : R0 | | |
| (110914h) | LSR_ERROR | 7 | Receiver FIFO Error bit. | | |
| | LSR_TX_EMPTY | 6 | 1: Transmitter (tx FIFO and shift registers) Empty indicator. Clear after writing data into tx FIFO. | | |
| | LSR_TXFIFO_EMPTY | 5 | 1: Transmit FIFO is empty. | | |
| | S | | Clear after writing data into tx FIFO. Generate a Transmitter Holding Register Empty interrupt. | | |
| | LSR_BI | 4 | Break Interrupt bit. | | |
| ~ C | LSR_FE | 3 | 1: Framing Error indicator. Clear when reading. Generate a Receiver Line Status interrupt. | | |
| | LSR_PE | 2 | 1: Parity Error indicator. Clear when reading. Generate a Receiver Line Status interrupt. | | |
| | LSR_OE | 1 | 1: RX Overrun Error indicator. Clear when reading. Generate a Receiver Line Status interrupt. | | |
| | LSR_DR | 0 | 1: Received Data Ready indicator. | | |
| 0Ch | REG110918 | 7:0 | Default : 0x00 Access : R0 | | |
| (110918h) | MSR_DCD_COMP | 7 | Complement of "DCD" or equal to "OUT2" in loopback. | | |
| | MSR_RI_COMP | 6 | Complement of "RI" or equal to "OUT1" in loopback. | | |
| | MSR_DSR_COMP | 5 | Complement of "DSR" or equal to "DTR" in loopback. | | |
| | MSR_CTS_COMP | 4 | Complement of "CTS" or equal to "RTS" in loopback. | | |
| | MSR_DDCD | 3 | Delta Data Carrier Detect (DDCD) indicator. "1": the "DCD" line has changed its state. Clear when reading. | | |



| UART1 Regi | UART1 Register (Bank = 1109) | | | | | |
|---------------------|------------------------------|-----|--|--|--|--|
| Index (Absolute) | Mnemonic | Bit | Description | | | |
| | MSR_TERI | 2 | Trailing Edge of Ring Indicator (TERI) detector. The "RI" line has changed its state from low to high. Clear when reading. | | | |
| | MSR_DDSR | 1 | Delta Data Set Ready (DDSR) indicator. "1": the "DSR" line has changed its state. Clear when reading. | | | |
| | MSR_DCTS | 0 | Delta Clear To Send (DCTS) indicator. "1": the "CTS" line has changed its state. Clear when reading. | | | |
| OEh | REG11091C | 7:0 | Default : 0x00 Access : RO | | | |
| (11091Ch) | | 7:5 | Reserved. | | | |
| | USR_RFF | 4 | Rx FIFO Full. | | | |
| | USR_RFNE | 3 | Rx FIFO Not Empty | | | |
| | USR_TFE | 2 | Tx FIFO Empty. | | | |
| | USR_TFNF | 1 | Tx FIFO Not Full. | | | |
| | USR_BU <mark>S</mark> Y | 0 | UART Busy. | | | |
| 10h | REG110920 | 7:0 | Default : 0x00 Access : RO | | | |
| (110920h) | | 7:6 | Reserved. | | | |
| | TFL[5:0] | 5:0 | Tx FIFO level. | | | |
| 12h | REG110924 | 7:0 | Default : 0x00 Access : RO | | | |
| (110924h) | - / | 7:6 | Reserved. | | | |
| | RFL[5:0] | 5:0 | Rx FIFO level. | | | |

3.4. UART2 Register (Bank = 110A)

| UART2 Register (Bank = 110A) | | | | |
|------------------------------|------------------|-----|--|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| 00h | REG110A00 | 7:0 | Default : 0x00 | Access : R/W |
| (110A00h) | THR_RBR_DLL[7:0] | 7:0 | FIFO results in the write Read: Receiver Buffer. Read receive FIFO; note | ng Register. e that writing data to a full data being lost. that any incoming data are d an overrun error occurs. |



| UART2 Regi | ster (Bank = 110A) | | | |
|--|--------------------|---|--|--|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | | | Divisor Latch LSB. | |
| 02h | REG110A04 | 7:0 | Default : 0x00 | Access : R/W |
| (110A04h) IER_DLH[7:0] 7:0 1. When "reg_lcr_dl_access" = 0. Interrupt Enable Registers (IER); 1: Bit [0]: Received Data Available Intercharacter Timeout Interrupt. Bit [1]: Transmitter Holding Register Bit [2]: Receiver Line Status Interrupt Bit [3]: Modem Status interrupt. Bit [7]: Programmable THRE Interrupt. Bit [7]: Programmable THRE Interrupt. Divisor Latch MSB. Baud rate = (serial clock freq.) / (16) | | rs (IER); 1: enabled. vailable Interrupt and upt. ng Register Empty Interrupt. tus Interrupt. rerrupt. IRE Interrupt. " = 1. | | |
| 04h | REG110A08 | 7:0 | Default : 0x00 | Access : R/W |
| (110A08h) | FCR_IIR[7:0] | 7:0 | Write. FIFO Control Register (FG Bit [0]: FIFO enable. Bit [1]: write "1" to clear Bit [2]: write "1" to clear Bit [5:4]: Transmit FIFO "00": FIFO empty: "01": 2 characters in the "10": FIFO 1/4 full; "11": FIFO 1/2 full. Bit [7:6]: Receiver FIFO I "00": 1 character in the F "01": FIFO 1/4 full; "10": FIFO 1/4 full; "10": FIFO 1/2 full. Read. Interrupt Identification R Bit [0]: 1: no interrupt is Bit [3:1]: interrupt identifi "110": Receiver Line Stat "010": Receiver Data Ava "001": Transmitter Holdir "000": Modem Status. | RX FIFO. TX FIFO. Empty trigger level. FIFO; Interrupt trigger level. TIFO; II. egisters (IIR). pending. fied. us. |
| 06h | REG110A0C | 7:0 | Default : 0x03 | Access : R/W |



| UART2 Regi | ister (Bank = 110A) | | | | |
|---------------------|---------------------|-----|---|--|--|
| Index (Absolute) | Mnemonic | Bit | Description | | |
| (110A0Ch) | LCR_DL_ACCESS | 7 | Divisor Latch Access. 1: The divisor latches can be accessed. | | |
| | LCR_BREAK_CTRL | 6 | Break control bit. | | |
| | - | 5 | Reserved. | | |
| | LCR_EVEN_PARITY_SEL | 4 | 1: Select even parity. | | |
| | LCR_PARITY_EN | 3 | 1: Generate parity bit on serial out. | | |
| | LCR_STOP_BITS | 2 | Specify the number of stop bits. "0": 1 stop bit; "1": 1.5 stop bits when 5-bit character length is selected and 2 bits otherwise. | | |
| | LCR_CHAR_BITS[1:0] | 1:0 | Select number of bits in each character. "00": 5 bits; "01": 6 bits; "10": 7 bits; "11": 8 bits. | | |
| 08h | REG110A10 | 7:0 | Default : 0x00 Access : R/W | | |
| (110A10h) | - | 7:6 | Reserved. | | |
| | MCR_AFCE | 5 | Auto Flow Control Enable; 1: enable. | | |
| | MCR_LOOPBACK | 4 | 1: Loopback mode. SOUT -> SIN (pad "STX_PAD_O" will be set to "1"). DTR -> DSR. RTS-> CTS. Out1 -> RI. Out2 -> DCD. | | |
| | MCR_OUT2 | 3 | In loopback mode, connect to Data Carrier Detect (DCD) signal input. | | |
| | MCR_OUT1 | 2 | In loopback mode, connect to Ring Indicator (RI) signal input. | | |
| | MCR_RTS | | Request To Send (RTS) signal control. "0": RTS is "1"; "1": RTS is "0". | | |
| | MCR_DTR | 0 | Data Terminal Ready (DTR) signal control. "0": DTR is "1"; "1": DTR is "0". | | |
| 0Ah | REG110A14 | 7:0 | Default : 0x00 Access : RO | | |
| (110A14h) | LSR_ERROR | 7 | Receiver FIFO Error bit. | | |
| | LSR_TX_EMPTY | 6 | 1: Transmitter (tx FIFO and shift registers) Empty indicator. Clear after writing data into tx FIFO. | | |
| | LSR_TXFIFO_EMPTY | 5 | 1: Transmit FIFO is empty. Clear after writing data into tx FIFO. | | |



| UART2 Regi | ister (Bank = 110A) | | | | |
|--|---------------------|-----|---|-------------|--|
| Index (Absolute) | Mnemonic | Bit | Description | | |
| | | | Generate a Transmitter Holding Register Empty interrupt. | | |
| | LSR_BI | 4 | Break Interrupt bit. | | |
| LSR_FE | | 3 | 1: Framing Error indicator. Clear when reading. Generate a Receiver Line Status interrupt. | | |
| | LSR_PE | 2 | 1: Parity Error indicator. Clear when reading. Generate a Receiver Line Status interrupt. | | |
| | LSR_OE | 1 | 1: RX Overrun Error indicator Clear when reading. Generate a Receiver Line Sta | | |
| | LSR_DR | 0 | 1: Received Data Ready indic | cator. | |
| 0Ch | REG110A18 | 7:0 | Default : 0x00 | Access : RO | |
| (110A18h) | MSR_DCD_COMP | 7 | Complement of "DCD" or equal to "OUT2" in loopback. | | |
| | MSR_RI_COMP | 6 | Complement of "RI" or equal to "OUT1" in loopback. | | |
| | MSR_DSR_COMP | 5 | Complement of "DSR" or equal to "DTR" in loopback. | | |
| | MSR_CTS_COMP | 4 | Complement of "CTS" or equal to "RTS" in loopback. | | |
| MSR_DDCD 3 Delta Data Carrier Detect (DDCD "1": the "DCD" line has changed Clear when reading. | | - | | | |
| 5 | MSR_TERI | 2 | Trailing Edge of Ring Indicate The "RI" line has changed its Clear when reading. | , , | |
| | MSR_DDSR | 1 | Delta Data Set Ready (DDSR) indicator. "1": the "DSR" line has changed its state. Clear when reading. | | |
| | MSR_DCTS | 0 | Delta Clear To Send (DCTS) indicator. "1": the "CTS" line has changed its state. Clear when reading. | | |
| OEh | REG110A1C | 7:0 | Default : 0x00 | Access : RO | |
| (110A1Ch) | - | 7:5 | Reserved. | | |
| | USR_RFF | 4 | Rx FIFO Full. | | |
| | USR_RFNE | 3 | Rx FIFO Not Empty. | | |
| | USR_TFE | 2 | Tx FIFO Empty. | | |
| | USR_TFNF | 1 | Tx FIFO Not Full. | | |
| | USR_BUSY | 0 | UART Busy. | | |



| UART2 Register (Bank = 110A) | | | | |
|------------------------------|-----------|-----|----------------|-------------|
| Index (Absolute) | Mnemonic | Bit | Description | |
| 10h | REG110A20 | 7:0 | Default : 0x00 | Access : RO |
| (110A20h) | - | 7:6 | Reserved. | |
| | TFL[5:0] | 5:0 | Tx FIFO level. | |
| 12h | REG110A24 | 7:0 | Default : 0x00 | Access : RO |
| (110A24h) | - | 7:6 | Reserved. | |
| | RFL[5:0] | 5:0 | Rx FIFO level. | |