SSD202D
UART/FUART Module Description

1. MODULE DESCRIPTION

1.1. Overview

The UART module provides UART protocol to different devices. This ASIC provides two UART engines and one fast UART engine.

1.2. Function Description

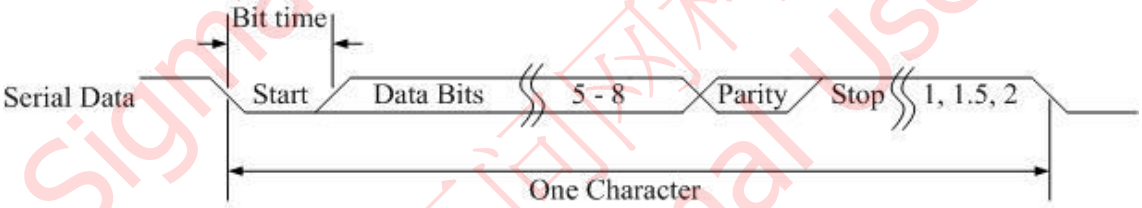
The UART module has the following features:

- Supports 32-byte FIFO for read and write respectively
- Supports interrupt
- Supports auto flow control

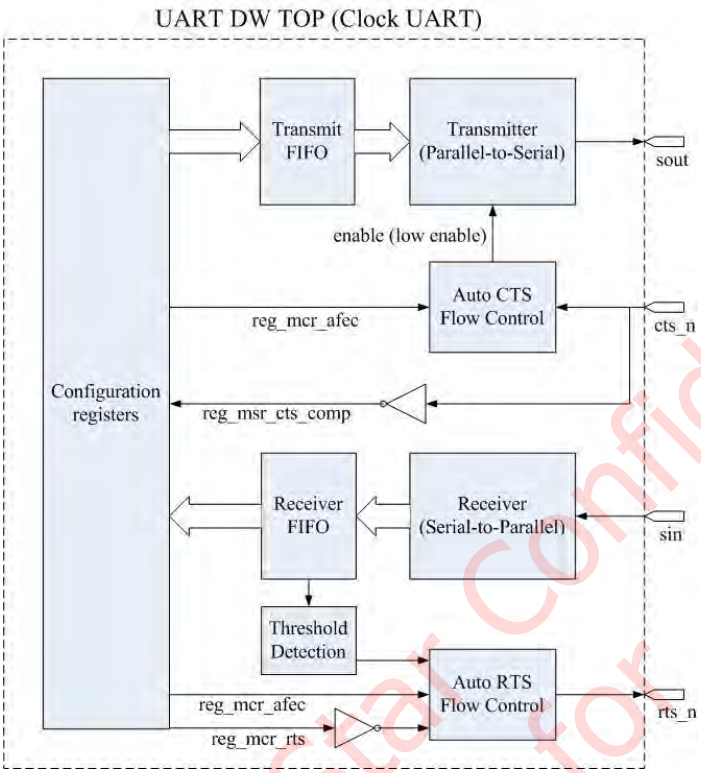
1.3. Operating Mode

UART Protocol:

A character is composed of start bit (1 bit), data bit (5-8 bits), parity bit (1 or none) and stop bit (1, 1.5 or 2 bits).



Block Diagram:



1.3.1 UART Initialization

- Set interrupt control register
- Set FIFO control register
- Set line control register
- Set auto flow control (optional)
- Set baud rate

1.3.2 UART Transmit or TX

- Write data to specified register to transmit characters
- Check line status register
- Get interrupt

1.3.3 UART Receive or RX

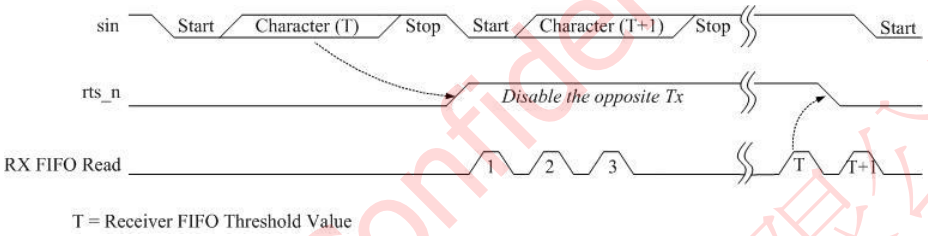
- Read data from specified register to get received characters
- Check line status register
- Get interrupt

Note:

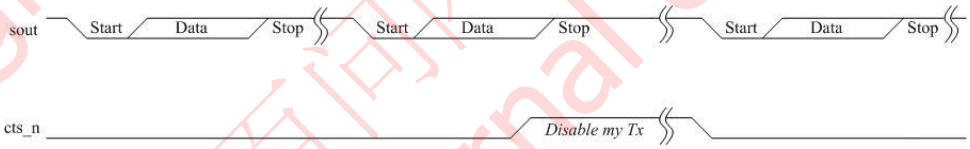
Auto Flow Control:

The "UART DW" can be configured to realize 16750-compatible Auto RTS/CTS serial data flow control mode.

- Auto RTS:
  1. Enable registers
  2. Timing:
     a. The “rts_n” output is pulled high (inactive) when the RX FIFO level reaches the threshold; this will keep the opposite UART from sending data.
     b. The “rts_n” output is pulled low (active) when the RX FIFO becomes empty by reading RBR; this will signal the opposite UART to continue sending data.
     c. Character (T+1) may be received because “rts_n” (high) was not detected before it entered the opposite UART’s transmitter.



- Auto CTS:
  1. Enable registers
  2. Timing:
     a. The “cts_n” input is pulled high (inactive); this will keep the transmitter from sending data.
     b. The “cts_n” input is pulled low (active); this will enable the transmission to resume.
     c. If “cts_n” input is not pulled high before the middle of the last “stop” bit, another character may be transmitted before the transmitter is disabled.
     d. While the transmitter is disabled, the TX FIFO can still be written and even become overflowed.

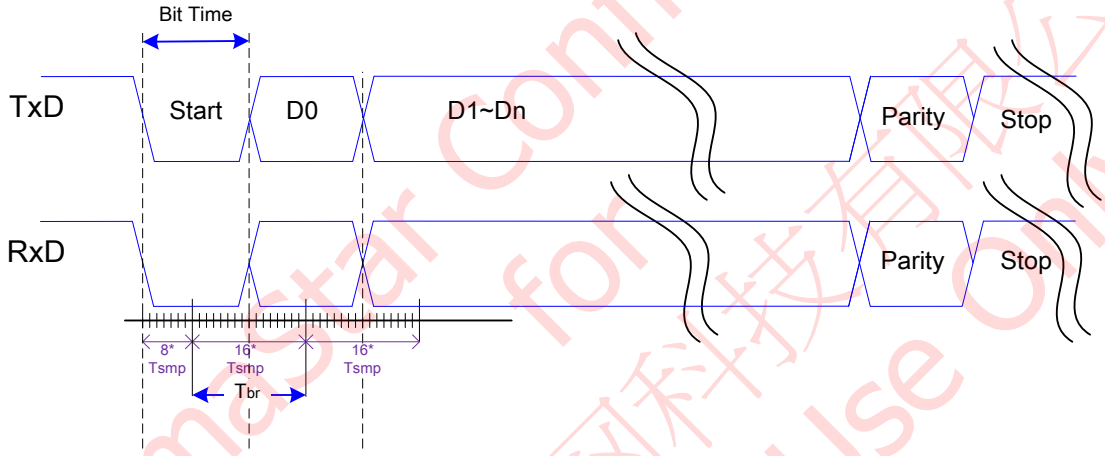


2. AC/DC SPECIFICATION

2.1. AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Baud Rate Period	Tbr		115200		bps
UART Sampling Period	Tsmp		1/16		Tbr

2.2. TxD/RxD Timing



3. REGISTER DESCRIPTION

3.1. FUART Register (Bank = 1102)

FUART Register (Bank = 1102)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (110200h)	REG110200	7:0	Default : 0x00	Access : R/W
	THR_RBR_DLL[7:0]	7:0	1. When "reg_lcr_dl_access" = 0. Write: Transmitter Holding Register. Write transmit FIFO; note that writing data to a full FIFO results in the write data being lost. Read: Receiver Buffer. Read receive FIFO; note that any incoming data are lost when FIFO is full and an overrun error occurs. 2. When "reg_lcr_dl_access" = 1. Divisor Latch LSB.	
02h (110204h)	REG110204	7:0	Default : 0x00	Access : R/W
	IER_DLH[7:0]	7:0	1. When "reg_lcr_dl_access" = 0. Interrupt Enable Registers (IER); 1: enabled. Bit [0]: Received Data Available Interrupt and Character Timeout Interrupt. Bit [1]: Transmitter Holding Register Empty Interrupt. Bit [2]: Receiver Line Status Interrupt. Bit [3]: Modem Status interrupt. Bit [7]: Programmable THRE Interrupt. 2. When "reg_lcr_dl_access" = 1. Divisor Latch MSB. Baud rate = (serial clock freq.) / (16 * divisor).	
04h (110208h)	REG110208	7:0	Default : 0x00	Access : R/W
	FCR_IIR[7:0]	7:0	1. Write. FIFO Control Register (FCR). Bit [0]: FIFO enable. Bit [1]: write "1" to clear RX FIFO. Bit [2]: write "1" to clear TX FIFO. Bit [5:4]: Transmit FIFO Empty trigger level. "00": FIFO empty; "01": 2 characters in the FIFO; "10": FIFO 1/4 full; "11": FIFO 1/2 full.	

FUART Register (Bank = 1102)			
Index (Absolute)	Mnemonic	Bit	Description
			Bit [7:6]: Receiver FIFO Interrupt trigger level. "00": 1 character in the FIFO; "01": FIFO 1/4 full; "10": FIFO 1/2 full; "11": FIFO 2 less than full. 2. Read. Interrupt Identification Registers (IIR). Bit [0]: 1: no interrupt is pending. Bit [3:1]: interrupt identified. "110": character timeout. "011": Receiver Line Status. "010": Receiver Data Available. "001": Transmitter Holding Register empty. "000": Modem Status.
06h (11020Ch)	REG11020C	7:0	Default : 0x03 Access : R/W
	LCR_DL_ACCESS	7	Divisor Latch Access. 1: The divisor latches can be accessed.
	LCR_BREAK_CTRL	6	Break control bit.
	-	5	Reserved.
	LCR_EVEN_PARITY_SEL	4	1: Select even parity.
	LCR_PARITY_EN	3	1: Generate parity bit on serial out.
	LCR_STOP_BITS	2	Specify the number of stop bits. "0": 1 stop bit; "1": 1.5 stop bits when 5-bit character length is selected and 2 bits otherwise.
	LCR_CHAR_BITS[1:0]	1:0	Select number of bits in each character. "00": 5 bits; "01": 6 bits; "10": 7 bits; "11": 8 bits.
08h (110210h)	REG110210	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	MCR_AFCE	5	Auto Flow Control Enable; 1: enable.
	MCR_LOOPBACK	4	1: Loopback mode. SOUT -> SIN (pad "STX_PAD_O" will be set to "1"). DTR -> DSR. RTS-> CTS. Out1 -> RI. Out2 -> DCD.
	MCR_OUT2	3	In loopback mode, connect to Data Carrier Detect (DCD) signal input.

FUART Register (Bank = 1102)				
Index (Absolute)	Mnemonic	Bit	Description	
	MCR_OUT1	2	In loopback mode, connect to Ring Indicator (RI) signal input.	
	MCR_RTS	1	Request To Send (RTS) signal control. "0": RTS is "1"; "1": RTS is "0".	
	MCR_DTR	0	Data Terminal Ready (DTR) signal control. "0": DTR is "1"; "1": DTR is "0".	
0Ah (110214h)	REG110214	7:0	Default : 0x00	Access : RO
	LSR_ERROR	7	Receiver FIFO Error bit.	
	LSR_TX_EMPTY	6	1: Transmitter (tx FIFO and shift registers) Empty indicator. Clear after writing data into tx FIFO.	
	LSR_TXFIFO_EMPTY	5	1: Transmit FIFO is empty. Clear after writing data into tx FIFO. Generate a Transmitter Holding Register Empty interrupt.	
	LSR_BI	4	Break Interrupt bit.	
	LSR_FE	3	1: Framing Error indicator. Clear when reading. Generate a Receiver Line Status interrupt.	
	LSR_PE	2	1: Parity Error indicator. Clear when reading. Generate a Receiver Line Status interrupt.	
	LSR_OE	1	1: RX Overrun Error indicator. Clear when reading. Generate a Receiver Line Status interrupt.	
	LSR_DR	0	1: Received Data Ready indicator.	
0Ch (110218h)	REG110218	7:0	Default : 0x00	Access : RO
	MSR_DCD_COMP	7	Complement of "DCD" or equal to "OUT2" in loopback.	
	MSR_RI_COMP	6	Complement of "RI" or equal to "OUT1" in loopback.	
	MSR_DSR_COMP	5	Complement of "DSR" or equal to "DTR" in loopback.	
	MSR_CTS_COMP	4	Complement of "CTS" or equal to "RTS" in loopback.	
	MSR_DDCD	3	Delta Data Carrier Detect (DDCD) indicator. "1": the "DCD" line has changed its state. Clear when reading.	
	MSR_TERI	2	Trailing Edge of Ring Indictor (TERI) detector. The "RI" line has changed its state from low to high. Clear when reading.	

FUART Register (Bank = 1102)				
Index (Absolute)	Mnemonic	Bit	Description	
	MSR_DDSR	1	Delta Data Set Ready (DDSR) indicator. "1": the "DSR" line has changed its state. Clear when reading.	
	MSR_DCTS	0	Delta Clear To Send (DCTS) indicator. "1": the "CTS" line has changed its state. Clear when reading.	
0Eh (11021Ch)	REG11021C	7:0	Default : 0x00	Access : RO
	-	7:5	Reserved.	
	USR_RFF	4	Rx FIFO Full.	
	USR_RFNE	3	Rx FIFO Not Empty.	
	USR_TFE	2	Tx FIFO Empty.	
	USR_TFNF	1	Tx FIFO Not Full.	
	USR_BUSY	0	UART Busy.	
10h (110220h)	REG110220	7:0	Default : 0x00	Access : RO
	-	7:6	Reserved.	
	TFL[5:0]	5:0	Tx FIFO level.	
12h (110224h)	REG110224	7:0	Default : 0x00	Access : RO
	-	7:6	Reserved.	
	RFL[5:0]	5:0	Rx FIFO level.	

3.2. UART0 Register (Bank = 1108)

UART0 Register (Bank = 1108)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (110800h)	REG110800	7:0	Default : 0x00	Access : R/W
	THR_RBR_DLL[7:0]	7:0	1. When "reg_lcr_dl_access" = 0. Write: Transmitter Holding Register. Write transmit FIFO; note that writing data to a full FIFO results in the write data being lost. Read: Receiver Buffer. Read receive FIFO; note that any incoming data are lost when FIFO is full and an overrun error occurs. 2. When "reg_lcr_dl_access" = 1. Divisor Latch LSB.	
02h	REG110804	7:0	Default : 0x00	Access : R/W

UART0 Register (Bank = 1108)			
Index (Absolute)	Mnemonic	Bit	Description
(110804h)	IER_DLH[7:0]	7:0	1. When "reg_lcr_dl_access" = 0. Interrupt Enable Registers (IER); 1: enabled. Bit [0]: Received Data Available Interrupt and Character Timeout Interrupt. Bit [1]: Transmitter Holding Register Empty Interrupt. Bit [2]: Receiver Line Status Interrupt. Bit [3]: Modem Status interrupt. Bit [7]: Programmable THRE Interrupt. 2. When "reg_lcr_dl_access" = 1. Divisor Latch MSB. Baud rate = (serial clock freq.) / (16 * divisor).
04h (110808h)	REG110808	7:0	Default : 0x00 / Access : R/W
	FCR_IIR[7:0]	7:0	1. Write. FIFO Control Register (FCR). Bit [0]: FIFO enable. Bit [1]: write "1" to clear RX FIFO. Bit [2]: write "1" to clear TX FIFO. Bit [5:4]: Transmit FIFO Empty trigger level. "00": FIFO empty; "01": 2 characters in the FIFO; "10": FIFO 1/4 full; "11": FIFO 1/2 full. Bit [7:6]: Receiver FIFO Interrupt trigger level. "00": 1 character in the FIFO; "01": FIFO 1/4 full; "10": FIFO 1/2 full; "11": FIFO 2 less than full. 2. Read. Interrupt Identification Registers (IIR). Bit [0]: 1: no interrupt is pending. Bit [3:1]: interrupt identified. "110": character timeout. "011": Receiver Line Status. "010": Receiver Data Available. "001": Transmitter Holding Register empty. "000": Modem Status.
06h (11080Ch)	REG11080C	7:0	Default : 0x03 / Access : R/W
	LCR_DL_ACCESS	7	Divisor Latch Access; 1: The divisor latches can be accessed.
	LCR_BREAK_CTRL	6	Break control bit.

UART0 Register (Bank = 1108)				
Index (Absolute)	Mnemonic	Bit	Description	
	-	5	Reserved.	
	LCR_EVEN_PARITY_SEL	4	1: Select even parity.	
	LCR_PARITY_EN	3	1: Generate parity bit on serial out.	
	LCR_STOP_BITS	2	Specify the number of stop bits. "0": 1 stop bit; "1": 1.5 stop bits when 5-bit character length is selected and 2 bits otherwise.	
	LCR_CHAR_BITS[1:0]	1:0	Select number of bits in each character. "00": 5 bits; "01": 6 bits; "10": 7 bits; "11": 8 bits.	
08h (110810h)	REG110810	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	MCR_AFCE	5	Auto Flow Control Enable; 1: enable.	
	MCR_LOOPBACK	4	1: Loopback mode. SOUT -> SIN (pad "STX_PAD_O" will be set to "1"). DTR -> DSR. RTS-> CTS. Out1 -> RI. Out2 -> DCD.	
	MCR_OUT2	3	In loopback mode, connect to Data Carrier Detect (DCD) signal input.	
	MCR_OUT1	2	In loopback mode, connect to Ring Indicator (RI) signal input.	
	MCR_RTS	1	Request To Send (RTS) signal control. "0": RTS is "1"; "1": RTS is "0".	
	MCR_DTR	0	Data Terminal Ready (DTR) signal control. "0": DTR is "1"; "1": DTR is "0".	
0Ah (110814h)	REG110814	7:0	Default : 0x00	Access : RO
	LSR_ERROR	7	Receiver FIFO Error bit.	
	LSR_TX_EMPTY	6	1: Transmitter (tx FIFO and shift registers) Empty indicator. Clear after writing data into tx FIFO.	
	LSR_TXFIFO_EMPTY	5	1: Transmit FIFO is empty. Clear after writing data into tx FIFO. Generate a Transmitter Holding Register Empty interrupt.	
	LSR_BI	4	Break Interrupt bit.	
	LSR_FE	3	1: Framing Error indicator.	

UART0 Register (Bank = 1108)				
Index (Absolute)	Mnemonic	Bit	Description	
			Clear when reading. Generate a Receiver Line Status interrupt.	
	LSR_PE	2	1: Parity Error indicator. Clear when reading. Generate a Receiver Line Status interrupt.	
	LSR_OE	1	1: RX Overrun Error indicator. Clear when reading. Generate a Receiver Line Status interrupt.	
	LSR_DR	0	1: Received Data Ready indicator.	
0Ch (110818h)	REG110818	7:0	Default : 0x00	Access : RO
	MSR_DCD_COMP	7	Complement of "DCD" or equal to "OUT2" in loopback.	
	MSR_RI_COMP	6	Complement of "RI" or equal to "OUT1" in loopback.	
	MSR_DSR_COMP	5	Complement of "DSR" or equal to "DTR" in loopback.	
	MSR_CTS_COMP	4	Complement of "CTS" or equal to "RTS" in loopback.	
	MSR_DDCD	3	Delta Data Carrier Detect (DDCD) indicator. "1": the "DCD" line has changed its state. Clear when reading.	
	MSR_TERI	2	Trailing Edge of Ring Indicator (TERI) detector. The "RI" line has changed its state from low to high. Clear when reading.	
	MSR_DDSR	1	Delta Data Set Ready (DDSR) indicator. "1": the "DSR" line has changed its state. Clear when reading.	
	MSR_DCTS	0	Delta Clear To Send (DCTS) indicator. "1": the "CTS" line has changed its state. Clear when reading.	
0Eh (11081Ch)	REG11081C	7:0	Default : 0x00	Access : RO
	-	7:5	Reserved.	
	USR_RFF	4	Rx FIFO Full.	
	USR_RFNE	3	Rx FIFO Not Empty.	
	USR_TFE	2	Tx FIFO Empty.	
	USR_TFNF	1	Tx FIFO Not Full.	
	USR_BUSY	0	UART Busy.	
10h (110820h)	REG110820	7:0	Default : 0x00	Access : RO
	-	7:6	Reserved.	
	TFL[5:0]	5:0	Tx FIFO level.	

UART0 Register (Bank = 1108)				
Index (Absolute)	Mnemonic	Bit	Description	
12h (110824h)	REG110824	7:0	Default : 0x00	Access : RO
	-	7:6	Reserved.	
	RFL[5:0]	5:0	Rx FIFO level.	

3.3. UART1 Register (Bank = 1109)

UART1 Register (Bank = 1109)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (110900h)	REG110900	7:0	Default : 0x00	Access : R/W
	THR_RBR_DLL[7:0]	7:0	1. When "reg_lcr_dl_access" = 0. Write: Transmitter Holding Register. Write transmit FIFO; note that writing data to a full FIFO results in the write data being lost. Read: Receiver Buffer. Read receive FIFO; note that any incoming data are lost when FIFO is full and an overrun error occurs. 2. When "reg_lcr_dl_access" = 1. Divisor Latch LSB.	
02h (110904h)	REG110904	7:0	Default : 0x00	Access : R/W
	IER_DLH[7:0]	7:0	1. When "reg_lcr_dl_access" = 0. Interrupt Enable Registers (IER); 1: enabled. Bit [0]: Received Data Available Interrupt and Character Timeout Interrupt. Bit [1]: Transmitter Holding Register Empty Interrupt. Bit [2]: Receiver Line Status Interrupt. Bit [3]: Modem Status interrupt. Bit [7]: Programmable THRE Interrupt. 2. When "reg_lcr_dl_access" = 1. Divisor Latch MSB. Baud rate = (serial clock freq.) / (16 * divisor).	
04h (110908h)	REG110908	7:0	Default : 0x00	Access : R/W
	FCR_IIR[7:0]	7:0	1. Write. FIFO Control Register (FCR). Bit [0]: FIFO enable. Bit [1]: write "1" to clear RX FIFO. Bit [2]: write "1" to clear TX FIFO. Bit [5:4]: Transmit FIFO Empty trigger level. "00": FIFO empty;	

UART1 Register (Bank = 1109)			
Index (Absolute)	Mnemonic	Bit	Description
			"01": 2 characters in the FIFO; "10": FIFO 1/4 full; "11": FIFO 1/2 full. Bit [7:6]: Receiver FIFO Interrupt trigger level. "00": 1 character in the FIFO; "01": FIFO 1/4 full; "10": FIFO 1/2 full; "11": FIFO 2 less than full. 2. Read. Interrupt Identification Registers (IIR). Bit [0]: 1: no interrupt is pending. Bit [3:1]: interrupt identified. "110": character timeout. "011": Receiver Line Status. "010": Receiver Data Available. "001": Transmitter Holding Register empty. "000": Modem Status.
06h (11090Ch)	REG11090C	7:0	Default : 0x03 Access : R/W
	LCR_DL_ACCESS	7	Divisor Latch Access. 1: The divisor latches can be accessed.
	LCR_BREAK_CTRL	6	Break control bit.
	-	5	Reserved.
	LCR_EVEN_PARITY_SEL	4	1: Select even parity.
	LCR_PARITY_EN	3	1: Generate parity bit on serial out.
	LCR_STOP_BITS	2	Specify the number of stop bits. "0": 1 stop bit; "1": 1.5 stop bits when 5-bit character length is selected and 2 bits otherwise.
	LCR_CHAR_BITS[1:0]	1:0	Select number of bits in each character. "00": 5 bits; "01": 6 bits; "10": 7 bits; "11": 8 bits.
08h (110910h)	REG110910	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	MCR_AFCE	5	Auto Flow Control Enable; 1: enable.
	MCR_LOOPBACK	4	1: Loopback mode. SOUT -> SIN (pad "STX_PAD_O" will be set to "1"). DTR -> DSR. RTS-> CTS. Out1 -> RI.

UART1 Register (Bank = 1109)				
Index (Absolute)	Mnemonic	Bit	Description	
			Out2 -> DCD.	
	MCR_OUT2	3	In loopback mode, connect to Data Carrier Detect (DCD) signal input.	
	MCR_OUT1	2	In loopback mode, connect to Ring Indicator (RI) signal input.	
	MCR_RTS	1	Request To Send (RTS) signal control. "0": RTS is "1"; "1": RTS is "0".	
	MCR_DTR	0	Data Terminal Ready (DTR) signal control. "0": DTR is "1"; "1": DTR is "0".	
0Ah (110914h)	REG110914	7:0	Default : 0x00	Access : RO
	LSR_ERROR	7	Receiver FIFO Error bit.	
	LSR_TX_EMPTY	6	1: Transmitter (tx FIFO and shift registers) Empty indicator. Clear after writing data into tx FIFO.	
	LSR_TXFIFO_EMPTY	5	1: Transmit FIFO is empty. Clear after writing data into tx FIFO. Generate a Transmitter Holding Register Empty interrupt.	
	LSR_BI	4	Break Interrupt bit.	
	LSR_FE	3	1: Framing Error indicator. Clear when reading. Generate a Receiver Line Status interrupt.	
	LSR_PE	2	1: Parity Error indicator. Clear when reading. Generate a Receiver Line Status interrupt.	
	LSR_OE	1	1: RX Overrun Error indicator. Clear when reading. Generate a Receiver Line Status interrupt.	
	LSR_DR	0	1: Received Data Ready indicator.	
0Ch (110918h)	REG110918	7:0	Default : 0x00	Access : RO
	MSR_DCD_COMP	7	Complement of "DCD" or equal to "OUT2" in loopback.	
	MSR_RI_COMP	6	Complement of "RI" or equal to "OUT1" in loopback.	
	MSR_DSR_COMP	5	Complement of "DSR" or equal to "DTR" in loopback.	
	MSR_CTS_COMP	4	Complement of "CTS" or equal to "RTS" in loopback.	
	MSR_DDCD	3	Delta Data Carrier Detect (DDCD) indicator. "1": the "DCD" line has changed its state. Clear when reading.	

UART1 Register (Bank = 1109)				
Index (Absolute)	Mnemonic	Bit	Description	
	MSR_TERI	2	Trailing Edge of Ring Indicator (TERI) detector. The "RI" line has changed its state from low to high. Clear when reading.	
	MSR_DDSR	1	Delta Data Set Ready (DDSR) indicator. "1": the "DSR" line has changed its state. Clear when reading.	
	MSR_DCTS	0	Delta Clear To Send (DCTS) indicator. "1": the "CTS" line has changed its state. Clear when reading.	
0Eh (11091Ch)	REG11091C	7:0	Default : 0x00	Access : RO
	-	7:5	Reserved.	
	USR_RFF	4	Rx FIFO Full.	
	USR_RFNE	3	Rx FIFO Not Empty.	
	USR_TFE	2	Tx FIFO Empty.	
	USR_TFNF	1	Tx FIFO Not Full.	
	USR_BUSY	0	UART Busy.	
10h (110920h)	REG110920	7:0	Default : 0x00	Access : RO
	-	7:6	Reserved.	
	TFL[5:0]	5:0	Tx FIFO level.	
12h (110924h)	REG110924	7:0	Default : 0x00	Access : RO
	-	7:6	Reserved.	
	RFL[5:0]	5:0	Rx FIFO level.	

3.4. UART2 Register (Bank = 110A)

UART2 Register (Bank = 110A)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (110A00h)	REG110A00	7:0	Default : 0x00	Access : R/W
	THR_RBR_DLL[7:0]	7:0	1. When "reg_lcr_dl_access" = 0. Write: Transmitter Holding Register. Write transmit FIFO; note that writing data to a full FIFO results in the write data being lost. Read: Receiver Buffer. Read receive FIFO; note that any incoming data are lost when FIFO is full and an overrun error occurs. 2. When "reg_lcr_dl_access" = 1.	

UART2 Register (Bank = 110A)				
Index (Absolute)	Mnemonic	Bit	Description	
			Divisor Latch LSB.	
02h (110A04h)	REG110A04	7:0	Default : 0x00	Access : R/W
	IER_DLH[7:0]	7:0	1. When "reg_lcr_dl_access" = 0. Interrupt Enable Registers (IER); 1: enabled. Bit [0]: Received Data Available Interrupt and Character Timeout Interrupt. Bit [1]: Transmitter Holding Register Empty Interrupt. Bit [2]: Receiver Line Status Interrupt. Bit [3]: Modem Status interrupt. Bit [7]: Programmable THRE Interrupt. 2. When "reg_lcr_dl_access" = 1. Divisor Latch MSB. Baud rate = (serial clock freq.) / (16 * divisor).	
04h (110A08h)	REG110A08	7:0	Default : 0x00	Access : R/W
	FCR_IIR[7:0]	7:0	1. Write. FIFO Control Register (FCR). Bit [0]: FIFO enable. Bit [1]: write "1" to clear RX FIFO. Bit [2]: write "1" to clear TX FIFO. Bit [5:4]: Transmit FIFO Empty trigger level. "00": FIFO empty; "01": 2 characters in the FIFO; "10": FIFO 1/4 full; "11": FIFO 1/2 full. Bit [7:6]: Receiver FIFO Interrupt trigger level. "00": 1 character in the FIFO; "01": FIFO 1/4 full; "10": FIFO 1/2 full; "11": FIFO 2 less than full. 2. Read. Interrupt Identification Registers (IIR). Bit [0]: 1: no interrupt is pending. Bit [3:1]: interrupt identified. "110": character timeout. "011": Receiver Line Status. "010": Receiver Data Available. "001": Transmitter Holding Register empty. "000": Modem Status.	
06h	REG110A0C	7:0	Default : 0x03	Access : R/W

UART2 Register (Bank = 110A)			
Index (Absolute)	Mnemonic	Bit	Description
(110A0Ch)	LCR_DL_ACCESS	7	Divisor Latch Access. 1: The divisor latches can be accessed.
	LCR_BREAK_CTRL	6	Break control bit.
	-	5	Reserved.
	LCR_EVEN_PARITY_SEL	4	1: Select even parity.
	LCR_PARITY_EN	3	1: Generate parity bit on serial out.
	LCR_STOP_BITS	2	Specify the number of stop bits. "0": 1 stop bit; "1": 1.5 stop bits when 5-bit character length is selected and 2 bits otherwise.
	LCR_CHAR_BITS[1:0]	1:0	Select number of bits in each character. "00": 5 bits; "01": 6 bits; "10": 7 bits; "11": 8 bits.
08h (110A10h)	REG110A10	7:0	Default : 0x00 | Access : R/W
	-	7:6	Reserved.
	MCR_AFCE	5	Auto Flow Control Enable; 1: enable.
	MCR_LOOPBACK	4	1: Loopback mode. SOUT -> SIN (pad "STX_PAD_O" will be set to "1"). DTR -> DSR. RTS-> CTS. Out1 -> RI. Out2 -> DCD.
	MCR_OUT2	3	In loopback mode, connect to Data Carrier Detect (DCD) signal input.
	MCR_OUT1	2	In loopback mode, connect to Ring Indicator (RI) signal input.
	MCR_RTS	1	Request To Send (RTS) signal control. "0": RTS is "1"; "1": RTS is "0".
	MCR_DTR	0	Data Terminal Ready (DTR) signal control. "0": DTR is "1"; "1": DTR is "0".
0Ah (110A14h)	REG110A14	7:0	Default : 0x00 | Access : RO
	LSR_ERROR	7	Receiver FIFO Error bit.
	LSR_TX_EMPTY	6	1: Transmitter (tx FIFO and shift registers) Empty indicator. Clear after writing data into tx FIFO.
	LSR_TXFIFO_EMPTY	5	1: Transmit FIFO is empty. Clear after writing data into tx FIFO.

UART2 Register (Bank = 110A)				
Index (Absolute)	Mnemonic	Bit	Description	
			Generate a Transmitter Holding Register Empty interrupt.	
	LSR_BI	4	Break Interrupt bit.	
	LSR_FE	3	1: Framing Error indicator. Clear when reading. Generate a Receiver Line Status interrupt.	
	LSR_PE	2	1: Parity Error indicator. Clear when reading. Generate a Receiver Line Status interrupt.	
	LSR_OE	1	1: RX Overrun Error indicator. Clear when reading. Generate a Receiver Line Status interrupt.	
	LSR_DR	0	1: Received Data Ready indicator.	
0Ch (110A18h)	REG110A18	7:0	Default : 0x00	Access : RO
	MSR_DCD_COMP	7	Complement of "DCD" or equal to "OUT2" in loopback.	
	MSR_RI_COMP	6	Complement of "RI" or equal to "OUT1" in loopback.	
	MSR_DSR_COMP	5	Complement of "DSR" or equal to "DTR" in loopback.	
	MSR_CTS_COMP	4	Complement of "CTS" or equal to "RTS" in loopback.	
	MSR_DDCD	3	Delta Data Carrier Detect (DDCD) indicator. "1": the "DCD" line has changed its state. Clear when reading.	
	MSR_TERI	2	Trailing Edge of Ring Indicator (TERI) detector. The "RI" line has changed its state from low to high. Clear when reading.	
	MSR_DDSR	1	Delta Data Set Ready (DDSR) indicator. "1": the "DSR" line has changed its state. Clear when reading.	
	MSR_DCTS	0	Delta Clear To Send (DCTS) indicator. "1": the "CTS" line has changed its state. Clear when reading.	
0Eh (110A1Ch)	REG110A1C	7:0	Default : 0x00	Access : RO
	-	7:5	Reserved.	
	USR_RFF	4	Rx FIFO Full.	
	USR_RFNE	3	Rx FIFO Not Empty.	
	USR_TFE	2	Tx FIFO Empty.	
	USR_TFNF	1	Tx FIFO Not Full.	
	USR_BUSY	0	UART Busy.	

UART2 Register (Bank = 110A)				
Index (Absolute)	Mnemonic	Bit	Description	
10h (110A20h)	REG110A20	7:0	Default : 0x00	Access : RO
	-	7:6	Reserved.	
	TFL[5:0]	5:0	Tx FIFO level.	
12h (110A24h)	REG110A24	7:0	Default : 0x00	Access : RO
	-	7:6	Reserved.	
	RFL[5:0]	5:0	Rx FIFO level.	