SSD202D
RTC Module Description

1. REGISTER DESCRIPTION

1.1. RTCPWC Register (Bank = 34)

RTCPWC Register (Bank = 34)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (3400h)	REG3400	7:0	Default : 0x00	Access : R/W
	DIG2RTC_SW0_RD	7	1: Get RTC SW0 value from "rtc2dig_rddata[31:0]" (gating by iso_en).	
	DIG2RTC_SW1_WR	6	1: Use "dig2rtc_wrdata[31:0]" to set SW1 base(gating by iso_en).	
	DIG2RTC_SW0_WR	5	1: Use "dig2rtc_wrdata[31:0]" to set SW0 base(gating by iso_en).	
	DIG2RTC_ALARM_WR	4	1: Use "dig2rtc_wrdata[31:0]" to set Alarm counter(gating by iso_en).	
	DIG2RTC_CNT_RST_WR	3	1: Reset RTC Counter value to 0(gating by iso_en).	
	DIG2RTC_BASE_RD	2	1: Get RTC base value from "rtc2dig_rddata[31:0]"(gating by iso_en).	
	DIG2RTC_BASE_WR	1	1: Use "dig2rtc_wrdata[31:0]" to set RTC Base(gating by iso_en).	
	-	0	Reserved.	
00h (3401h)	REG3401	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	DIG2RTC_SW1_RD	0	1: Get RTC SW1 value from "rtc2dig_rddata[31:0]" (gating by iso_en).	
01h (3402h)	REG3402	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	DIG2RTC_INT_CLR	3	1: Clear rtc2dig_int (Alarm interrupt)(gating by iso_en).	
	DIG2RTC_ALARM_EN	2	1: Set Alarm enable to 1, which also can read from "rtc2dig_alarm_en"(gating by iso_en).	
	DIG2RTC_ALARM_RD	1	1: Get RTC Alarm value from "rtc2dig_rddata[31:0]"(gating by iso_en).	
	DIG2RTC_CNT_RD	0	1: Get RTC counter value from "rtc2dig_rddata[31:0]" (gating by iso_en).	
03h	REG3406	7:0	Default : 0x00	Access : R/W

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(3406h)	-	7:3	Reserved.	
	DIG2RTC_ISO_CTRL[2:0]	2:0	Bit 2-0 ISO_EN control signal. Input "000 -> 001 > 011 -> 111 -> 101 -> 001 -> 000" to enable ISO_EN for 1ms.	
04h (3408h)	REG3408	7:0	Default : 0x00	Access : R/W
	DIG2RTC_WRDATA[7:0]	7:0	DIG2RTC_WRDATA. According to current value of "dig2rtc_base_wr" & "dig2rtc_alarm_wr" & "dig2rtc_sw0_wr" & "dig2rtc_sw1_wr", to write data into corresponding counter.	
04h (3409h)	REG3409	7:0	Default : 0x00	Access : R/W
	DIG2RTC_WRDATA[15:8]	7:0	See description of '3408h'.	
05h (340Ah)	REG340A	7:0	Default : 0x00	Access : R/W
	DIG2RTC_WRDATA[23:16]	7:0	See description of '3408h'.	
05h (340Bh)	REG340B	7:0	Default : 0x00	Access : R/W
	DIG2RTC_WRDATA[31:24]	7:0	See description of '3408h'.	
06h (340Ch)	REG340C	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	DIG2RTC_SET	0	1: Set "rtc2dig_valid" to 1, which is direct bypass to Analog part.	
07h (340Eh)	REG340E	7:0	Default : 0x00	Access : RO
	-	7:1	Reserved.	
	RTC2DIG_VALID	0	Get value from "dig2rtc_set", bypass from Analog Part.	
08h (3410h)	REG3410	7:0	Default : 0x00	Access : RO
	-	7:4	Reserved.	
	RTC2DIG_ISO_CTRL_ACK	3	ISO control ack signal. SW can read this bit to indicate the ISO control is correct or not. "000(S0) -> 001 (S1) > 011 (S2) -> 111 (S3) -> 101 (S4) -> 001 (S5) -> 000 (S0)" Ack signal will be 1, when under S1/S3/S5 state.	
	-	2	Reserved.	
	RTC2DIG_INT	1	Alarm interrupt , which can be clear by "dig2rtc_int_clr"	
	RTC2DIG_ALARM_EN	0	Get value from "dig2rtc_alarm_en", read for debug usage. 1: Means the Alarm function is enable.	
09h	REG3412	7:0	Default : 0x00	Access : RO

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(3412h)	RTC2DIG_RDDATA[7:0]	7:0	RTC read data. According the current value of "dig2rtc_base_rd", "dig2rtc_alarm_rd", "dig2rtc_sw0_rd", "dig2rtc_sw1_rd" to decide the read data type.	
09h (3413h)	REG3413	7:0	Default : 0x00	Access : RO
	RTC2DIG_RDDATA[15:8]	7:0	See description of '3412h'.	
0Ah (3414h)	REG3414	7:0	Default : 0x00	Access : RO
	RTC2DIG_RDDATA[23:16]	7:0	See description of '3412h'.	
0Ah (3415h)	REG3415	7:0	Default : 0x00	Access : RO
	RTC2DIG_RDDATA[31:24]	7:0	See description of '3412h'.	
0Bh (3416h)	REG3416	7:0	Default : 0x00	Access : RO
	-	7:1	Reserved.	
	RTC2DIG_CNT_UPDATING	0	RTC counter updating period (1Hz clock edge) indication. 0: RTC counter value is ready to read. 1: RTC counter is under updating (1ms width enclosing 1Hz clock edge), when SW get 1 in this bit, please read the counter value again to get valid data.	
0Ch (3418h)	REG3418	7:0	Default : 0x00	Access : RO
	RTC2DIG_RDDATA_CNT[7:0]	7:0	RTC read data for time counter(latch rtc2dig_rddata). According the current value of "dig2rtc_cnt_rd" to decide the read data type.	
0Ch (3419h)	REG3419	7:0	Default : 0x00	Access : RO
	RTC2DIG_RDDATA_CNT[15:8]	7:0	See description of '3418h'.	
0Dh (341Ah)	REG341A	7:0	Default : 0x00	Access : RO
	RTC2DIG_RDDATA_CNT[23:16]	7:0	See description of '3418h'.	
0Dh (341Bh)	REG341B	7:0	Default : 0x00	Access : RO
	RTC2DIG_RDDATA_CNT[31:24]	7:0	See description of '3418h'.	
0Eh (341Ch)	REG341C	7:0	Default : 0x00	Access : WO
	-	7:1	Reserved.	
	DIG2RTC_CNT_RD_TRIG	0	Rtc2dig_rddata_cnt and cnt_updating trigger signal. 0: RTC counter and cnt_updating would't update. 1: Generate a pluse to latch data before read ,including signal rtc2dig_rddata[31:0] and rtc2dig_cnt updating.	

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0Fh (341Eh)	REG341E	7:0	Default : 0x05	Access : R/W
	-	7:3	Reserved.	
	DIG2PWC_EMGCY_OFF_EN	2	Set 1 to Enable PWC Power-Key 1 emergency shut-down (gating by iso_en).	
	DIG2PWC_ALARM_ON_EN	1	Set 1 to Enable RTC alarm to power-on system via PWC function (gating by iso_en).	
	DIG2PWC_PWR_EN_CTRL	0	Software control of PWC Power Enable; Set to 0 and initiate an isolation control cycle to start Power-Off sequence(gating by iso_en).	
10h (3420h)	REG3420	7:0	Default : 0xFF	Access : R/W
	DIG2PWC_OPT_7_0[7:0]	7:0	Software control of PWC Powerkey 0-7(gating by iso_en). 1: Enable function. 0: Disable function.	
10h (3421h)	REG3421	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	SEL_32K_CLEAN_JITTER	2	Register for poc_atop/rtc_xtal.	
	SEL_32K_COMP_DRV	1	Register for poc_atop/rtc_xtal.	
	PMTEST_INT	0	Replace PAD_PMTESET, when PAD_PMTEST not bound.	
11h (3422h)	REG3422	7:0	Default : 0x00	Access : RO
	PWC2DIG_FLAG_7_0[7:0]	7:0	PWC power-on flag. User can check the status to know which key/event trigger power-on. [2:0]. 3'b000: power-key 1 power-on. 3'b001: power-key 2 power-on. 3'b010: power-key 3 power-on. 3'b011: power-key 4 power-on. 3'b100: power-key 5 power-on. 3'b101: Alarm power-on.	
12h (3424h)	REG3424	7:0	Default : 0x00	Access : RO
	-	7:6	Reserved.	
	PWC2DIG_PWRKEY_5	5	Power key-5 status.	
	PWC2DIG_PWRKEY_4	4	Power key-4 status.	
	PWC2DIG_PWRKEY_3	3	Power key-3 status.	
	PWC2DIG_PWRKEY_2	2	Power key-2 status.	
	PWC2DIG_PWRKEY_1	1	Power key-1 status.	

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	PWC2DIG_PWR_GOOD	0	Power good status.	
13h (3426h)	REG3426	7:0	Default : 0x00	Access : RO
	-	7:3	Reserved.	
	PWC2DIG_RESET_N	2	PWR reset status.	
	32K_OK	1	Flag XTAL 32k OK.	
	PWC2DIG_PWR_EN_STATE	0	Power enable status.	
14h (3428h)	REG3428	7:0	Default : 0x00	Access : RO
	POC_TESTBUS[7:0]	7:0	[0]: Pwr_on_st. [1]: Pwr_off_trig. [2]: Pwr_on_fail. [3]: Pwr_on_done. [4]: Pwc_off_cs. [5]: Pwc_on_seq_cs. [6]: Pwc_on_cs. [7]: Pwr_en. [8]: Gr_rst. [9]: Hw_rst_reboot. [10]: Pwrkey1_deb. [11]: Pwrkey2_deb. [12]: 1'b0. [13]: Pwrkey4_deb. [14]: Pwrkey5_deb. [15]: 1'b0.	
14h (3429h)	REG3429	7:0	Default : 0x00	Access : RO
	POC_TESTBUS[15:8]	7:0	See description of '3428h'.	
15h (342Ah)	REG342A	7:0	Default : 0x00	Access : RO
	-	7:6	Reserved.	
	RTC_TESTBUS[5:0]	5:0	[0]: ISO_EN. [1]: Clk_1hz_p. [2]: Clk_1hz. [3]: Clk_8hz. [4]: Clk_128hz. [5]: Clk_1khz.	