SSD202D
CHIPTOP Module Description

1. REGISTER DESCRIPTION

1.1. CHIPTOP Register (Bank = 101E)

CHIPTOP Register (Bank = 101E)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (101E00h)	REG101E00	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	CKG_ALLDFT	0	MIU clock selects DFT clock. MPLL_SYN clock selects DFT clock. MIU_REC clock selects DFT clock. GE clock selects DFT clock.	
01h (101E03h)	REG101E03	7:0	Default : 0x02	Access : R/W
	-	7:6	Reserved.	
	SETL	5	Digital pads set low.	
	SETH	4	Digital pads set high.	
	-	3:2	Reserved.	
	FT_MODE	1	FT mode. 1: Enable FT mode. 0: Disable FT mode.	
	-	0	Reserved.	
03h (101E06h)	REG101E06	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	UART0_MODE[2:0]	6:4	UART0 Mode.	
	-	3	Reserved.	
	FUART_MODE[2:0]	2:0	FUART Mode.	
03h (101E07h)	REG101E07	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	UART2_MODE[2:0]	6:4	UART2 Mode.	
	-	3	Reserved.	
	UART1_MODE[2:0]	2:0	UART1 Mode.	
07h (101E0Eh)	REG101E0E	7:0	Default : 0x00	Access : R/W
	PWM2_MODE[1:0]	7:6	PWM2 Mode.	
	PWM1_MODE[2:0]	5: 3	PWM1 Mode.	

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	PWM0_MODE[2:0]	2:0	PWM0 Mode.	
07h (101E0Fh)	REG101E0F	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	PWM3_MODE[2:0]	3:1	PWM3 Mode.	
	PWM2_MODE[2]	0	See description of '101E0Eh'.	
08h (101E11h)	REG101E11	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SDIO_MODE[1:0]	1:0	SDIO Mode.	
09h (101E12h)	REG101E12	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	I2C1_MODE[2:0]	6:4	I2C1 Mode.	
	-	3	Reserved.	
	I2C0_MODE[2:0]	2:0	I2C0 Mode.	
0Ah (101E14h)	REG101E14	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	PM_SPICZ2_MODE[1:0]	5:4	PM SPI CZ2 Mode.	
	-	3:1	Reserved.	
	IDAC_MODE	0	IDAC Mode.	
0Ch (101E18h)	REG101E18	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	SPI0_MODE[2:0]	2:0	SPI0 Mode.	
0Dh (101E1Ah)	REG101E1A	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	BT1120_MODE[1:0]	1:0	BT1120 Mode.	
0Dh (101E1Bh)	REG101E1B	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	TX_MIPI_MODE[1:0]	5:4	MIPI TX mode.	
	TTL_MODE[3:0]	3:0	TTL Mode.	
0Eh (101E1Ch)	REG101E1C	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	ETH0_MODE	0	ETH0 Mode.	
0Eh (101E1Dh)	REG101E1D	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	

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	ETH1_MODE[3:0]	3:0	ETH1 Mode.	
0Fh (101E1Eh)	REG101E1E	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	EJ_MODE[1:0]	1:0	EJ Mode.	
0Fh (101E1Fh)	REG101E1F	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	I2S_MODE[1:0]	5:4	I2S Mode.	
	-	3	Reserved.	
	DMIC_MODE[2:0]	2:0	DMIC Mode.	
12h (101E24h)	REG101E24	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	TEST_OUT_MODE[1:0]	5:4	Select TEST_OUT mode. 2'd0: TEST_OUT functions are not enabled. 2'd1: TEST_OUT[23:0] use FUART/SR/SPI0 pads. 2'd2: TEST_OUT[23:0] use I2C0/SD/USB/SAR/PM/ETH pads. 2'd3: TEST_OUT[15:0] use SR pads.	
	-	3:2	Reserved.	
	TEST_IN_MODE[1:0]	1:0	Select TEST IN mode. 2'd0: TEST_IN functions are not enabled. 2'd1: TEST_IN[23:0] use FUART/SR/SPI0 pads. 2'd2: TEST_IN[23:0] use I2C0/SD/USB/SAR/PM/ETH pads. 2'd3: TEST_IN[14:0] use SAR/ETH/FUART/SPI0/SD/USB pads.	
1Ch (101E39h)	REG101E39	7:0	Default : 0x00	Access : R/W
	BIST_MODE_EXT	7	BIST mode enable (disabled by default).	
	BIST_START_EXT	6	BIST mode start.	
	-	5	Reserved.	
	FORCE_ALLSRAM_ON	4	Force all of the whole chip SRAM to power-on.	
	-	3:0	Reserved.	
1Dh (101E3Ah)	REG101E3A	7:0	Default : 0x00	Access : RO
	BIST_DONE[7:0]	7:0	Indicate SRAM done. [0]: Dig_gp. [1]: Pm_gp. [2]: Sc_gp.	

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			[3]: Dec_gp. [4]~[14]: N/A. [15]: All.	
1Dh (101E3Bh)	REG101E3B	7:0	Default : 0x00	Access : RO
	BIST_DONE[15:8]	7:0	See description of '101E3Ah'.	
1Eh (101E3Ch)	REG101E3C	7:0	Default : 0x00	Access : RO
	BIST_FAIL[7:0]	7:0	Indicate SRAM fail. [0]: Dig_gp. [1]: Pm_gp. [2]: Sc_gp. [3]: Dec_gp. [4]~[14]: N/A. [15]: All.	
1Eh (101E3Dh)	REG101E3D	7:0	Default : 0x00	Access : RO
	BIST_FAIL[15:8]	7:0	See description of '101E3Ch'.	
20h (101E40h)	REG101E40	7:0	Default : 0xFF	Access : R/W
	CHIPTOP_DUMMY_0[7:0]	7:0	Dummy registers for CHIPTOP.	
20h (101E41h)	REG101E41	7:0	Default : 0xFF	Access : R/W
	CHIPTOP_DUMMY_0[15:8]	7:0	See description of '101E40h'.	
21h (101E42h)	REG101E42	7:0	Default : 0x00	Access : R/W
	CHIPTOP_DUMMY_1[7:0]	7:0	Dummy registers for CHIPTOP. [0]: Clk_MIU_xd2MIU ICG control. 0: Disable. 1: Enable.	
21h (101E43h)	REG101E43	7:0	Default : 0x00	Access : R/W
	CHIPTOP_DUMMY_1[15:8]	7:0	See description of '101E42h'.	
22h (101E44h)	REG101E44	7:0	Default : 0xFF	Access : R/W
	CHIPTOP_DUMMY_2[7:0]	7:0	Dummy registers for CHIPTOP.	
22h (101E45h)	REG101E45	7:0	Default : 0xFF	Access : R/W
	CHIPTOP_DUMMY_2[15:8]	7:0	See description of '101E44h'.	
23h (101E46h)	REG101E46	7:0	Default : 0x00	Access : R/W
	CHIPTOP_DUMMY_3[7:0]	7:0	Dummy registers for CHIPTOP.	
23h (101E47h)	REG101E47	7:0	Default : 0x00	Access : R/W
	CHIPTOP_DUMMY_3[15:8]	7:0	See description of '101E46h'.	
30h	REG101E60	7:0	Default : 0x00	Access : R/W

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Index (Absolute)	Mnemonic	Bit	Description	
(101E60h)	GPIO_DRV[7:0]	7:0	GPIO pad control.	
30h (101E61h)	REG101E61	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	GPIO_DRV[14: 8]	6:0	See description of '101E60h'.	
31h (101E62h)	REG101E62	7:0	Default : 0xFF	Access : R/W
	GPIO_PE[7:0]	7:0	GPIO pad control.	
31h (101E63h)	REG101E63	7:0	Default : 0x7F	Access : R/W
	-	7	Reserved.	
	GPIO_PE[14: 8]	6:0	See description of '101E62h'.	
32h (101E64h)	REG101E64	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	SD_DRV[6:0]	6:0	SD pad control.	
32h (101E65h)	REG101E65	7:0	Default : 0x7F	Access : R/W
	-	7	Reserved.	
	SD_PE[6:0]	6:0	SD pad control.	
35h (101E6Ah)	REG101E6A	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	UART0_DRV[1:0]	5:4	UART0 pad control.	
	FUART_DRV[3:0]	3:0	FUART pad control.	
35h (101E6Bh)	REG101E6B	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	UART1_DRV[1:0]	1:0	UART1 pad control.	
36h (101E6Ch)	REG101E6C	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	HDMITX_DRV[1:0]	1:0	HDMI pad control.	
38h (101E70h)	REG101E70	7:0	Default : 0xFF	Access : R/W
	TTL_IE[7:0]	7:0	TTL pad control.	
38h (101E71h)	REG101E71	7:0	Default : 0xFF	Access : R/W
	TTL_IE[15:8]	7:0	See description of '101E70h'.	
39h (101E72h)	REG101E72	7:0	Default : 0xFF	Access : R/W
	TTL_IE[23:16]	7:0	See description of '101E70h'.	
39h (101E73h)	REG101E73	7:0	Default : 0x0F	Access : R/W
	-	7:4	Reserved.	

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Index (Absolute)	Mnemonic	Bit	Description	
	TTL_IE[27:24]	3:0	See description of '101E70h'.	
3Ah (101E74h)	REG101E74	7:0	Default : 0xFF	Access : R/W
	TTL_PE[7:0]	7:0	TTL pad control.	
3Ah (101E75h)	REG101E75	7:0	Default : 0xFF	Access : R/W
	TTL_PE[15:8]	7:0	See description of '101E74h'.	
3Bh (101E76h)	REG101E76	7:0	Default : 0xFF	Access : R/W
	TTL_PE[23:16]	7:0	See description of '101E74h'.	
3Bh (101E77h)	REG101E77	7:0	Default : 0x0F	Access : R/W
	-	7:4	Reserved.	
	TTL_PE[27:24]	3:0	See description of '101E74h'.	
3Ch (101E78h)	REG101E78	7:0	Default : 0xFF	Access : R/W
	TTL_PS[7:0]	7:0	TTL pad control.	
3Ch (101E79h)	REG101E79	7:0	Default : 0xFF	Access : R/W
	TTL_PS[15:8]	7:0	See description of '101E78h'.	
3Dh (101E7Ah)	REG101E7A	7:0	Default : 0xFF	Access : R/W
	TTL_PS[23:16]	7:0	See description of '101E78h'.	
3Dh (101E7Bh)	REG101E7B	7:0	Default : 0x0F	Access : R/W
	-	7:4	Reserved.	
	TTL_PS[27:24]	3:0	See description of '101E78h'.	
3Eh (101E7Ch)	REG101E7C	7:0	Default : 0x00	Access : R/W
	TTL_DRV[7:0]	7:0	TTL pad control.	
3Eh (101E7Dh)	REG101E7D	7:0	Default : 0x00	Access : R/W
	TTL_DRV[15:8]	7:0	See description of '101E7Ch'.	
3Fh (101E7Eh)	REG101E7E	7:0	Default : 0x00	Access : R/W
	TTL_DRV[23:16]	7:0	See description of '101E7Ch'.	
3Fh (101E7Fh)	REG101E7F	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	TTL_DRV[27:24]	3:0	See description of '101E7Ch'.	
40h (101E80h)	REG101E80	7:0	Default : 0x03	Access : R/W
	-	7:2	Reserved.	
	MCU_BRIDGE_EN_MODE[1:0]	1:0	Clock MCU gating control. 00: Use MCU_bridge_en (HW saving mode 0). 01: Use MCU_bridge_en_d (HW saving mode 1, preferred).	

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Index (Absolute)	Mnemonic	Bit	Description	
			10: SW saving power mode. 11: Always enable (default).	
44h (101E88h)	REG101E88	7:0	Default : 0xFF	Access : R/W
	RIU_WCLK_MASK[7:0]	7:0	RIU write clock mask. [0]: Sc_gp. [1]: Vhe_gp. [2]: HeMCU_gp. [3]: Mipi_gp. [4]: Mcu_if_gp. [5]: Others.	
44h (101E89h)	REG101E89	7:0	Default : 0xFF	Access : R/W
	RIU_WCLK_MASK[15:8]	7:0	See description of '101E88h'.	
45h (101E8Ah)	REG101E8A	7:0	Default : 0xFF	Access : R/W
	RESERVED3[7:0]	7:0	Reserved.	
45h (101E8Bh)	REG101E8B	7:0	Default : 0xFF	Access : R/W
	RESERVED3[15:8]	7:0	See description of '101E8Ah'.	
46h (101E8Ch)	REG101E8C	7:0	Default : 0xFF	Access : R/W
	RESERVED4[7:0]	7:0	Reserved.	
46h (101E8Dh)	REG101E8D	7:0	Default : 0xFF	Access : R/W
	RESERVED4[15:8]	7:0	See description of '101E8Ch'.	
47h (101E8Eh)	REG101E8E	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	BOND_OV_EN[4:0]	4:0	Bonding overwrite enable.	
47h (101E8Fh)	REG101E8F	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	BOND_OV[4:0]	4:0	Bonding overwrite value.	
48h (101E90h)	REG101E90	7:0	Default : 0x00	Access : RO
	-	7:5	Reserved.	
	BOND_IN[4:0]	4:0	Bonding value.	
50h (101EA1h)	REG101EA1	7:0	Default : 0x80	Access : R/W
	ALLPAD_IN	7	1: Set all pads (except PM) as input.	
	-	6:0	Reserved.	
53h (101EA6h)	REG101EA6	7:0	Default : 0x10	Access : R/W
	UART_SEL1[3:0]	7:4	Select controller for PAD_FUART_RX and PAD_FUART_TX.	

CHIPTOP Register (Bank = 101E)				
Index (Absolute)	Mnemonic	Bit	Description	
	UART_SEL0[3:0]	3:0	Select controller for PAD_PM_UART_RX and PAD_PM_UART_TX. 0000: N/A. 0001: FUART. 0010: UART0. 0011: UART1. 0100: UART2. 0101: UART_DEC. Note: For PAD_PM_UART_RX and PAD_PM_UART_TX, please refer to the "reg_hk51_uart0_en" and "reg_uart_rx_enable" in pm_sleep registers. (a). "reg_hk51_uart0_en" == 0. (b). "reg_uart_rx_enable" == 1.	
53h (101EA7h)	REG101EA7	7:0	Default : 0x32	Access : R/W
	UART_SEL3[3:0]	7:4	Select controller for PAD_UART1_RX and PAD_UART1_TX.	
	UART_SEL2[3:0]	3:0	Select controller for PAD_UART0_RX and PAD_UART0_TX.	
54h (101EA8h)	REG101EA8	7:0	Default : 0x54	Access : R/W
	UART_SEL5[3:0]	7:4	Select controller for PAD_PM_LCD1/LCD0.	
	UART_SEL4[3:0]	3:0	Select controller for PAD_UART2_RX and PAD_UART2_TX.	
55h (101EAAh)	REG101EAA	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	JTAG_SEL[3:0]	3:0	JTAG selection.	
55h (101EABh)	REG101EAB	7:0	Default : 0x00	Access : R/W
	UART_PAD_INVERSE[7:0]	7:0	Invert PAD UART TX/RX.	
56h (101EACh)	REG101EAC	7:0	Default : 0x00	Access : R/W
	UART_INNER_LOOPBACK[7:0]	7:0	Enable of inner loopback test for 3 sets of UART controller. [0]: N/A. [1]: FUART enable. [2]: UART0 enable. [3]: UART1 enable. [4]~[7]: N/A.	
56h (101EADh)	REG101EAD	7:0	Default : 0x00	Access : R/W
	UART_OUTER_LOOPBACK[7:0]	7:0	Enable of outer loopback test for 4 sets of UART pad. [0]: PM_UART enable. [1]: FUART enable. [2]: UART0 enable.	

CHIPTOP Register (Bank = 101E)				
Index (Absolute)	Mnemonic	Bit	Description	
			[3]: UART1 enable. [4]~[7]: N/A.	
57h (101EAEh)	REG101EAE	7:0	Default : 0x00	Access : R/W
	FORCE_RX_DISABLE[7:0]	7:0	Disable RX signals from PADs.	
57h (101EAFh)	REG101EAF	7:0	Default : 0x00	Access : R/W
	FORCE_RX_DISABLE[15:8]	7:0	See description of '101EAEh'.	
58h (101EB0h)	REG101EB0	7:0	Default : 0x00	Access : R/W
	FPGA_MIU_OPTION[7:0]	7:0	FPGA_MIU_OPTION.	
58h (101EB1h)	REG101EB1	7:0	Default : 0x00	Access : R/W
	FPGA_MIU_OPTION[15:8]	7:0	See description of '101EB0h'.	
65h (101ECAh)	REG101ECA	7:0	Default : 0x00	Access : RO
	-	7:5	Reserved.	
	CHIP_CONFIG_STAT[4:0]	4:0	CHIP_CONFIG status.	
65h (101ECBh)	REG101ECB	7:0	Default : 0x00	Access : RO
	-	7:5	Reserved.	
	POWERGOOD_AVDD	4	POWERGOOD_AVDD status.	
	-	3:2	Reserved.	
	IN_SEL_DBUS	1	IN_SEL_DBUS.	
	IN_SEL_SBUS	0	IN_SEL_SBUS.	
69h (101ED3h)	REG101ED3	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	BOOT_FROM_SDRAM	3	Boot from SDRAM. 1: Enable boot from SDRAM. 0: Disable boot from SDRAM.	
	-	2:0	Reserved.	
6Ah (101ED4h)	REG101ED4	7:0	Default : 0x00	Access : R/W
	BOOT_FROM_SDRAM_OFFSET[7:0]	7:0	The booting address of SDRAM.	
6Ah (101ED5h)	REG101ED5	7:0	Default : 0x00	Access : R/W
	BOOT_FROM_SDRAM_OFFSET[15:8]	7:0	See description of '101ED4h'.	
6Bh (101ED6h)	REG101ED6	7:0	Default : 0x00	Access : R/W
	BOOT_FROM_SDRAM_OFFSET[23:16]	7:0	See description of '101ED4h'.	

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6Bh (101ED7h)	REG101ED7	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	BOOT_FROM_SDRAM_OFFSET[25:24]	1:0	See description of '101ED4h'.	
70h (101EE1h)	REG101EE1	7:0	Default : 0x00	Access : R/W
	CLK_CALC_EN	7	CLK_CALC_EN. 1: Enable. 0: Disable.	
	-	6: 3	Reserved.	
	ROSC_OUT_SEL[2:0]	2:0	Ring OSC output select. 000: Select delay chain 0. 001: Select delay chain 1. 010: Select delay chain 2. 011: Select delay chain 3. 100: Select delay chain 4. 101: Select delay chain 5. 110: Select delay chain 6. 111: Select delay chain 7.	
71h (101EE2h)	REG101EE2	7:0	Default : 0x00	Access : RO
	CALC_CNT_REPORT[7:0]	7:0	CALC_CNT_REPORT.	
71h (101EE3h)	REG101EE3	7:0	Default : 0x00	Access : RO
	CALC_CNT_REPORT[15:8]	7:0	See description of '101EE2h'.	
73h (101EE6h)	REG101EE6	7:0	Default : 0xFF	Access : R/W
	RESERVED[7:0]	7:0	Reserved.	
73h (101EE7h)	REG101EE7	7:0	Default : 0xFF	Access : R/W
	RESERVED[15:8]	7:0	See description of '101EE6h'.	
74h (101EE8h)	REG101EE8	7:0	Default : 0x00	Access : R/W
	RESERVED[23:16]	7:0	See description of '101EE6h'.	
74h (101EE9h)	REG101EE9	7:0	Default : 0x00	Access : R/W
	RESERVED[31:24]	7:0	See description of '101EE6h'.	
75h (101EEAh)	REG101EEA	7:0	Default : 0x00	Access : R/W
	TEST_RB	7	Setting for the data arrangement on test bus.	
	TEST_GB	6	Setting for the data arrangement on test bus.	
	TEST_RG	5	Setting for the data arrangement on test bus.	
	-	4	Reserved.	

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	SWAPTEST12BIT	3	Swap MSB 12 bits with LSB 12 bits of test bus.	
	CLK_OUT_SEL[2:0]	2:0	Select TEST_CLK_OUT source. 3'd0: TEST_CLK_OUT = TEST_BUS_GB[0]. 3'd1: TEST_CLK_OUT = TEST_BUS_GB[1]. 3'd2: TEST_CLK_OUT = TEST_BUS_GB[2]. 3'd3: TEST_CLK_OUT = TEST_BUS_GB[3]. 3'd4: TEST_CLK_OUT = TEST_BUS_GB[4]. 3'd5: TEST_CLK_OUT = TEST_BUS_GB[5]. 3'd6: TEST_CLK_OUT = TEST_BUS_GB[6]. 3'd7: TEST_CLK_OUT = TEST_BUS_GB[7].	
75h (101EEBh)	REG101EEB	7:0	Default : 0x00	Access : R/W
	ROSC_IN_SEL	7	Select the input source of ring oscillator in CHIP_CONF. 1: Close-loop (enable ring oscillator). 0: Open-loop (input from external digital input).	
	TESTBUS_EN	6	Enable test bus output (disabled by default).	
	TESTCLK_MODE	5	TESTCLK_MODE used in TEST_CTRL.	
	-	4: 2	Reserved.	
	SEL_CLK_TEST_OUT[1:0]	1:0	Select CLK_TEST_OUT. 2'd0: Select CLK_TEST_OUT[47:0]. 2'd1: Select CLK_TEST_OUT[95:48]. 2'd2: Select CLK_TEST_OUT[143:96]. 2'd3: Reserved.	
76h (101EECh)	REG101EEC	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	SINGLE_CLK_OUT_SEL[2:0]	2:0	Select single CLK_OUT. 3'd1: TEST_BUS[11] = TEST_CLK_OUT_d2. TEST_BUS[10] = TEST_CLK_OUT. 3'd2: TEST_BUS[11] = TEST_CLK_OUT_d2. TEST_BUS[10] = TEST_CLK_OUT_d4. 3'd3: TEST_BUS[11] = TEST_CLK_OUT_d2. TEST_BUS[10] = TEST_CLK_OUT_d8. 3'd4: TEST_BUS[11] = TEST_CLK_OUT_d2. TEST_BUS[10] = TEST_CLK_OUT_d16. 3'd5: TEST_BUS[11] = TEST_CLK_OUT_d2. TEST_BUS[10] = TEST_CLK_OUT_d32. 3'd6: TEST_BUS[11] = TEST_CLK_OUT_d2. TEST_BUS[10] = TEST_CLK_OUT_d64. Others: No TEST_CLK_OUT.	

CHIPTOP Register (Bank = 101E)				
Index (Absolute)	Mnemonic	Bit	Description	
77h (101EEEh)	REG101EEE	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	TEST_BUS24B_SEL[5:0]	5:0	Select TEST_BUS[23:0] source. 6'd2: TEST_BUS = ANA_MISC_TEST_OUT. 6'd3: TEST_BUS = MIU_TEST_OUT. 6'd4: TEST_BUS = DIAMOND_TOP_WP_TEST_OUT. 6'd6: TEST_BUS = UTMI_P1_TEST_OUT. 6'd7: TEST_BUS = UTMI_P2_TEST_OUT. 6'd8: TEST_BUS = AUSDM_TEST_OUT. 6'd9: TEST_BUS = DIG_PM_TEST_OUT. 6'd10: TEST_BUS = MCU_IF_TEST_OUT. 6'd11: TEST_BUS = UTMI_P3_TEST_OUT. 6'd16: TEST_BUS = SC_GP_TEST_OUT. 6'd17: TEST_BUS = DEC_GP_TEST_OUT. 6'd25: TEST_BUS = CLKGEN_TEST_OUT. 6'd26: TEST_BUS = CLKGEN_TEST_OUT2. Others: No TEST_OUT.	
7Bh (101EF6h)	REG101EF6	7:0	Default : 0x00	Access : R/W
	CHIPTOP_RESERVED[7:0]	7:0		
7Bh (101EF7h)	REG101EF7	7:0	Default : 0x00	Access : R/W
	CHIPTOP_RESERVED[15:8]	7:0	See description of '101EF6h'.	
7Ch (101EF8h)	REG101EF8	7:0	Default : 0xFF	Access : R/W
	CHK_CLK_HEMCU_FREQ_CMP_DATA[7:0]	7:0		
7Ch (101EF9h)	REG101EF9	7:0	Default : 0xFF	Access : R/W
	CHK_CLK_HEMCU_FREQ_CMP_DATA[15:8]	7:0	See description of '101EF8h'.	
7Dh (101EFAh)	REG101EFA	7:0	Default : 0x03	Access : R/W
	-	7:4	Reserved.	
	256BUS_2X_DIV_EN[3:0]	3:0	256bus MIU 2x div enable.	
7Eh (101EFCh)	REG101EFC	7:0	Default : 0x0F	Access : R/W
	-	7:4	Reserved.	
	MIU2X_DIV_RSTZ[3:0]	3:0	Clk_MIU2x_div sw rstz. [0]: MIU0. [3:1]: Reserved.	