SSD202D
I2C Module Description

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1. MODULE DESCRIPTION

1.1. Overview

The inter-integrated circuit (I2C) controller provides the master I2C transfer protocol. It contains engine system control by CPU access or DMA transfer. This chip provides two I2C controllers.

1.2. Function Description

The I2C controller has the following features:

- Flexible setting for I2C high and low
- Supports DMA read/write
- Supports 7-bit standard and 10-bit extended address
- Supports n write mode in DMA write mode
- Supports clock stretching

1.3. Operating Mode

1.3.1 General I2C Initialization

- Set I2C configure register
- Set high/low/start/stop count

1.3.2 General I2C Start

- Send start command
- Wait for ready and clear flag

1.3.3 General I2C Write

- Write to the device with Write ID
- Wait for ready and clear flag
- Write address or data into data register
- Wait for ready and clear flag
- Check acknowledgement from slave

1.3.4 General I2C Read

- Read to the device with Write ID
- Wait for ready and clear flag
- Set read ack and trigger read command
- Wait for ready and clear flag
- Read data from register

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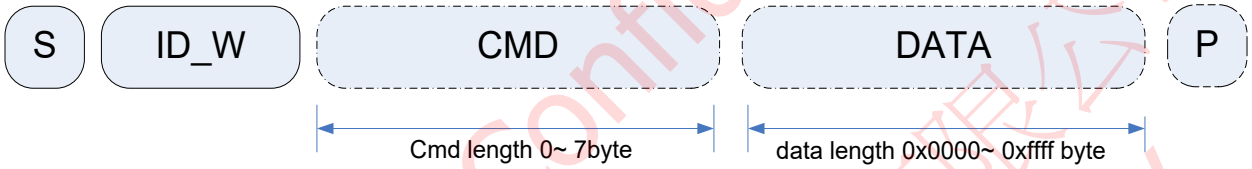
1.3.5 General I2C Stop

- Send stop command
- Wait for ready and clear flag

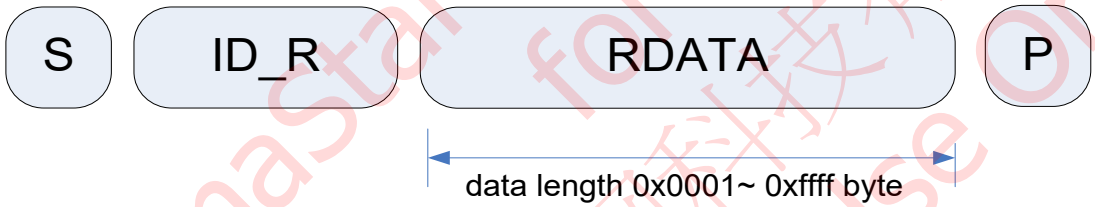
1.3.6 I2C DMA Mode

- Enable DMA mode
- Set DRAM address
- Set I2C configuration register (read/write, transfer format, slave ID…)
- Trigger DMA mode to start engine
- Wait for Interrupt and clear it

DMA write:



DMA read:



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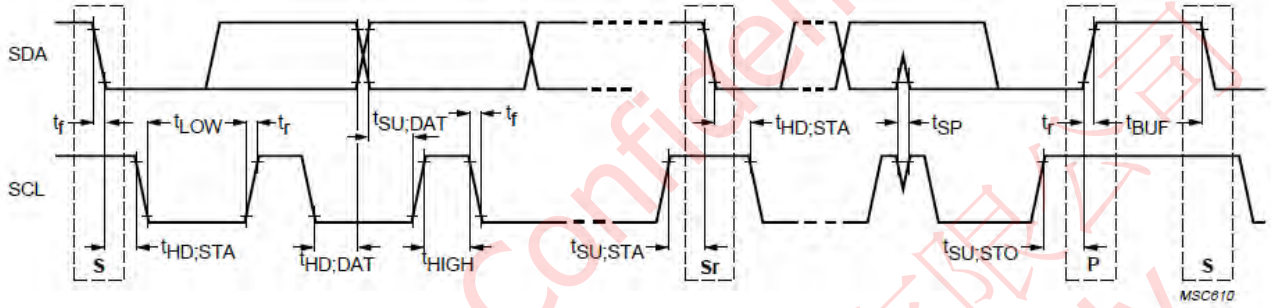
2. AC/DC SPECIFICATION

2.1. AC Timing Diagram



2.2. Standard Mode

Parameter	Symbol	Standard mode		Unit
		Min	Max	
Clock Frequency	fSCL	-	100	kHz
Re-start Hold Time	tHD;STA	4	-	µs
SCL Low Period	tLOW	4.7	-	µs
SCL High Period	tHIGH	4.0	-	µs
RE-start Set-up Time	tSU;STA	4.7	-	µs
SDA Hold Time	tHD;DAT	5	-	µs
SDA Set-up Time	tSU;DAT	250	-	ns
Rise Time of Signals	tr	-	1000	ns
Fall Time of Signals	tf	-	300	ns
STOP Set-up Time	tSU;STO	4.0	-	µs
Bus Free High Time between STOP and START Condition	tBUF	4.7	-	µs

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2.3. Fast Mode

Parameter	Symbol	Fast mode		Unit
		Min	Max	
Clock Frequency	fSCL	-	400	kHz
Re-start Hold Time	tHD;STA	0.6	-	µs
SCL Low Period	tLOW	1.3	-	µs
SCL High Period	tHIGH	0.6	-	µs
RE-start Set-up Time	tSU;STA	0.6	-	µs
SDA Hold Time	tHD;DAT	0	0.9-	µs
SDA Set-up Time	tSU;DAT	100	-	ns
Rise Time of Signals	tr	20+0.1Cb	300	ns
Fall Time of Signals	tf	20+0.1Cb	300	ns
STOP Set-up Time	tSU;STO	0.6	-	µs
Bus Free High Time between STOP and START Condition	tBUF	1.3	-	µs

Note: Cb = total capacitance of one bus line in pF

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3. REGISTER DESCRIPTION

3.1. MIIC0 Register (Bank = 1118)

MIIC0 Register (Bank = 1118)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (111800h)	REG111800	7:0	Default : 0x01	Access : R/W
	MIIC_CFG[7:0]	7:0	MIIC configuration register. Bit[7]: reg_error_det_en. 0: Disable. 1: Enable. Bit[6]: reg_oen_push_en. 0: Disable. 1: Enable. Bit[5]: Enable filter. 0: Disable. 1: Enable. Bit[4]: Enable timeout interrupt. 0: Disable. 1: Enable. Bit[3]: Enable clock stretching. 0: Disable. 1: Enable. Bit[2]: Interrupt enable. 0: Disable. 1: Enable. Bit[1]: Enable DMA. 0: Disable. 1: Enable. Bit[0]: Reset. 0: Reset. 1: Not reset.	
01h (111802h)	REG111802	7:0	Default : 0x00	Access : WO
	-	7:1	Reserved.	
	CMD_START	0	MIIC command. [0]: Start.	
01h (111803h)	REG111803	7:0	Default : 0x00	Access : WO
	-	7:1	Reserved.	

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MIIC0 Register (Bank = 1118)			
Index (Absolute)	Mnemonic	Bit	Description
	CMD_STOP	0	MIIC command. [1]: Stop.
02h (111804h)	REG111804	7:0	Default : 0x00 Access : R/W
	WDATA[7:0]	7:0	I2C write data.
02h (111805h)	REG111805	7:0	Default : 0x00 Access : RO
	-	7:1	Reserved.
	WRITE_ACK	0	I2C ACK for write data from slave IIC.
03h (111806h)	REG111806	7:0	Default : 0x00 Access : RO
	RDATA[7:0]	7:0	I2C read data.
03h (111807h)	REG111807	7:0	Default : 0x00 Access : R/W
	-	7:2	Reserved.
	ACK_BIT	1	I2C ACK for read data to slave IIC.
	RDATA_EN	0	I2C read data trigger.
04h (111808h)	REG111808	7:0	Default : 0x00 Access : R/W
	-	7:1	Reserved.
	FLAG	0	MIIC interrupt flag.
05h (11180Ah)	REG11180A	7:0	Default : 0x00 Access : RO
	-	7:5	Reserved.
	MIIC_STATE[4:0]	4:0	MIIC final state machine (debug only).
05h (11180Bh)	REG11180B	7:0	Default : 0x00 Access : RO
	-	7	Reserved.
	MIIC_INT_STATUS[6:0]	6:0	interrupt status. [0]: Ic_start_det_intr. [1]: Ic_stop_det_intr. [2]: Ic_rx_done_intr. [3]: Ic_tx_done_intr. [4]: Clock_stretching_intr. [5]: Scl_error_inte. [6]: Time_out_intr.
06h (11180Ch)	REG11180C	7:0	Default : 0x00 Access : RO
	-	7:5	Reserved.
	SCLO	4	Pad_SCLO.
	-	3:2	Reserved.
	SDAI	1	Pad_SDAI.
	SCLI	0	Pad_SCLI.

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MIIC0 Register (Bank = 1118)				
Index (Absolute)	Mnemonic	Bit	Description	
08h (111810h)	REG111810	7:0	Default : 0x00	Access : R/W
	STOP_CNT[7:0]	7:0	This register sets the SCL and SDA count for stop.	
08h (111811h)	REG111811	7:0	Default : 0x00	Access : R/W
	STOP_CNT[15:8]	7:0	See description of '111810h'.	
09h (111812h)	REG111812	7:0	Default : 0x00	Access : R/W
	HCNT[7:0]	7:0	This register sets the SCL clock high-period count.	
09h (111813h)	REG111813	7:0	Default : 0x00	Access : R/W
	HCNT[15:8]	7:0	See description of '111812h'.	
0Ah (111814h)	REG111814	7:0	Default : 0x00	Access : R/W
	LCNT[7:0]	7:0	This register sets the SCL clock low-period count.	
0Ah (111815h)	REG111815	7:0	Default : 0x00	Access : R/W
	LCNT[15:8]	7:0	See description of '111814h'.	
0Bh (111816h)	REG111816	7:0	Default : 0x00	Access : R/W
	SDA_CNT[7:0]	7:0	This register sets the clock count between falling edge SCL and SDA.	
0Bh (111817h)	REG111817	7:0	Default : 0x00	Access : R/W
	SDA_CNT[15:8]	7:0	See description of '111816h'.	
0Ch (111818h)	REG111818	7:0	Default : 0x00	Access : R/W
	START_CNT[7:0]	7:0	This register sets the SCL and SDA count for start.	
0Ch (111819h)	REG111819	7:0	Default : 0x00	Access : R/W
	START_CNT[15:8]	7:0	See description of '111818h'.	
0Dh (11181Ah)	REG11181A	7:0	Default : 0x00	Access : R/W
	DATA_LAT_CNT[7:0]	7:0	This register sets the data latch timing.	
0Dh (11181Bh)	REG11181B	7:0	Default : 0x00	Access : R/W
	DATA_LAT_CNT[15:8]	7:0	See description of '11181Ah'.	
0Eh (11181Ch)	REG11181C	7:0	Default : 0x00	Access : R/W
	TIMEOUT_CNT[7:0]	7:0	This register sets timing delay of timeout interrupt occurred.	
0Eh (11181Dh)	REG11181D	7:0	Default : 0x00	Access : R/W
	TIMEOUT_CNT[15:8]	7:0	See description of '11181Ch'.	
0Fh (11181Eh)	REG11181E	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	SCLI_DELAY[2:0]	2:0	Reserved.	

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MIIC0 Register (Bank = 1118)				
Index (Absolute)	Mnemonic	Bit	Description	
20h (111840h)	REG111840	7:0	Default : 0x1A	Access : RO, R/W
	-	7:6	Reserved.	
	MIU_NS	5	MIU secure bit.	
	MIU_PRIORITY	4	Set MIU priority.	
	MIU_RST	3	MIU software reset.	
	DMA_CFG[2:0]	2:0	DMA configuration register. Bit[2]: Interrupt enable. 0: Disable. 1: Enable. Bit[1]: DMA software Reset. 0: Reset. 1: Not reset.	
21h (111842h)	REG111842	7:0	Default : 0x00	Access : R/W
	MIU_ADDR[7:0]	7:0	Get tx data or put rx data address in DRAM.	
21h (111843h)	REG111843	7:0	Default : 0x00	Access : R/W
	MIU_ADDR[15:8]	7:0	See description of '111842h'.	
22h (111844h)	REG111844	7:0	Default : 0x00	Access : R/W
	MIU_ADDR[23:16]	7:0	See description of '111842h'.	
22h (111845h)	REG111845	7:0	Default : 0x00	Access : R/W
	MIU_ADDR[31:24]	7:0	See description of '111842h'.	
23h (111846h)	REG111846	7:0	Default : 0x00	Access : R/W
	MIU_SEL	7	MIIC channel select.	
	READ_CMD	6	MIIC transfer format. 1: Read. 0: Write.	
	STOP_DISABLE	5	MIIC transfer format. 1: S + data .. 0: S + data ...+ P.	
	-	4:0	Reserved.	
24h (111848h)	REG111848	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	DMA_TRANSFER_DONE	0	SW needs to set this bit to clear transfer_done flag or interrupt in order to receive the subsequent DMA transfer_done flag or interrupt.	
25h	REG11184A	7:0	Default : 0x00	Access : R/W

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MIIC0 Register (Bank = 1118)				
Index (Absolute)	Mnemonic	Bit	Description	
(11184Ah)	CMD_DATA[7:0]	7:0	I2C Tx Data Buffer and Command.	
25h (11184Bh)	REG11184B	7:0	Default : 0x00	Access : R/W
	CMD_DATA[15:8]	7:0	See description of '11184Ah'.	
26h (11184Ch)	REG11184C	7:0	Default : 0x00	Access : R/W
	CMD_DATA[23:16]	7:0	See description of '11184Ah'.	
26h (11184Dh)	REG11184D	7:0	Default : 0x00	Access : R/W
	CMD_DATA[31:24]	7:0	See description of '11184Ah'.	
27h (11184Eh)	REG11184E	7:0	Default : 0x00	Access : R/W
	CMD_DATA[39: 32]	7:0	See description of '11184Ah'.	
27h (11184Fh)	REG11184F	7:0	Default : 0x00	Access : R/W
	CMD_DATA[47:40]	7:0	See description of '11184Ah'.	
28h (111850h)	REG111850	7:0	Default : 0x00	Access : R/W
	CMD_DATA[55:48]	7:0	See description of '11184Ah'.	
28h (111851h)	REG111851	7:0	Default : 0x00	Access : R/W
	CMD_DATA[63: 56]	7:0	See description of '11184Ah'.	
29h (111852h)	REG111852	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	CMD_LEN[3:0]	3:0	Transfer command register length (0~8).	
2Ah (111854h)	REG111854	7:0	Default : 0x00	Access : R/W
	DATA_LEN[7:0]	7:0	Transfer command register length.	
2Ah (111855h)	REG111855	7:0	Default : 0x00	Access : R/W
	DATA_LEN[15:8]	7:0	See description of '111854h'.	
2Bh (111856h)	REG111856	7:0	Default : 0x00	Access : R/W
	DATA_LEN[23:16]	7:0	See description of '111854h'.	
2Bh (111857h)	REG111857	7:0	Default : 0x00	Access : R/W
	DATA_LEN[31:24]	7:0	See description of '111854h'.	
2Ch (111858h)	REG111858	7:0	Default : 0x00	Access : RO
	DMA_TC[7:0]	7:0	DMA transfer count register for MIIC0 (debug only).	
2Ch (111859h)	REG111859	7:0	Default : 0x00	Access : RO
	DMA_TC[15:8]	7:0	See description of '111858h'.	
2Dh (11185Ah)	REG11185A	7:0	Default : 0x00	Access : RO
	DMA_TC[23:16]	7:0	See description of '111858h'.	
2Dh	REG11185B	7:0	Default : 0x00	Access : RO

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MIIC0 Register (Bank = 1118)				
Index (Absolute)	Mnemonic	Bit	Description	
(11185Bh)	DMA_TC[31:24]	7:0	See description of '111858h'.	
2Eh (11185Ch)	REG11185C	7:0	Default : 0x00	Access : R/W
	SAR[7:0]	7:0	I2C Slave Address. [9:0]: 10-bit mode slave address. [6:0]: Normal mode slave address.	
2Eh (11185Dh)	REG11185D	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	10BIT_MODE	2	I2C Slave Address mode setting. 1: 10-bit mode slave address. 0: Normal mode slave address.	
	SAR[9: 8]	1:0	See description of '11185Ch'.	
2Fh (11185Eh)	REG11185E	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	DMA_TRIGGER	0	DMA transfer trigger.	
2Fh (11185Fh)	REG11185F	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	RE_TRIGGER	0	DMA transfer RE_TRIGGER, for data transfer not complete.	
31h (111862h)	REG111862	7:0	Default : 0x00	Access : RO
	STATE[7:0]	7:0	DMA FSM (debug only).	
31h (111863h)	REG111863	7:0	Default : 0x00	Access : RO
	-	7:1	Reserved.	
	MIU_LAST_DONE_Z	0	MIU last done z (debug only).	

3.2. MIIC1 Register (Bank = 1119)

MIIC1 Register (Bank = 1119)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (111900h)	REG111900	7:0	Default : 0x01	Access : R/W
	MIIC_CFG[7:0]	7:0	MIIC configuration register. Bit[7]: reg_error_det_en. 0: Disable. 1: Enable. Bit[6]: reg_oen_push_en. 0: Disable.	

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MIIC1 Register (Bank = 1119)				
Index (Absolute)	Mnemonic	Bit	Description	
			1: Enable. Bit[5]: Enable filter. 0: Disable. 1: Enable. Bit[4]: Enable timeout interrupt. 0: Disable. 1: Enable. Bit[3]: Enable clock stretching. 0: Disable. 1: Enable. Bit[2]: Interrupt enable. 0: Disable. 1: Enable. Bit[1]: Enable DMA. 0: Disable. 1: Enable. Bit[0]: Reset. 0: Reset. 1: Not reset.	
01h (111902h)	REG111902	7:0	Default : 0x00	Access : WO
	-	7:1	Reserved.	
	CMD_START	0	MIIC command. [0]: Start.	
01h (111903h)	REG111903	7:0	Default : 0x00	Access : WO
	-	7:1	Reserved.	
	CMD_STOP	0	MIIC command. [1]: Stop.	
02h (111904h)	REG111904	7:0	Default : 0x00	Access : R/W
	WDATA[7:0]	7:0	I2C write data.	
02h (111905h)	REG111905	7:0	Default : 0x00	Access : RO
	-	7:1	Reserved.	
	WRITE_ACK	0	I2C ACK for write data from slave IIC.	
03h (111906h)	REG111906	7:0	Default : 0x00	Access : RO
	RDATA[7:0]	7:0	I2C read data.	
03h (111907h)	REG111907	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	ACK_BIT	1	I2C ACK for read data to slave IIC.	

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MIIC1 Register (Bank = 1119)				
Index (Absolute)	Mnemonic	Bit	Description	
	RDATA_EN	0	I2C read data trigger.	
04h (111908h)	REG111908	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	FLAG	0	MIIC interrupt flag.	
05h (11190Ah)	REG11190A	7:0	Default : 0x00	Access : RO
	-	7:5	Reserved.	
	MIIC_STATE[4:0]	4:0	MIIC final state machine (debug only).	
05h (11190Bh)	REG11190B	7:0	Default : 0x00	Access : RO
	-	7	Reserved.	
	MIIC_INT_STATUS[6:0]	6:0	Interrupt status. [0]: Ic_start_det_intr. [1]: Ic_stop_det_intr. [2]: Ic_rx_done_intr. [3]: Ic_tx_done_intr. [4]: Clock_stretching_intr. [5]: Scl_error_inte. [6]: Time_out_intr.	
06h (11190Ch)	REG11190C	7:0	Default : 0x00	Access : RO
	-	7:5	Reserved.	
	SCLO	4	Pad_SCLO.	
	-	3:2	Reserved.	
	SDAI	1	Pad_SDAI.	
	SCLI	0	Pad_SCLI.	
08h (111910h)	REG111910	7:0	Default : 0x00	Access : R/W
	STOP_CNT[7:0]	7:0	This register sets the SCL and SDA count for stop.	
08h (111911h)	REG111911	7:0	Default : 0x00	Access : R/W
	STOP_CNT[15:8]	7:0	See description of '111910h'.	
09h (111912h)	REG111912	7:0	Default : 0x00	Access : R/W
	HCNT[7:0]	7:0	This register sets the SCL clock high-period count.	
09h (111913h)	REG111913	7:0	Default : 0x00	Access : R/W
	HCNT[15:8]	7:0	See description of '111912h'.	
0Ah (111914h)	REG111914	7:0	Default : 0x00	Access : R/W
	LCNT[7:0]	7:0	This register sets the SCL clock low-period count.	
0Ah	REG111915	7:0	Default : 0x00	Access : R/W

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MIIC1 Register (Bank = 1119)				
Index (Absolute)	Mnemonic	Bit	Description	
(111915h)	LCNT[15:8]	7:0	See description of '111914h'.	
0Bh (111916h)	REG111916	7:0	Default : 0x00	Access : R/W
	SDA_CNT[7:0]	7:0	This register sets the clock count between falling edge SCL and SDA.	
0Bh (111917h)	REG111917	7:0	Default : 0x00	Access : R/W
	SDA_CNT[15:8]	7:0	See description of '111916h'.	
0Ch (111918h)	REG111918	7:0	Default : 0x00	Access : R/W
	START_CNT[7:0]	7:0	This register sets the SCL and SDA count for start.	
0Ch (111919h)	REG111919	7:0	Default : 0x00	Access : R/W
	START_CNT[15:8]	7:0	See description of '111918h'.	
0Dh (11191Ah)	REG11191A	7:0	Default : 0x00	Access : R/W
	DATA_LAT_CNT[7:0]	7:0	This register sets the data latch timing.	
0Dh (11191Bh)	REG11191B	7:0	Default : 0x00	Access : R/W
	DATA_LAT_CNT[15:8]	7:0	See description of '11191Ah'.	
0Eh (11191Ch)	REG11191C	7:0	Default : 0x00	Access : R/W
	TIMEOUT_CNT[7:0]	7:0	This register sets timing delay of timeout interrupt occurred.	
0Eh (11191Dh)	REG11191D	7:0	Default : 0x00	Access : R/W
	TIMEOUT_CNT[15:8]	7:0	See description of '11191Ch'.	
0Fh (11191Eh)	REG11191E	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	SCLI_DELAY[2:0]	2:0	Reserved.	
20h (111940h)	REG111940	7:0	Default : 0x1A	Access : RO, R/W
	-	7:6	Reserved.	
	MIU_NS	5	MIU secure bit.	
	MIU_PRIORITY	4	Set MIU priority.	
	MIU_RST	3	MIU software reset.	
	DMA_CFG[2:0]	2:0	DMA configuration register. Bit[2]: Interrupt enable. 0: Disable. 1: Enable. Bit[1]: DMA software Reset. 0: Reset. 1: Not reset.	
21h	REG111942	7:0	Default : 0x00	Access : R/W

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MIIC1 Register (Bank = 1119)				
Index (Absolute)	Mnemonic	Bit	Description	
(111942h)	MIU_ADDR[7:0]	7:0	Get tx data or put rx data address in DRAM.	
21h (111943h)	REG111943	7:0	Default : 0x00	Access : R/W
	MIU_ADDR[15:8]	7:0	See description of '111942h'.	
22h (111944h)	REG111944	7:0	Default : 0x00	Access : R/W
	MIU_ADDR[23:16]	7:0	See description of '111942h'.	
22h (111945h)	REG111945	7:0	Default : 0x00	Access : R/W
	MIU_ADDR[31:24]	7:0	See description of '111942h'.	
23h (111946h)	REG111946	7:0	Default : 0x00	Access : R/W
	MIU_SEL	7	MIIC channel select.	
	READ_CMD	6	MIIC transfer format. 1: Read. 0: Write.	
	STOP_DISABLE	5	MIIC transfer format. 1: S + data .. 0: S + data ...+ P.	
	-	4:0	Reserved.	
24h (111948h)	REG111948	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	DMA_TRANSFER_DONE	0	SW needs to set this bit to clear transfer_done flag or interrupt in order to receive the subsequent DMA transfer_done flag or interrupt.	
25h (11194Ah)	REG11194A	7:0	Default : 0x00	Access : R/W
	CMD_DATA[7:0]	7:0	I2C Tx Data Buffer and Command.	
25h (11194Bh)	REG11194B	7:0	Default : 0x00	Access : R/W
	CMD_DATA[15:8]	7:0	See description of '11194Ah'.	
26h (11194Ch)	REG11194C	7:0	Default : 0x00	Access : R/W
	CMD_DATA[23:16]	7:0	See description of '11194Ah'.	
26h (11194Dh)	REG11194D	7:0	Default : 0x00	Access : R/W
	CMD_DATA[31:24]	7:0	See description of '11194Ah'.	
27h (11194Eh)	REG11194E	7:0	Default : 0x00	Access : R/W
	CMD_DATA[39: 32]	7:0	See description of '11194Ah'.	
27h (11194Fh)	REG11194F	7:0	Default : 0x00	Access : R/W
	CMD_DATA[47:40]	7:0	See description of '11194Ah'.	
28h	REG111950	7:0	Default : 0x00	Access : R/W

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MIIC1 Register (Bank = 1119)				
Index (Absolute)	Mnemonic	Bit	Description	
(111950h)	CMD_DATA[55:48]	7:0	See description of '11194Ah'.	
28h (111951h)	REG111951	7:0	Default : 0x00	Access : R/W
	CMD_DATA[63: 56]	7:0	See description of '11194Ah'.	
29h (111952h)	REG111952	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	CMD_LEN[3:0]	3:0	Transfer command register length (0~8).	
2Ah (111954h)	REG111954	7:0	Default : 0x00	Access : R/W
	DATA_LEN[7:0]	7:0	Transfer command register length.	
2Ah (111955h)	REG111955	7:0	Default : 0x00	Access : R/W
	DATA_LEN[15:8]	7:0	See description of '111954h'.	
2Bh (111956h)	REG111956	7:0	Default : 0x00	Access : R/W
	DATA_LEN[23:16]	7:0	See description of '111954h'.	
2Bh (111957h)	REG111957	7:0	Default : 0x00	Access : R/W
	DATA_LEN[31:24]	7:0	See description of '111954h'.	
2Ch (111958h)	REG111958	7:0	Default : 0x00	Access : RO
	DMA_TC[7:0]	7:0	DMA transfer count register for MIIC0 (debug only).	
2Ch (111959h)	REG111959	7:0	Default : 0x00	Access : RO
	DMA_TC[15:8]	7:0	See description of '111958h'.	
2Dh (11195Ah)	REG11195A	7:0	Default : 0x00	Access : RO
	DMA_TC[23:16]	7:0	See description of '111958h'.	
2Dh (11195Bh)	REG11195B	7:0	Default : 0x00	Access : RO
	DMA_TC[31:24]	7:0	See description of '111958h'.	
2Eh (11195Ch)	REG11195C	7:0	Default : 0x00	Access : R/W
	SAR[7:0]	7:0	I2C Slave Address. [9:0]: 10-bit mode slave address. [6:0]: Normal mode slave address.	
2Eh (11195Dh)	REG11195D	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	10BIT_MODE	2	I2C Slave Address mode setting. 1: 10-bit mode slave address. 0: Normal mode slave address.	
	SAR[9: 8]	1:0	See description of '11195Ch'.	
2Fh (11195Eh)	REG11195E	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	

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MIIC1 Register (Bank = 1119)				
Index (Absolute)	Mnemonic	Bit	Description	
	DMA_TRIGGER	0	DMA transfer trigger.	
2Fh (11195Fh)	REG11195F	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	RE_TRIGGER	0	DMA transfer RE_TRIGGER, for data transfer not complete.	
31h (111962h)	REG111962	7:0	Default : 0x00	Access : RO
	STATE[7:0]	7:0	DMA FSM (debug only).	
31h (111963h)	REG111963	7:0	Default : 0x00	Access : RO
	-	7:1	Reserved.	
	MIU_LAST_DONE_Z	0	MIU last done z (debug only).	

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