# SSD202D
# SPI Module Description

# 1. MODULE DESCRIPTION

## 1.1. Overview

The SPI module provides a memory controller interface to connect to external SPI NAND/NOR flash. It contains two functions: FSP (Flash Self Programming) and ISP (Internal Self Programming) for different system scenarios.

### 1.1.1 Function Description

The SPI module has the following features:

- Supports 8 read/write buffers to transmit data respectively
- Supports start, end and byte to byte delay for users
- Supports DMA read/write only mode with 24-bit data length
- Supports write data to client first under DMA read mode
- Supports 8 client chip selects
- Supports CPHA, CPOL setting
- Supports read from LSB mode
- Supports full-duplex mode
- Supports three-wire mode

### 1.1.2 Operating Mode

#### *1.1.2.1. Flash Self-Programming Transfer Step*

- FSP initial:
  - Set transfer data to registers.
  - Set how many bytes will be sent to flash during first to third runs.
  - Set how many bytes will be read from flash during first to third runs.
  - Set configuration: number of commands, RDSR in which command, enable, etc.
- FSP trigger:
  - When this bit is set, FSP controller will perform operation.
- FSP status - FSP completed flag:
  - When FSP operation is completed, HW sets this bit as high. Before starting the next data transfer, SW needs to clear this bit.
  - When FSP operation is completed, FSP also issues an interrupt to CPU. SW needs to clear the interrupt.
- FSP read data port:
  - When FSP operation is completed, SW can get data from FSP internal register.

#### *1.1.2.2. Internal Self-Programming Step*

The ISP module accesses SPI flash through I2C protocol to transfer data. It needs to enter a password to enable the engine to ensure security.

- Enter ISP:
  - I2C Start
  - Chip ID
  - ISP password
  - I2C Stop

- Command for ISP engine:
  - Transfer command and data to ISP engine

#### *1.1.2.3. SPI DMA Write through BDMA*

1. Set BDMA destination device to FSP.
2. Set BDMA source setting.
3. Set FSP outside data size.
4. Enable FSP outside mode and set which byte can be replaced as DRAM data.
5. Trigger BDMA and FSP.
6. Wait for FSP interrupt.

#### *1.1.2.4. SPI DMA Read through BDMA*

1. Set BDMA source device to SPI and the source related setting.
2. Set destination device as DRAM or SRAM and the other destination setting.
3. Trigger BDMA.
4. Wait for BDMA done register

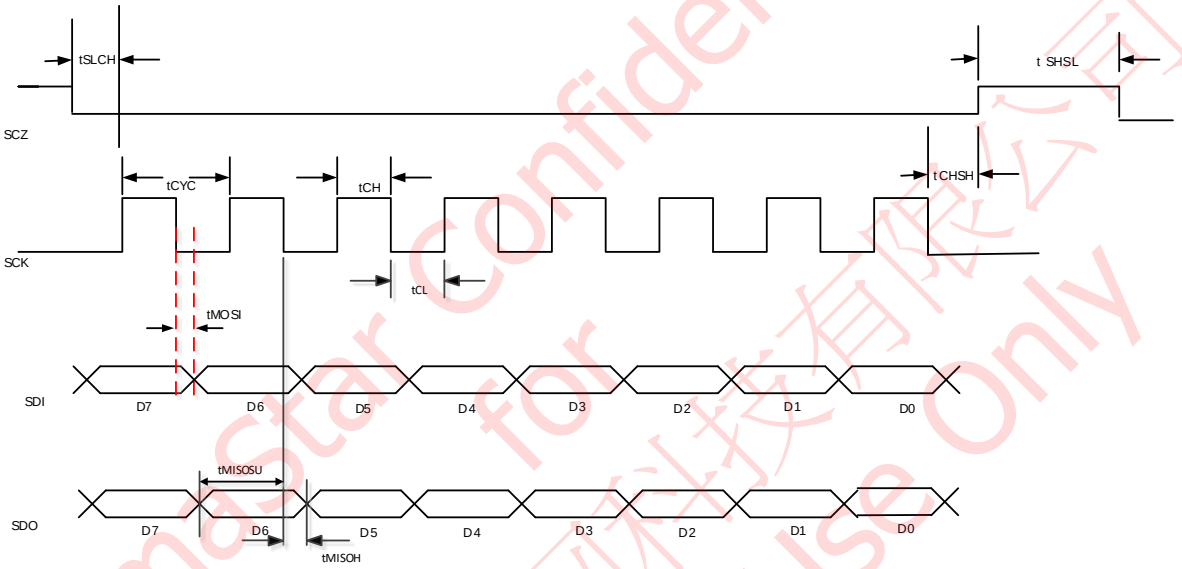
#### *1.1.2.5. SPI Dual/Quad Mode Setting*

1. Set mode register for each command, including general SPI command 0x3B, 0xBB, 0x6B, 0xEB, 0x0B, and 0xEB.
2. Users can define their own command data for each type of transfer mode.

# 2. AC/DC SPECIFICATION

## 2.1. SPI NOR Interface

### 2.1.1 SPI Data Timing - CSZ, SCK, SDI and SDO




### 2.1.2 SPI AC Characteristics for Operation

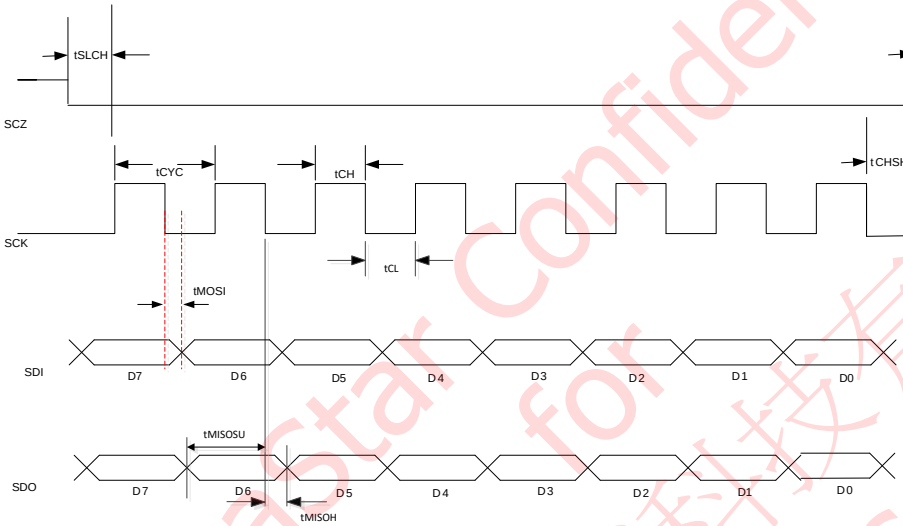
| Parameter | Symbol | Min | Typ | Max | Unit | Remarks |
|---|---|---|---|---|---|---|
| CS High | tSHSL | 1 | | 15 | tCYC | |
| CS Setup | tSLCH | 1 | | 15 | tCYC | |
| CS Hold | tCHSH | 1 | | 15 | tCYC | |
| SCK period | tCYC | 9.3 | | | ns | |
| SCK High Time | tCH | 45 | 50 | 55 | % | |
| SCK Low Time | tCL | 45 | 50 | 55 | % | |
| Master Out Slave In | tMOSI | -2 | | (tCYC/2)-2 | ns | Relative to the falling edge of SCK |
| Master In Slave Out Setup time | tMISOSU | 4.6 | | | ns | Relative to the falling edge of SCK |
| Master In Slave Out Hold time | tMISOH | 0.3 | | | ns | Relative to the falling edge of SCK |

### 2.1.3 SPI DC Characteristics for Operation

| Parameter | Symbol | Min | Typ | Max | Unit | Remarks |
|---|---|---|---|---|---|---|
| Input Low Voltage | VIL | | | 0.9 | V | |
| Input High Voltage | VIH | 2.0 | | | V | |

## 2.2. SPI NAND Interface

### 2.2.1 SPI Data Timing - CSZ, SCK, SDI and SDO




### 2.2.2 SPI AC Characteristics for Operation

| Parameter | Symbol | Min | Typ | Max | Unit | Remarks |
|---|---|---|---|---|---|---|
| CS High | tSHSL | 1 | | 15 | tCYC | |
| CS Setup | tSLCH | 1 | | 15 | tCYC | |
| CS Hold | tCHSH | 1 | | 15 | tCYC | |
| SCK period | tCYC | 9.3 | | | ns | |
| SCK High Time | tCH | 45 | 50 | 55 | % | |
| SCK Low Time | tCL | 45 | 50 | 55 | % | |
| Master Out Slave In | tMOSI | -2 | | (tCYC/2)-2 | ns | Relative to the falling edge of SCK |
| Master In Slave Out Setup time | tMISOSU | 4.6 | | | ns | Relative to the falling edge of SCK |
| Master In Slave Out Hold time | tMISOH | 0.3 | | | ns | Relative to the falling edge of SCK |

### 2.2.3 SPI DC Characteristics for Operation

| Parameter | Symbol | Min | Typ | Max | Unit | Remarks |
|---|---|---|---|---|---|---|
| Input Low Voltage | VIL | | | 0.9 | V | |
| Input High Voltage | VIH | 2.0 | | | V | |

# 3. REGISTER DESCRIPTION

## 3.1. QSPI Register (Bank = 17)

| QSPI Register (Bank = 17) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| 00h (1700h) | REG1700 | 7:0 | Default : 0x00 | Access : R/W |
| | MASK_GRANT[7:0] | 7:0 | | |
| 01h (1702h) | REG1702 | 7:0 | Default : 0x00 | Access : R/W |
| | MASK_TIME_OUT_CTRL[7:0] | 7:0 | | |
| 02h (1705h) | REG1705 | 7:0 | Default : 0x00 | Access : RO |
| | MASK_TIME_OUT_STATUS[7:0] | 7:0 | | |
| 03h (1706h) | REG1706 | 7:0 | Default : 0x00 | Access : R/W |
| | MASK_TIME_OUT_LEN[7:0] | 7:0 | | |
| 03h (1707h) | REG1707 | 7:0 | Default : 0x00 | Access : R/W |
| | MASK_TIME_OUT_LEN[15:8] | 7:0 | See description of '1706h'. | |
| 04h (1708h) | REG1708 | 7:0 | Default : 0x00 | Access : R/W |
| | MASK_TIME_OUT_LEN[23:16] | 7:0 | See description of '1706h'. | |
| 04h (1709h) | REG1709 | 7:0 | Default : 0x10 | Access : R/W |
| | MASK_TIME_OUT_LEN[31:24] | 7:0 | See description of '1706h'. | |
| 05h (170Ah) | REG170A | 7:0 | Default : 0x00 | Access : RO |
| | MASK_TIME_OUT_CNT[7:0] | 7:0 | | |
| 05h (170Bh) | REG170B | 7:0 | Default : 0x00 | Access : RO |
| | MASK_TIME_OUT_CNT[15:8] | 7:0 | See description of '170Ah'. | |
| 06h (170Ch) | REG170C | 7:0 | Default : 0x00 | Access : RO |
| | MASK_TIME_OUT_CNT[23:16] | 7:0 | See description of '170Ah'. | |
| 06h (170Dh) | REG170D | 7:0 | Default : 0x00 | Access : RO |
| | MASK_TIME_OUT_CNT[31:2 | 7:0 | See description of '170Ah'. | |

| QSPI Register (Bank = 17) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | 4] | | | |
| 07h (170Eh) | REG170E | 7:0 | Default : 0x00 | Access : R/W |
| | SPI_ARB_CTRL[7:0] | 7:0 | [0]: Non_pm_ack timeout_en. | |
| 07h (170Fh) | REG170F | 7:0 | Default : 0x00 | Access : RO |
| | SPI_ARB_STATUS[7:0] | 7:0 | [0]: Reg_non_pm_ack timeout_flag. | |
| 08h (1710h) | REG1710 | 7:0 | Default : 0xFF | Access : R/W |
| | NON_PM_ACK_TIMEOUT_LEN[7:0] | 7:0 | | |
| 08h (1711h) | REG1711 | 7:0 | Default : 0x01 | Access : R/W |
| | NON_PM_ACK_TIMEOUT_LEN[15:8] | 7:0 | See description of '1710h'. | |
| 09h (1712h) | REG1712 | 7:0 | Default : 0x00 | Access : RO |
| | NON_PM_ACK_TIMEOUT_CNT[7:0] | 7:0 | | |
| 09h (1713h) | REG1713 | 7:0 | Default : 0x00 | Access : RO |
| | NON_PM_ACK_TIMEOUT_CNT[15:8] | 7:0 | See description of '1712h'. | |
| 0Ah (1714h) | REG1714 | 7:0 | Default : 0x02 | Access : R/W |
| | SPI_SW_MODE[7:0] | 7:0 | [0]: CS SW mode enable.<br>[1]: CS SW control<br>0: CS = 0, 1: CS = 1. | |
| 40h (1780h) | REG1780 | 7:0 | Default : 0x04 | Access : R/W |
| | - | 7:3 | Reserved. | |
| | DELAY_TREE_SEL[2:0] | 2:0 | Value of the delay tree. | |
| 50h (17A0h) | REG17A0 | 7:0 | Default : 0x00 | Access : R/W |
| | CMD_111_M0[7:0] | 7:0 | User-defined command for 1-1-1 normal read mode. | |
| 50h (17A1h) | REG17A1 | 7:0 | Default : 0x00 | Access : R/W |
| | CMD_111_M1[7:0] | 7:0 | User-defined command for 1-1-1 fast read mode. | |
| 51h (17A2h) | REG17A2 | 7:0 | Default : 0x00 | Access : R/W |
| | CMD_112[7:0] | 7:0 | User-defined command for 1-1-2 read mode. | |
| 51h (17A3h) | REG17A3 | 7:0 | Default : 0x00 | Access : R/W |
| | CMD_122[7:0] | 7:0 | User-defined command for 1-2-2 read mode. | |
| 52h (17A4h) | REG17A4 | 7:0 | Default : 0x00 | Access : R/W |
| | CMD_114[7:0] | 7:0 | User-defined command for 1-1-4 read mode. | |

| QSPI Register (Bank = 17) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| 52h (17A5h) | REG17A5 | 7:0 | Default : 0x00 | Access : R/W |
| | CMD_144[7:0] | 7:0 | User-defined command for 1-4-4 read mode. | |
| 53h (17A6h) | REG17A6 | 7:0 | Default : 0x00 | Access : R/W |
| | CMD_444_M0[7:0] | 7:0 | User-defined command for 4-4-4 read mode (dummy cycle = 4). | |
| 53h (17A7h) | REG17A7 | 7:0 | Default : 0x00 | Access : R/W |
| | CMD_444_M1[7:0] | 7:0 | User-defined command for 4-4-4 read mode (dummy cycle = 6). | |
| 54h (17A8h) | REG17A8 | 7:0 | Default : 0x00 | Access : R/W |
| | DUMMY_CYC_VAL[7:0] | 7:0 | User-defined dummy cycle value. | |
| 54h (17A9h) | REG17A9 | 7:0 | Default : 0x00 | Access : R/W |
| | - | 7:4 | Reserved. | |
| | WRAP_VAL[3:0] | 3:0 | User-defined wrap value for SPI NAND. | |
| 58h (17B0h) | REG17B0 | 7:0 | Default : 0x00 | Access : R/W |
| | 2_CMD_111_M0[7:0] | 7:0 | User-defined command for 1-1-1 normal read mode for CS1. | |
| 58h (17B1h) | REG17B1 | 7:0 | Default : 0x00 | Access : R/W |
| | 2_CMD_111_M1[7:0] | 7:0 | User-defined command for 1-1-1 fast read mode for CS1. | |
| 59h (17B2h) | REG17B2 | 7:0 | Default : 0x00 | Access : R/W |
| | 2_CMD_112[7:0] | 7:0 | User-defined command for 1-1-2 read mode for CS1. | |
| 59h (17B3h) | REG17B3 | 7:0 | Default : 0x00 | Access : R/W |
| | 2_CMD_122[7:0] | 7:0 | User-defined command for 1-2-2 read mode for CS1. | |
| 5Ah (17B4h) | REG17B4 | 7:0 | Default : 0x00 | Access : R/W |
| | 2_CMD_114[7:0] | 7:0 | User-defined command for 1-1-4 read mode for CS1. | |
| 5Ah (17B5h) | REG17B5 | 7:0 | Default : 0x00 | Access : R/W |
| | 2_CMD_144[7:0] | 7:0 | User-defined command for 1-4-4 read mode for CS1. | |
| 5Bh (17B6h) | REG17B6 | 7:0 | Default : 0x00 | Access : R/W |
| | 2_CMD_444_M0[7:0] | 7:0 | User-defined command for 4-4-4 read mode for CS1 (dummy cycle = 4). | |
| 5Bh (17B7h) | REG17B7 | 7:0 | Default : 0x00 | Access : R/W |
| | 2_CMD_444_M1[7:0] | 7:0 | User-defined command for 4-4-4 read mode for CS1 (dummy cycle = 6). | |
| 5Ch (17B8h) | REG17B8 | 7:0 | Default : 0x00 | Access : R/W |
| | 2_DUMMY_CYC_VAL[7:0] | 7:0 | User-defined dummy cycle value for CS1. | |

| QSPI Register (Bank = 17) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| 5Ch (17B9h) | REG17B9 | 7:0 | Default : 0x00 | Access : R/W |
| | - | 7:4 | Reserved. | |
| | 2_WRAP_VAL[3:0] | 3:0 | User-defined wrap value for SPI NAND. | |
| 60h (17C0h) | REG17C0 | 7:0 | Default : 0x00 | Access : R/W |
| | - | 7 | Reserved. | |
| | SECOND_CKG_SPI[6:0] | 6:0 | Bit[3:0]: user-defined dummy cycle number for CS1.<br>Bit[4]: user-defined dummy cycle mode enable for CS1.<br>0: Disable.<br>1: Enable. | |
| 60h (17C1h) | REG17C1 | 7:0 | Default : 0x00 | Access : R/W |
| | SECOND_CFG_QSPI[7:0] | 7:0 | Bit[8]: CMD_Bypass_Mode for CS1.<br>Bit[11]: 3/4 byte address mode.<br>0: 3-byte.<br>1: 4-byte. | |
| 61h (17C2h) | REG17C2 | 7:0 | Default : 0x1A | Access : R/W |
| | SECOND_CSZ_SETUP[3:0] | 7:4 | CSZ setup time for CS1 (relative to SCK).<br>4'h0: 1 SPI clock cycle.<br>4.h1: 2 SPI clock cycles.<br>4'hf: 16 SPI clock cycles. | |
| | SECOND_CSZ_HIGH[3:0] | 3:0 | CSZ deselect time for CS1 (SCZ = high).<br>4'h0: 1 SPI clock cycle.<br>4.h1: 2 SPI clock cycles.<br>4'hf: 16 SPI clock cycles. | |
| 61h (17C3h) | REG17C3 | 7:0 | Default : 0x01 | Access : R/W |
| | - | 7:4 | Reserved. | |
| | SECOND_CSZ_HOLD[3:0] | 3:0 | CSZ hold time for CS1 (relative to SCK).<br>4'h0: 1 SPI clock cycle.<br>4.h1: 2 SPI clock cycles.<br>4'hf: 16 SPI clock cycles. | |
| 62h (17C4h) | REG17C4 | 7:0 | Default : 0x00 | Access : R/W |
| | - | 7:4 | Reserved. | |
| | SECOND_MODE_SEL[3:0] | 3:0 | Second SPI model select for CS1.<br>0x0: Normal mode (1-1-1), (SPI command is 0x03).<br>0x1: Enable fast read mode (1-1-1), (SPI command is 0x0B).<br>0x2: Enable (1-1-2) mode, (SPI command is 0x3B).<br>0x3: Enable (1-2-2) mode, (SPI command is 0xBB). | |

| QSPI Register (Bank = 17) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | | | 0xa: Enable (1-1-4) mode, (SPI command is 0x6B).<br>0xb: Enable (1-4-4) mode, (SPI command is 0xEB).<br>0xc: Enable (4-4-4) mode with 4 dummy cycles, (SPI command is 0x0B).<br>0xd: Enable (4-4-4) mode with 6 dummy cycles, (SPI command is 0xEB). | |
| 63h (17C6h) | REG17C6 | 7:0 | Default : 0x00 | Access : R/W |
| | SECOND_REPLACED_CMD[7:0] | 7:0 | The second replaced command for CS1. | |
| 64h (17C8h) | REG17C8 | 7:0 | Default : 0x00 | Access : R/W |
| | - | 7:4 | Reserved. | |
| | CLK_DIV_CNT_EN | 3 | SPI receive div. counter enable. | |
| | CLK_DIV_CNT_SEL[2:0] | 2:0 | SPI receive div. counter output mux select. | |
| 66h (17CCh) | REG17CC | 7:0 | Default : 0xFF | Access : R/W |
| | TIMEOUT_CNT_VALUE[7:0] | 7:0 | Timeout counter value. | |
| 66h (17CDh) | REG17CD | 7:0 | Default : 0xFF | Access : R/W |
| | TIMEOUT_CNT_VALUE[15:8] | 7:0 | See description of '17CCh'. | |
| 67h (17CEh) | REG17CE | 7:0 | Default : 0xFF | Access : R/W |
| | TIMEOUT_CNT_VALUE[23:16] | 7:0 | See description of '17CCh'. | |
| 67h (17CFh) | REG17CF | 7:0 | Default : 0x40 | Access : R/W |
| | TIMEOUT_CNT_EN | 7 | Timeout counter enable. | |
| | TIMEOUT_CNT_RST | 6 | Timeout counter reset. | |
| | - | 5:0 | Reserved. | |
| 68h (17D0h) | REG17D0 | 7:0 | Default : 0x00 | Access : R/W |
| | CSZ_REPLACE_VAL[3:0] | 7:4 | CSZ signal replaced by register value.<br>B0: CS0 replace value.<br>B1: CS1 replace value.<br>B2: CS2 replace value.<br>B3: CS3 replace value. | |
| | CSZ_REPLACE_EN[3:0] | 3:0 | Enable function for CSZ signal replacement by register value.<br>B0: CS0 replace enable.<br>B1: CS1 replace enable.<br>B2: CS2 replace enable.<br>B3: CS3 replace enable. | |

| QSPI Register (Bank = 17) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| 6Dh (17DAh) | REG17DA | 7:0 | Default : 0x1A | Access : R/W |
| | FSP_CSZ_SETUP[3:0] | 7:4 | CSZ setup time for FSP (relative to SCK).<br>4'h0: 1 SPI clock cycle.<br>4.h1: 2 SPI clock cycles.<br>4'hf: 16 SPI clock cycles. | |
| | FSP_CSZ_HIGH[3:0] | 3:0 | CSZ deselect time for FSP (SCZ = high).<br>4'h0: 1 SPI clock cycle.<br>4.h1: 2 SPI clock cycles.<br>4'hf: 16 SPI clock cycles. | |
| 6Dh (17DBh) | REG17DB | 7:0 | Default : 0x01 | Access : R/W |
| | - | 7:4 | Reserved. | |
| | FSP_CSZ_HOLD[3:0] | 3:0 | CSZ hold time for FSP (relative to SCK).<br>4'h0: 1 SPI clock cycle.<br>4.h1: 2 SPI clock cycles.<br>4'hf: 16 SPI clock cycles. | |
| 6Eh (17DCh) | REG17DC | 7:0 | Default : 0x1A | Access : R/W |
| | FSP2_CSZ_SETUP[3:0] | 7:4 | CSZ setup time for FSP2 (relative to SCK).<br>4'h0: 1 SPI clock cycle.<br>4.h1: 2 SPI clock cycles.<br>4'hf: 16 SPI clock cycles. | |
| | FSP2_CSZ_HIGH[3:0] | 3:0 | CSZ deselect time for FSP2 (SCZ = high).<br>4'h0: 1 SPI clock cycle.<br>4.h1: 2 SPI clock cycles.<br>4'hf: 16 SPI clock cycles. | |
| 6Eh (17DDh) | REG17DD | 7:0 | Default : 0x01 | Access : R/W |
| | - | 7:4 | Reserved. | |
| | FSP2_CSZ_HOLD[3:0] | 3:0 | CSZ hold time for FSP2 (relative to SCK).<br>4'h0: 1 SPI clock cycle.<br>4.h1: 2 SPI clock cycles.<br>4'hf: 16 SPI clock cycles. | |
| 70h (17E0h) | REG17E0 | 7:0 | Default : 0x00 | Access : R/W |
| | - | 7 | Reserved. | |
| | CKG_SPI[6:0] | 6:0 | Bit[3:0]: user-defined dummy cycle number.<br>Bit[4]: user-defined dummy cycle mode enable.<br>0: Disable.<br>1: Enable.<br>Bit[5]: Force to disable address continue at FSP mode. | |

| QSPI Register (Bank = 17) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | | | 0: Disable.<br>1: Enable. | |
| 70h<br>(17E1h) | REG17E1 | 7:0 | Default : 0x00 | Access : R/W |
| | CFG_QSPI[7:0] | 7:0 | Bit[8]: CMD_Bypass_Mode.<br>Bit[9]: disable address continue.<br>Bit[10]: wait FSP done.<br>Bit[11]: 3/4 byte address mode.<br>0: 3-byte.<br>1: 4-byte. | |
| 71h<br>(17E2h) | REG17E2 | 7:0 | Default : 0x1A | Access : R/W |
| | CSZ_SETUP[3:0] | 7:4 | CSZ setup time (relative to SCK).<br>4'h0: 1 SPI clock cycle.<br>4.h1: 2 SPI clock cycles.<br>4'hf: 16 SPI clock cycles. | |
| | CSZ_HIGH[3:0] | 3:0 | CSZ deselect time (SCZ = high).<br>4'h0: 1 SPI clock cycle.<br>4.h1: 2 SPI clock cycles.<br>4'hf: 16 SPI clock cycles. | |
| 71h<br>(17E3h) | REG17E3 | 7:0 | Default : 0x01 | Access : R/W |
| | - | 7:4 | Reserved. | |
| | CSZ_HOLD[3:0] | 3:0 | CSZ hold time (relative to SCK).<br>4'h0: 1 SPI clock cycle.<br>4.h1: 2 SPI clock cycles.<br>4'hf: 16 SPI clock cycles. | |
| 72h<br>(17E4h) | REG17E4 | 7:0 | Default : 0x00 | Access : R/W |
| | - | 7:4 | Reserved. | |
| | MODE_SEL[3:0] | 3:0 | SPI model select (command-address-data).<br>0x0: Normal mode (1-1-1), (SPI command is 0x03).<br>0x1: Enable fast read mode (1-1-1), (SPI command is 0x0B).<br>0x2: Enable (1-1-2) mode, (SPI command is 0x3B).<br>0x3: Enable (1-2-2) mode, (SPI command is 0xBB).<br>0xa: Enable (1-1-4) mode, (SPI command is 0x6B).<br>0xb: Enable (1-4-4) mode, (SPI command is 0xEB).<br>0xc: Enable (4-4-4) mode with 4 dummy cycles, (SPI command is 0x0B).<br>0xd: Enable (4-4-4) mode with 6 dummy cycles, (SPI command is 0xEB). | |

| QSPI Register (Bank = 17) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| 73h (17E6h) | REG17E6 | 7:0 | Default : 0x00 | Access : R/W |
| | REPLACED_CMD[7:0] | 7:0 | The replaced command. | |
| 74h (17E8h) | REG17E8 | 7:0 | Default : 0x00 | Access : R/W |
| | SPARE_0[7:0] | 7:0 | Bit[0]: wrap mode for CS0 flash, for SW to write when the flash enters into wrap mode.<br>0: Not wrap mode.<br>1: Wrap mode.<br>Bit[1]: wrap 16 bytes for CS0 flash, for SW to write.<br>0: Not 16 byte.<br>1: 16 byte.<br>Bit[2]: wrap 32 bytes for CS0 flash, for SW to write.<br>0: Not 32 byte.<br>1: 32 byte.<br>Bit[3]: wrap 64 bytes for CS0 flash, for SW to write.<br>0: Not 64 byte.<br>1: 64 byte.<br>Bit[4]: wrap 128 bytes for CS0 flash, for SW to write.<br>0: Not 128 byte.<br>1: 128 byte.<br>Bit[7:5]: reserved, keep the data as default value.<br>Bit[8]: wrap mode for CS1 flash, for SW to write when the flash enters into wrap mode.<br>0: Not wrap mode.<br>1: Wrap mode.<br>Bit[9]: wrap 16 bytes for CS1 flash, for SW to write.<br>0: Not 16 byte.<br>1: 16 byte.<br>Bit[10]: wrap 32 bytes for CS1 flash, for SW to write.<br>0: Not 32 byte.<br>1: 32 byte.<br>Bit[11]: wrap 64 bytes for CS1 flash, for SW to write.<br>0: Not 64 byte.<br>1: 64 byte.<br>Bit[12]: wrap 128 bytes for CS1 flash, for SW to write.<br>0: Not 128 byte.<br>1: 128 byte.<br>Bit[15:13]: reserved, keep the data as default value. | |
| 74h (17E9h) | REG17E9 | 7:0 | Default : 0x00 | Access : R/W |
| | SPARE_0[15:8] | 7:0 | See description of '17E8h'. | |

| QSPI Register (Bank = 17) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| 76h (17ECh) | REG17EC | 7:0 | Default : 0x00 | Access : RO |
| | DEBUG_BUS_0[7:0] | 7:0 | DEBUG_BUS_0. | |
| 76h (17EDh) | REG17ED | 7:0 | Default : 0x00 | Access : RO |
| | DEBUG_BUS_0[15:8] | 7:0 | See description of '17ECh'. | |
| 77h (17EEh) | REG17EE | 7:0 | Default : 0x00 | Access : RO |
| | DEBUG_BUS_1[7:0] | 7:0 | DEBUG_BUS_1. | |
| 77h (17EFh) | REG17EF | 7:0 | Default : 0x00 | Access : RO |
| | DEBUG_BUS_1[15:8] | 7:0 | See description of '17EEh'. | |
| 78h (17F0h) | REG17F0 | 7:0 | Default : 0x00 | Access : RO |
| | DEBUG_BUS_2[7:0] | 7:0 | DEBUG_BUS_2. | |
| 78h (17F1h) | REG17F1 | 7:0 | Default : 0x00 | Access : RO |
| | DEBUG_BUS_2[15:8] | 7:0 | See description of '17F0h'. | |
| 79h (17F2h) | REG17F2 | 7:0 | Default : 0x00 | Access : RO |
| | DEBUG_BUS_3[7:0] | 7:0 | DEBUG_BUS_3. | |
| 79h (17F3h) | REG17F3 | 7:0 | Default : 0x00 | Access : RO |
| | DEBUG_BUS_3[15:8] | 7:0 | See description of '17F2h'. | |
| 7Ah (17F4h) | REG17F4 | 7:0 | Default : 0x00 | Access : R/W |
| | - | 7:2 | Reserved. | |
| | CHIP_SELECT[1:0] | 1:0 | 00: Select external #1 SPI Flash.<br>01: Select external #2 SPI Flash.<br>10: Select external #3 SPI Flash.<br>11: Reserved. | |
| 7Bh (17F6h) | REG17F6 | 7:0 | Default : 0x00 | Access : RO |
| | - | 7:1 | Reserved. | |
| | SWITCH_CS_BUSY | 0 | 1: Switch SPI CS is busy<br>(In this stage, access to SPI Flash is forbidden).<br>0: Switch SPI CS is done. | |
| 7Ch (17F8h) | REG17F8 | 7:0 | Default : 0xFF | Access : R/W |
| | FUNC_SETTING_DEF1[7:0] | 7:0 | Bit[0]: reserved.<br>Bit[1]: use comb. CSZ setting (setup and high).<br>0: Disable.<br>1: Enable.<br>Bit[2]: reserved.<br>Bit[4:3]: Embedded flash size.<br>00: 64Mb. | |

| QSPI Register (Bank = 17) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | | | 01: 128Mb.<br>10: 16Mb.<br>11: 32Mb.<br>Bit[15:5]: reserved, keep the data as default value. | |
| 7Ch (17F9h) | REG17F9 | 7:0 | Default : 0xFF | Access : R/W |
| | FUNC_SETTING_DEF1[15:8] | 7:0 | See description of '17F8h'. | |
| 7Dh (17FAh) | REG17FA | 7:0 | Default : 0x00 | Access : R/W |
| | FUNC_SETTING_DEF0[7:0] | 7:0 | Bit[0]: use index to support 4-byte address.<br>0: Disable.<br>1: Enable.<br>Bit[1]: one burst data over two flash enable.<br>0: Disable.<br>1: Enable.<br>Bit[2]: 4-byte address mode enable.<br>0: Disable.<br>1: Enable.<br>Bit[3]: use user-defined command.<br>0: Use default command.<br>1: Use user-defined command.<br>Bit[4]: use user-defined dummy cycle value at command bypass mode.<br>0: Use 0xa5.<br>1: Use user-defined value.<br>Bit[5]: incremental command at flash wrap mode support enable.<br>0: Disable.<br>1: Enable.<br>Bit[6]: wrap command at flash non-wrap mode support enable.<br>0: Disable.<br>1: Enable.<br>Bit[7]: reserved, keep the data as default value.<br>Bit[8]: SPI IO pin mode after FSP read.<br>0: Output mode.<br>1: Input mode.<br>Bit[9]: CS select by address enable.<br>Bit[10]: reserved.<br>Bit[11]: addr_2byte_en.<br>Bit[12]: force_dummy_cyc_en.<br>Bit[13]: addr_over_write_en. | |

| QSPI Register (Bank = 17) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | | | Bit[15:12]: reserved, keep the data as default value. | |
| 7Dh (17FBh) | REG17FB | 7:0 | Default : 0x00 | Access : R/W |
| | FUNC_SETTING_DEF0[15:8] | 7:0 | See description of '17FAh'. | |
| 7Fh (17FEh) | REG17FE | 7:0 | Default : 0x00 | Access : R/W |
| | - | 7:1 | Reserved. | |
| | ENDIA | 0 | For 32-bit CPU read data. | |