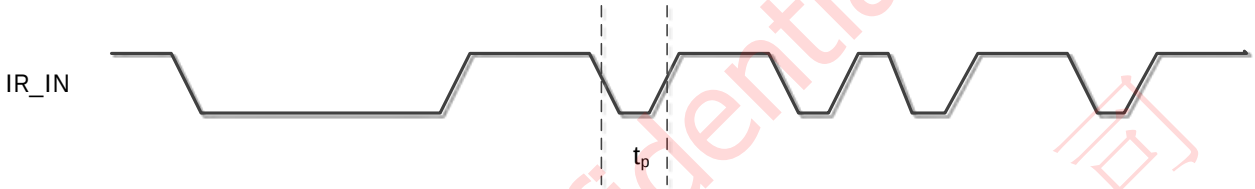
SSD202D
IR Module Description

1. AC/DC SPECIFICATION

1.1. AC Timing Diagram



1.2. IR SW Mode

Parameter	Symbol	Standard Mode		Unit
		Min.	Max.	
Pulse Width	t_p	1.0	20000.0	us

2. REGISTER DESCRIPTION

2.1. IR Register (Bank = 3D)

IR Register (Bank = 3D)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (3D00h)	REG3D00	7:0	Default : 0x1F	Access : R/W
	RC_FIFO_WFIRST	7	RC FIFO write first. 0: Read first; 1: write first.	
	RC_FIFO_CLEAR	6	RC FIFO clear. 0: Disable; 1: enable.	
	RC_AUTOCONFIG	5	Auto config RC5 and RC6 setting.	
	RC6_LS_THR_L[4:0]	4:0	RC6 leading pulse threshold * 32.	
00h (3D01h)	REG3D01	7:0	Default : 0x70	Access : R/W
	RCIN_INV	7	RC input invert. 0=disabe;1=enable.	
	RC_DEBUG_SEL[2:0]	6:4	111: PM RC anykey wakeup fix enable. Others: Reserved.	
	RC_WKUP_EN	3	RC wake up enable. 0=disable; 1=enable.	
	RC5EXT_EN	2	Extended RC-5 enable. 0=disable; 1=enable.	
	RC6_EN	1	0= RC5;1= RC6.	
	RC_EN	0	RC receiver enable. 0=disable; 1=enable.	
01h (3D02h)	REG3D02	7:0	Default : 0xA0	Access : R/W
	RC_LONGPULSE_THR[7:0]	7:0	RC long pulse threshold. To judge long pulse or not.	
01h (3D03h)	REG3D03	7:0	Default : 0x04	Access : R/W
	-	7:5	Reserved.	
	RC_LONGPULSE_THR[12:8]	4:0	See description of '3D02h'.	
02h (3D04h)	REG3D04	7:0	Default : 0xC0	Access : R/W
	RC_LONGPULSE_MAR[7:0]	7:0	RC6 long pulse margin, only for RC6.	
02h (3D05h)	REG3D05	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	

IR Register (Bank = 3D)				
Index (Absolute)	Mnemonic	Bit	Description	
	RC6_LS_THR_H[2:0]	4:2	RC6 leading pulse threshold * 1024.	
	RC_LONGPULSE_MAR[9:8]	1:0	See description of '3D04h'.	
03h (3D06h)	REG3D06	7:0	Default : 0x41	Access : R/W
	RC_INT_THR[6:0]	7:1	RC Integrator threshold * 8. To judge 0 or 1.	
	RC6_ECO_EN	0	RC6 ECO function enable.	
03h (3D07h)	REG3D07	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	RC_CLKDIV[4:0]	4:0	RC operating clock divisor ratio.	
04h (3D08h)	REG3D08	7:0	Default : 0x3C	Access : R/W
	RC_WDOG_COUNT[7:0]	7:0	RC watch dog counter (based on 2kHz for 1MHz clock input).	
04h (3D09h)	REG3D09	7:0	Default : 0x10	Access : R/W
	RC_TIMEOUT_COUNT[7:0]	7:0	RC timeout counter (based on 0.5kHz for 1MHz clock input).	
05h (3D0Ah)	REG3D0A	7:0	Default : 0xFF	Access : R/W
	COMP_RCKEY1[7:0]	7:0	RC power wakeup key1.	
05h (3D0Bh)	REG3D0B	7:0	Default : 0xFF	Access : R/W
	COMP_RCKEY2[7:0]	7:0	RC power wakeup key2.	
06h (3D0Ch)	REG3D0C	7:0	Default : 0x00	Access : RO
	RCKEY_ADDRESS[7:0]	7:0	RC decode address. RC5: {2'b0,toggle,address[4:0]}. RC6: Address[7:0].	
06h (3D0Dh)	REG3D0D	7:0	Default : 0x00	Access : RO
	RCKEY_COMMAND[7:0]	7:0	RC decode command. RC5: {repeat,1'b0,command[5:0]}. RC5EXT: {repeat,command[6:0]}. RC6: Command[7:0].	
07h (3D0Eh)	REG3D0E	7:0	Default : 0x00	Access : RO
	-	7:5	Reserved.	
	RCKEY_MISC[4:0]	4:0	RC6 decode MISC data. [2:0]: MODE[2:0]. [3]: Toggle. [4]: Repeat.	
08h	REG3D10	7:0	Default : 0x00	Access : RO

IR Register (Bank = 3D)				
Index (Absolute)	Mnemonic	Bit	Description	
(3D10h)	-	7	Reserved.	
	RC_FIFO_WPTR[2:0]	6:4	RC FIFO write pointer.	
	-	3	Reserved.	
	RC_FIFO_FULL	2	RC FIFO full.	
	RC_TIMEOUT_FLAG	1	RC time-out flag. 1: Time-out.	
	RC_FIFO_EMPTY	0	RC FIFO empty.	
08h (3D11h)	REG3D11	7:0	Default : 0x00	Access : RO
	-	7:3	Reserved.	
	RC_FIFO_RPTR[2:0]	2:0	RC FIFO read pointer.	
09h (3D12h)	REG3D12	7:0	Default : 0x00	Access : WO
	-	7:1	Reserved.	
	RC_FIFO_RD_PULSE	0	RC FIFO read pulse gen.	
09h (3D13h)	REG3D13	7:0	Default : 0x00	Access : WO
	-	7:1	Reserved.	
	RC_WKUP_CLR	0	RC wake up clear pulse generator.	
0Ah (3D14h)	REG3D14	7:0	Default : 0xFF	Access : R/W
	RC_ADDRESS[7:0]	7:0	RC power wakeup address.	
0Ah (3D15h)	REG3D15	7:0	Default : 0x01	Access : R/W
	RC_BOUND_DET_MODE	7	RC boundary detection mode. 0: Threshold detect. 1: Boundary detect.	
	-	6:2	Reserved.	
	RC_ANYKEY_EN	1	RC anykey wakeup enable.	
	RCADR_CMP_EN	0	RC power wakeup address enable.	
10h (3D20h)	REG3D20	7:0	Default : 0x00	Access : R/W
	RC_1T_LB[7:0]	7:0	RC 1T pulse low bound.	
10h (3D21h)	REG3D21	7:0	Default : 0x00	Access : R/W
	RSVD_10_3B[2:0]	7:5	Reserved.	
	RC_1T_LB[12:8]	4:0	See description of '3D20h'.	
11h (3D22h)	REG3D22	7:0	Default : 0x00	Access : R/W
	RC_1T_HB[7:0]	7:0	RC 1T pulse high bound.	
11h (3D23h)	REG3D23	7:0	Default : 0x00	Access : R/W
	RSVD_11_3B[2:0]	7:5	Reserved.	

IR Register (Bank = 3D)				
Index (Absolute)	Mnemonic	Bit	Description	
	RC_1T_HB[12:8]	4:0	See description of '3D22h'.	
12h (3D24h)	REG3D24	7:0	Default : 0x00	Access : R/W
	RC_2T_LB[7:0]	7:0	RC 2T pulse low bound.	
12h (3D25h)	REG3D25	7:0	Default : 0x00	Access : R/W
	RSVD_12_3B[2:0]	7:5	Reserved.	
	RC_2T_LB[12:8]	4:0	See description of '3D24h'.	
13h (3D26h)	REG3D26	7:0	Default : 0x00	Access : R/W
	RC_2T_HB[7:0]	7:0	RC 2T pulse high bound.	
13h (3D27h)	REG3D27	7:0	Default : 0x00	Access : R/W
	RSVD_13_3B[2:0]	7:5	Reserved.	
	RC_2T_HB[12:8]	4:0	See description of '3D26h'.	
14h (3D28h)	REG3D28	7:0	Default : 0x00	Access : R/W
	RC_3T_LB[7:0]	7:0	RC 3T pulse low bound.	
14h (3D29h)	REG3D29	7:0	Default : 0x00	Access : R/W
	RSVD_14_3B[2:0]	7:5	Reserved.	
	RC_3T_LB[12:8]	4:0	See description of '3D28h'.	
15h (3D2Ah)	REG3D2A	7:0	Default : 0x00	Access : R/W
	RC_3T_HB[7:0]	7:0	RC 3T pulse high bound.	
15h (3D2Bh)	REG3D2B	7:0	Default : 0x00	Access : R/W
	RSVD_15_3B[2:0]	7:5	Reserved.	
	RC_3T_HB[12:8]	4:0	See description of '3D2Ah'.	
16h (3D2Ch)	REG3D2C	7:0	Default : 0x00	Access : R/W
	RC_6T_LB[7:0]	7:0	RC 6T pulse low bound.	
16h (3D2Dh)	REG3D2D	7:0	Default : 0x00	Access : R/W
	RSVD_16_3B[2:0]	7:5	Reserved.	
	RC_6T_LB[12:8]	4:0	See description of '3D2Ch'.	
17h (3D2Eh)	REG3D2E	7:0	Default : 0x00	Access : R/W
	RC_6T_HB[7:0]	7:0	RC 6T pulse high bound.	
17h (3D2Fh)	REG3D2F	7:0	Default : 0x00	Access : R/W
	RSVD_17_3B[2:0]	7:5	Reserved.	
	RC_6T_HB[12:8]	4:0	See description of '3D2Eh'.	
40h (3D80h)	REG3D80	7:0	Default : 0xBE	Access : R/W
	IR_INV	7	Invert the polarity for input IR signal.	

IR Register (Bank = 3D)				
Index (Absolute)	Mnemonic	Bit	Description	
	IR_INT_MASK	6	IR Interrupt request Mask for mcu.	
	IR_RPCODE_EN	5	IR Repeat Code check enable.	
	IR_LG01H_CHK_EN	4	IR Logic 0/1 High level edge Check Enable.	
	IR_DCODE_PCHK_EN	3	IR Data Code Parity Check Enable.	
	IR_CCODE0_CHK_EN	2	IR Customer Code 0 Check Enable. (There are two customer codes could be set for decoding different remote controller.).	
	IR_LDCCHK_EN	1	IR Leader Code (header + off code) Check Enable.	
	IR_EN	0	IR decode Enable for Full/Raw mode.	
40h (3D81h)	REG3D81	7:0	Default : 0xC1	Access : R/W
	IR_INT_CRC_MASK	7	Interrupt Mask for IR CRC check.	
	RAW_RPT_INT_MASK	6	Interrupt Mask for Repeat code in RAW mode.	
	IR_TSTBUS_SEL[1:0]	5:4	IR TESTBUS output select. 0: Select testbus 0. 1: Select testbus 1. 2: Select testbus 2. 3: Select testbus 0.	
	IR_BIT_INV_EN	3	Enable for IR decode logic bit inverse. 0: Disable. 1: Enable.	
	IR_KEY_MSB_FIRST	2	Enable for IR key MSB first. 0: The key data format is LSB first. (ie, key[0:7]). 1: The key data format is MSB first (ie, key[7:0]).	
	IR_SEPR_EN	1	IR Separator Code check Enable (for Mitsubishi only).	
	IR_TIMEOUT_CHK_EN	0	IR Time-Out Check Enable.	
41h (3D82h)	REG3D82	7:0	Default : 0xF2	Access : R/W
	IR_HDC_UPB[7:0]	7:0	The counter Upper Bound for Header Code.	
41h (3D83h)	REG3D83	7:0	Default : 0x2B	Access : R/W
	-	7:6	Reserved.	
	IR_HDC_UPB[13:8]	5:0	See description of '3D82h'.	
42h (3D84h)	REG3D84	7:0	Default : 0x5E	Access : R/W
	IR_HDC_LOB[7:0]	7:0	The counter Lower Bound for Header Code.	
42h (3D85h)	REG3D85	7:0	Default : 0x1A	Access : R/W
	-	7:6	Reserved.	

IR Register (Bank = 3D)				
Index (Absolute)	Mnemonic	Bit	Description	
	IR_HDC_LOB[13:8]	5:0	See description of '3D84h'.	
43h (3D86h)	REG3D86	7:0	Default : 0xF9	Access : R/W
	IR_OFC_UPB[7:0]	7:0	The counter Upper Bound for Off Code.	
43h (3D87h)	REG3D87	7:0	Default : 0x15	Access : R/W
	-	7:5	Reserved.	
	IR_OFC_UPB[12:8]	4:0	See description of '3D86h'.	
44h (3D88h)	REG3D88	7:0	Default : 0x2F	Access : R/W
	IR_OFC_LOB[7:0]	7:0	The counter Lower Bound for Off Code.	
44h (3D89h)	REG3D89	7:0	Default : 0x0D	Access : R/W
	-	7:5	Reserved.	
	IR_OFC_LOB[12:8]	4:0	See description of '3D88h'.	
45h (3D8Ah)	REG3D8A	7:0	Default : 0x35	Access : R/W
	IR_OFC_RP_UPB[7:0]	7:0	The counter Upper Bound for Repeat Off Code.	
45h (3D8Bh)	REG3D8B	7:0	Default : 0x0C	Access : R/W
	-	7:5	Reserved.	
	IR_OFC_RP_UPB[12:8]	4:0	See description of '3D8Ah'.	
46h (3D8Ch)	REG3D8C	7:0	Default : 0x53	Access : R/W
	IR_OFC_RP_LOB[7:0]	7:0	The counter Lower Bound for Repeat Off Code.	
46h (3D8Dh)	REG3D8D	7:0	Default : 0x07	Access : R/W
	-	7:5	Reserved.	
	IR_OFC_RP_LOB[12:8]	4:0	See description of '3D8Ch'.	
47h (3D8Eh)	REG3D8E	7:0	Default : 0xBC	Access : R/W
	IR_LG01H_UPB[7:0]	7:0	The counter Upper Bound for Logic 0/1 High level width.	
47h (3D8Fh)	REG3D8F	7:0	Default : 0x02	Access : R/W
	-	7:2	Reserved.	
	IR_LG01H_UPB[9:8]	1:0	See description of '3D8Eh'.	
48h (3D90h)	REG3D90	7:0	Default : 0xA4	Access : R/W
	IR_LG01H_LOB[7:0]	7:0	The counter Lower Bound for Logic 0/1 High level width.	
48h (3D91h)	REG3D91	7:0	Default : 0x01	Access : R/W
	-	7:2	Reserved.	
	IR_LG01H_LOB[9:8]	1:0	See description of '3D90h'.	
49h (3D92h)	REG3D92	7:0	Default : 0x78	Access : R/W
	IR_LG0_UPB[7:0]	7:0	The counter Upper Bound for Logic 0 width.	

IR Register (Bank = 3D)				
Index (Absolute)	Mnemonic	Bit	Description	
49h (3D93h)	REG3D93	7:0	Default : 0x05	Access : R/W
	-	7:3	Reserved.	
	IR_LG0_UPB[10:8]	2:0	See description of '3D92h'.	
4Ah (3D94h)	REG3D94	7:0	Default : 0x48	Access : R/W
	IR_LG0_LOB[7:0]	7:0	The counter Lower Bound for Logic 0 width.	
4Ah (3D95h)	REG3D95	7:0	Default : 0x03	Access : R/W
	-	7:3	Reserved.	
	IR_LG0_LOB[10:8]	2:0	See description of '3D94h'.	
4Bh (3D96h)	REG3D96	7:0	Default : 0xF0	Access : R/W
	IR_LG1_UPB[7:0]	7:0	The counter Upper Bound for Logic 1 width.	
4Bh (3D97h)	REG3D97	7:0	Default : 0x0A	Access : R/W
	-	7:4	Reserved.	
	IR_LG1_UPB[11:8]	3:0	See description of '3D96h'.	
4Ch (3D98h)	REG3D98	7:0	Default : 0x90	Access : R/W
	IR_LG1_LOB[7:0]	7:0	The counter Lower Bound for Logic 1 width.	
4Ch (3D99h)	REG3D99	7:0	Default : 0x06	Access : R/W
	-	7:4	Reserved.	
	IR_LG1_LOB[11:8]	3:0	See description of '3D98h'.	
4Dh (3D9Ah)	REG3D9A	7:0	Default : 0x00	Access : R/W
	IR_SEPR_UPB[7:0]	7:0	The counter Upper Bound for Separator Code width.	
4Dh (3D9Bh)	REG3D9B	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	IR_SEPR_UPB[11:8]	3:0	See description of '3D9Ah'.	
4Eh (3D9Ch)	REG3D9C	7:0	Default : 0x00	Access : R/W
	IR_SEPR_LOB[7:0]	7:0	The counter Lower Bound for Separator Code width.	
4Eh (3D9Dh)	REG3D9D	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	IR_SEPR_LOB[11:8]	3:0	See description of '3D9Ch'.	
4Fh (3D9Eh)	REG3D9E	7:0	Default : 0x8C	Access : R/W
	IR_TIMEOUT_CYC[7:0]	7:0	The counter value for IR Timeout Cycles. Timeout check will start when under below condition. 1. IR_TIMEOUT_CHK_EN=1. 2. Counter value > IR_TIMEOUT_CYC.	
4Fh	REG3D9F	7:0	Default : 0x00	Access : R/W

IR Register (Bank = 3D)				
Index (Absolute)	Mnemonic	Bit	Description	
(3D9Fh)	IR_TIMEOUT_CYC[15:8]	7:0	See description of '3D9Eh'.	
50h (3DA0h)	REG3DA0	7:0	Default : 0x30	Access : R/W
	IR_TIMEOUT_CLR_SW	7	IR Timeout Clear by SoftWare. 1: Enable. 0: Disable.	
	IR_TIMEOUT_CLR_SET[2:0]	6:4	IR Timeout Clear Set. 000: Timeout be clear at HDC check pass. 001: Timeout be clear at OFC check pass & Decode 0 state. 010: Timeout be clear at Customer Code check pass. 011: Timeout be clear at Key Data Code check pass. 100: S/w clear, need also to set "TIMEOUT_CLR_SW=1" . Recommend: Set 011 for NEC-like format.	
	-	3	Reserved.	
	IR_TIMEOUT_CYC[18:16]	2:0	See description of '3D9Eh'.	
50h (3DA1h)	REG3DA1	7:0	Default : 0x1F	Access : R/W
	IR_CCODE_BYTE	7	IR Customer Code Byte setting (full mode use only). 0: 1 byte customer code. 1: 2 bytes customer code. default: 1'b1 (for NEC format).	
	IR_CODE_BIT_NUM[6:0]	6:0	IR data code total bits. 00: 1 bit. 01: 2 bits. 10: 3 bits. ... 7f: 128 bits.	
51h (3DA2h)	REG3DA2	7:0	Default : 0x00	Access : R/W, WO
	RPT_FLAG_CLR_RAW	7	Interrupt Flag Clear for "IR repeat code flag in RAW mode" 1: Clear interrupt flag. 0: Not clear interrupt flag.	
	IR_RECOV_SHOT_CNT	6	Recover ir_shot_cnt as like sample rate is 1MHz. 0: Disable. 1: Enable, available at sample rate is 64kHz.	
	IR_SEPR_BIT[5:0]	5:0	IR Separator Bits setting (Only used for Mitsubishi format in full mode). The code data bit decode after this bit will into separator	

IR Register (Bank = 3D)				
Index (Absolute)	Mnemonic	Bit	Description	
			state when REG_IR_SEPR_EN=1 (3D81h[1]).	
51h (3DA3h)	REG3DA3	7:0	Default : 0x0F	Access : R/W, WO
	IR_FIFO_CLR	7	IR FIFO Clear Pulse Generation. 1: Generate 1T fifo clear pulse. 0: Normal operation. It is recommended to clear ir fifo when leaving power down mode.	
	IR_SW_FIFO_EN	6	SW FIFO mode enable (Decoder will help to save sw counter value and its pn_shot_flag into FIFO). 0: Disable. 1: Enable.	
	IR_SHOT_SEL[1:0]	5:4	The pshot/nshot selection for internal counter (Only used in S/W mode). 2'b01 : only pshot edge detect for counter. 2'b10 : only nshot edge detect for counter. 2'b00/11 : both pshot and nshot edge detect for counter.	
	IR_FIFO_FULL_EN	3	IR FIFO Full Enable (Used in Full/Raw mode). 0: Disable FIOF Full (data can be written over when FIFO is full). 1: Enable FIFO Full (data will be discarded when FIFO is full).	
	IR_FIFO_DEPTH[2:0]	2:0	FIFO Depth (for decoded IR code data or IR raw data, not for S/W mode counter data), totally support 16 bytes depth. 000: 9 bytes. 001: 10 bytes. 010: 11 bytes. 011: 12 bytes. 100: 13 bytes. 101: 14 bytes. 110: 15 bytes. 111: 16 bytes. Recommend: 16'bytes (3'b111).	
52h (3DA4h)	REG3DA4	7:0	Default : 0x00	Access : R/W
	IR_CCODE0[7:0]	7:0	IR Customer Code 0. (There are two customer codes could be set for decoding different remote controller. That is, we can decode 2 different remote controllers with same format.	

IR Register (Bank = 3D)				
Index (Absolute)	Mnemonic	Bit	Description	
			Also, each key have its flag to identify the key is come from which remote TX).	
52h (3DA5h)	REG3DA5	7:0	Default : 0x00	Access : R/W
	IR_CCODE0[15:8]	7:0	See description of '3DA4h'.	
53h (3DA6h)	REG3DA6	7:0	Default : 0x00	Access : R/W
	IR_GLHRM_NUM[7:0]	7:0	Glitch Removal Number for crystal based counter. The glitches will be removed whenever their cycle width below the GLHRM_NUM cycle.	
53h (3DA7h)	REG3DA7	7:0	Default : 0x00	Access : R/W
	IR_GLHRM_NUM_H[1:0]	7:6	Glitch Removal Number for crystal based counter. (extended).	
	IR_DECOMODE[1:0]	5:4	IR Decode Mode selection. 00/11 : Full decode mode (NEC and NEC-like format). 01: S/W mode (shot mode, output edge count value). 10: Raw mode (header decode only, output raw data).	
	IR_GLHRM_EN	3	Glitch Removal Enable.	
	IR_GLHRM_NUM[10:8]	2:0	See description of '3DA6h'.	
54h (3DA8h)	REG3DA8	7:0	Default : 0x00	Access : R/W
	IR_CKDIV_NUM[7:0]	7:0	The Divided Number of IR decoder input clock, the divided clock is for internal counter use. The input clock source of IR decoder is (XTAL/4) MHz. 8_h00: Divided by 1. 8_h01: Divided by 2. ... 8_hFF: Divided by 256. Recommend: 8_h02 for Xtal clock=14.318MHz. 8_h05 for Xtal clock=25.00MHz.	
54h (3DA9h)	REG3DA9	7:0	Default : 0x00	Access : RO
	IR_KEY_DATA[7:0]	7:0	IR Key Data output. (for Full/Raw mode data). After reading IR_KEY_DATA (3DA9h), you must set IR_FIFO_RD_PULSE=1 (3DB0h[0]) for internal fifo read pointer go to the next one.	
55h (3DAAh)	REG3DAA	7:0	Default : 0x00	Access : RO
	IR_SHOT_CNT[7:0]	7:0	IR Shot Count value output in s/w mode, the type of shot is select from IR_SHOT_SEL (3DA3h[5:4]).	

IR Register (Bank = 3D)				
Index (Absolute)	Mnemonic	Bit	Description	
55h (3DABh)	REG3DAB	7:0	Default : 0x00	Access : RO
	IR_SHOT_CNT[15:8]	7:0	See description of '3DAAh'.	
56h (3DACh)	REG3DAC	7:0	Default : 0x00	Access : RO
	-	7	Reserved.	
	IR_TX1_FLAG	6	IR remote controller TX1 send flag (This flag is only used for Full Decode Mode). 0: IR key data was sent from TX0. 1: IR key data was sent from TX1. PS: Before using this flag, you must set ir_ccode0_chk_en/ ir_ccode1_chk_en/ ir_ccode0/ ir_ccode1 for this feature.	
	IR_DATA_LOST_STATUS	5	IR data lost flag (Just for testing and system monitor purpose). This flag can only be used for those cases which decoded data been saved into FIFO. (1) full decode mode. (2) raw decode mode. (3) SW decode FIFO mode (pure "SW decode mode" cannot supported !).	
	IR_SHOT_P	4	IR shot type (pshot/nshot) in s/w mode. 0: Nshot occurs. 1: Pshot occurs.	
	-	3	Reserved.	
	IR_SHOT_CNT[18:16]	2:0	See description of '3DAAh'.	
56h (3DADh)	REG3DAD	7:0	Default : 0x00	Access : RO
	IR_RC_WKUP_FLAG	7	IR RC wakeup function flag.	
	IR_NEC_WKUP_FLAG	6	IR NEC wakeup function flag.	
	IR_INT_CRC_FLAG	5	IR CRC function interrupt flag.	
	IR_INT_FLAG	4	IR normal function interrupt flag.	
	IR_FIFO_FULL	3	IR FIFO Full Flag. 1: FIFO is full. 0: FIFO is not full yet.	
	IR_TIMEOUT_FLAG	2	IR Timeout Flag. 1: Timeout occurs. 0: Not timeout yet.	
	IR_FIFO_EMPTY	1	IR FIFO Empty flag for Full/Raw mode.	
	IR_RPT_FLAG	0	IR FIFO data Repeat Flag for Full mode.	

IR Register (Bank = 3D)				
Index (Absolute)	Mnemonic	Bit	Description	
57h (3DAEh)	REG3DAE	7:0	Default : 0x00	Access : RO
	IR_CRC_GOLDEN[7:0]	7:0	IR CRC Golden value, calculated by hardware while entering into power down mode. This value can be read just for reference, software don't need to fill any value. (Read-Only).	
57h (3DAFh)	REG3DAF	7:0	Default : 0x00	Access : RO
	IR_CRC_GOLDEN[15:8]	7:0	See description of '3DAEh'.	
58h (3DB0h)	REG3DB0	7:0	Default : 0x20	Access : R/W, WO
	IR_WKUP_KEY_SEL[3:0]	7:4	There are 2 kinds of meaning of this register for different decode modes: (1) For IR full decode mode (ir_decomode=00 or 11). IR key byte select for wakeup key compare (Just select one byte of the decoded data for compare). 0: Select byte 0 of IR signal as IR key (1st byte of IR data bytes). 1: Select byte 1 of IR signal as IR key (2nd byte of IR data bytes). 2: Select byte 2 of IR signal as IR key (3rd byte of IR data bytes). ..... F: Select byte 15 of IR signal as IR key (7th byte of IR data bytes). (2) For IR raw decode mode (ir_decomode=10). IR raw data select for wakeup compare. Decoder will compare the selected 4-bytes of the decoded raw data with the 4- byte wakeup key {ir_nec_comp_key4, ir_nec_comp_key3, ir_nec_comp_key2, ir_nec_comp_key1}. 0: Compare raw data [31:0] to the 4 -byte wakeup key. 1: Compare raw data [39:8] to the 4 -byte wakeup key. 2: Compare raw data [47:16] to the 4 -byte wakeup key. 3: Compare raw data [55:24] to the 4 -byte wakeup key. 4: Compare raw data [63:32] to the 4 -byte wakeup key. 5: Compare raw data [71:40] to the 4 -byte wakeup key. 6: Compare raw data [79:48] to the 4 -byte wakeup key. 7: Compare raw data [87:56] to the 4 -byte wakeup key. 8: Compare raw data [95:64] to the 4 -byte wakeup key. 9: Compare raw data [103:72] to the 4 -byte wakeup key. A: Compare raw data [111:80] to the 4 -byte wakeup key. B: Compare raw data [119:88] to the 4 -byte wakeup key.	

IR Register (Bank = 3D)				
Index (Absolute)	Mnemonic	Bit	Description	
			C~F: reserved.	
	IR_NEC_WKUP_FLAG_CLR	3	IR wakeup flag clear of NEC (or NEC-like) format. 1: Clear pulse generate. 0: No operation.	
	IR_FLAG_CLR	2	IR interrupt flag clear. 1: Clear pulse generate. 0: No operation.	
	IR_CRC_FLAG_CLR	1	IR crc interrupt flag clear. 1: Clear pulse generate. 0: No operation.	
	-	0	Reserved.	
58h (3DB1h)	REG3DB1	7:0	Default : 0x00	Access : WO
	-	7:1	Reserved.	
	IR_PPM_SW_RST	0	IR PPM (NEC) decoder Soft Reset. 0: Not reset. 1: Reset. ps: Write 1 clear (write-clear register, no need to write 0).	
59h (3DB2h)	REG3DB2	7:0	Default : 0xFF	Access : R/W
	IR_NEC_COMP_KEY1[7:0]	7:0	IR compare key1 for wakeup function of NEC (or NEC-like) format.	
59h (3DB3h)	REG3DB3	7:0	Default : 0xFF	Access : R/W
	IR_NEC_COMP_KEY2[7:0]	7:0	IR compare key2 for wakeup function of NEC (or NEC-like) format.	
5Ah (3DB4h)	REG3DB4	7:0	Default : 0x00	Access : R/W
	IR_ANYKEY_WKUP_EN	7	Enable for IR wakeup by any key (Customer code must matched) matched function. 0: Disable. 1: Enable.	
	IR_NEC_WKUP_EN	6	Enable for IR wakeup function of NEC (or NEC-like) format. 0: Disable. 1: Enable.	
	-	5	Reserved.	
	IR_4MAT_SEL[4:0]	4:0	IR data sequence format select for NEC-like (PPM modulation) formats. 0: Format not define, decided by code_bit assignment (ir_ccode_byte (reg_3D50h[15], ir_code_bit_num	

IR Register (Bank = 3D)				
Index (Absolute)	Mnemonic	Bit	Description	
			(reg_3D50h[14:8])). 1: C16D8D8P format (ex: NEC, Toshiba format). 2: C8D8 format (ex: Mitsubushi, Konka format). 3: C4D8C4D8P format (ex: RCA format). 4: C26D8D8P format. 5: C32D8D8P format. 6: C5D6C5D6P format. 7: C6D6C6D6P format. 8: D7C6 format (ex: Sony-D7C6). 9: D7C8 format (ex: Sony-D7C8). 10: D8C6 format (ex: Sony-D8C6). 11: D5_only format (ex: MV500). 12: S1C4D6 format (ex: IRT1250). 13: C5D6D4 format (ex: LR3715M). 14: R1T1C3D6 format (ex: M3004 LAB1-Carrier). 15~31: Reserved. Note: S = System Code. C = Customer Code Bits, (ex: C8= customer code 8bits). D = Data (Key) Code Bits, (ex: D8= data code 8bits). P = Format with Parity Check (ex: 3th byte and 4th byte of NEC format).	
5Bh (3DB6h)	REG3DB6	7:0	Default : 0xFF	Access : R/W
	IR_NEC_COMP_KEY3[7:0]	7:0	IR compare key3 for wakeup function of NEC (or NEC-like) format.	
5Bh (3DB7h)	REG3DB7	7:0	Default : 0xFF	Access : R/W
	IR_NEC_COMP_KEY4[7:0]	7:0	IR compare key4 for wakeup function of NEC (or NEC-like) format.	
5Ch (3DB8h)	REG3DB8	7:0	Default : 0xFF	Access : R/W
	IR_NEC_WKEY1_BIT_EN[7:0]	7:0	IR wakeup key1 bit enable for NEC (or NEC-like) format, for each bit. 0: Disable. 1: Enable.	
5Ch (3DB9h)	REG3DB9	7:0	Default : 0xFF	Access : R/W
	IR_NEC_WKEY2_BIT_EN[7:0]	7:0	IR wakeup key2 bit enable for NEC (or NEC-like) format, for each bit. 0: Disable. 1: Enable.	
5Dh	REG3DBA	7:0	Default : 0xFF	Access : R/W

IR Register (Bank = 3D)				
Index (Absolute)	Mnemonic	Bit	Description	
(3DBAh)	IR_NEC_WKEY3_BIT_EN[7:0]	7:0	IR wakeup key3 bit enable for NEC (or NEC-like) format, for each bit. 0: Disable. 1: Enable.	
5Dh (3DBBh)	REG3DBB	7:0	Default : 0xFF	Access : R/W
	IR_NEC_WKEY4_BIT_EN[7:0]	7:0	IR wakeup key4 bit enable for NEC (or NEC-like) format, for each bit. 0: Disable. 1: Enable.	
60h (3DC0h)	REG3DC0	7:0	Default : 0xFF	Access : R/W
	IR_CCODE1[7:0]	7:0	IR Customer Code 1. (There are two customer codes could be set for decoding different remote controllers. That is, we can decode 2 different remote controllers with same format. Also, each key have its flag to identify the key is come from which remote TX.).	
60h (3DC1h)	REG3DC1	7:0	Default : 0x00	Access : R/W
	IR_CCODE1[15:8]	7:0	See description of '3DC0h'.	
61h (3DC2h)	REG3DC2	7:0	Default : 0x00	Access : R/W
	RSVD_61H[7:2]	7:2	Reserved register for ECO.	
	PRE_GLITCH	1	Enable for fixing 3D-IR issue. 0: Disable. 1: Enable.	
	IR_CCODE1_CHK_EN	0	IR Customer Code 1 Check Enable. (There are two customer codes could be set for decoding different remote controllers.).	
61h (3DC3h)	REG3DC3	7:0	Default : 0x00	Access : R/W
	RSVD_61H[15:8]	7:0	See description of '3DC2h'.	
63h (3DC6h)	REG3DC6	7:0	Default : 0x00	Access : WO
	-	7:1	Reserved.	
	DATA_LOST_STS_CLR	0	IR data lost flag clear. 0: No action. 1: Clear (write clear pulse).	
64h (3DC8h)	REG3DC8	7:0	Default : 0x00	Access : RO
	IR_CRC_VAL[7:0]	7:0	Ir crc val.	

IR Register (Bank = 3D)				
Index (Absolute)	Mnemonic	Bit	Description	
64h (3DC9h)	REG3DC9	7:0	Default : 0x00	Access : RO
	IR_CRC_VAL[15:8]	7:0	See description of '3DC8h'.	

2.2. IR Register (Bank = 3D)

IR Register (Bank = 3D)				
Index (Absolute)	Mnemonic	Bit	Description	
58h (3DB0h)	REG3DB0	7:0	Default : 0x00	Access : WO
	-	7:1	Reserved.	
	IR_FIFO_RD_PULSE	0	IR FIFO Read Pulse. 1: Read. 0: Not read. Note: Need to set this bit to 1 after s/w read "IR_KEY_DATA" (3DA9h) (to let FIFO read pointer go to the next one).	