# SSD202D
# GPIO Module Description

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# 1. REGISTER DESCRIPTION

## 1.1. PM_GPIO Register (Bank = 0F)

| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| 00h (0F00h) | REG0F00 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_0 | 7 | GPIO_0's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_0 | 6 | GPIO_0's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_0 | 5 | GPIO_0's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_0 | 4 | GPIO_0's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_0 | 3 | GPIO_0's glitch remover enable. | |
| | GPIO_PM_IN_0 | 2 | GPIO_0's input. | |
| | GPIO_PM_OUT_0 | 1 | GPIO_0's output. | |
| | GPIO_PM_OEN_0 | 0 | GPIO_0's output enable. | |
| 00h (0F01h) | REG0F01 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_0 | 7 | GPIO_0's PAD PS. | |
| | GPIO_PM_PAD_PE_0 | 6 | GPIO_0's PAD PE. | |
| | GPIO_PM_PAD_DRV1_0 | 5 | GPIO_0's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_0 | 4 | GPIO_0's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_0 | 1 | GPIO_0's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_0 | 0 | GPIO_0's FIQ final status for edge wake-up source. | |
| 01h (0F02h) | REG0F02 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_1 | 7 | GPIO_1's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_1 | 6 | GPIO_1's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_1 | 5 | GPIO_1's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_1 | 4 | GPIO_1's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_1 | 3 | GPIO_1's glitch remover enable. | |
| | GPIO_PM_IN_1 | 2 | GPIO_1's input. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | GPIO_PM_OUT_1 | 1 | GPIO_1's output. | |
| | GPIO_PM_OEN_1 | 0 | GPIO_1's output enable. | |
| 01h (0F03h) | REG0F03 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_1 | 7 | GPIO_1's PAD PS. | |
| | GPIO_PM_PAD_PE_1 | 6 | GPIO_1's PAD PE. | |
| | GPIO_PM_PAD_DRV1_1 | 5 | GPIO_1's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_1 | 4 | GPIO_1's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_1 | 1 | GPIO_1's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_1 | 0 | GPIO_1's FIQ final status for edge wake-up source. | |
| 02h (0F04h) | REG0F04 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_2 | 7 | GPIO_2's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_2 | 6 | GPIO_2's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_2 | 5 | GPIO_2's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_2 | 4 | GPIO_2's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_2 | 3 | GPIO_2's glitch remover enable. | |
| | GPIO_PM_IN_2 | 2 | GPIO_2's input. | |
| | GPIO_PM_OUT_2 | 1 | GPIO_2's output. | |
| | GPIO_PM_OEN_2 | 0 | GPIO_2's output enable. | |
| 02h (0F05h) | REG0F05 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_2 | 7 | GPIO_2's PAD PS. | |
| | GPIO_PM_PAD_PE_2 | 6 | GPIO_2's PAD PE. | |
| | GPIO_PM_PAD_DRV1_2 | 5 | GPIO_2's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_2 | 4 | GPIO_2's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_2 | 1 | GPIO_2's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_2 | 0 | GPIO_2's FIQ final status for edge wake-up source. | |
| 03h (0F06h) | REG0F06 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_3 | 7 | GPIO_3's FIQ polarity for edge wake-up source. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | GPIO_PM_WK_FIQ_CLR_3 | 6 | GPIO_3's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_3 | 5 | GPIO_3's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_3 | 4 | GPIO_3's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_3 | 3 | GPIO_3's glitch remover enable. | |
| | GPIO_PM_IN_3 | 2 | GPIO_3's input. | |
| | GPIO_PM_OUT_3 | 1 | GPIO_3's output. | |
| | GPIO_PM_OEN_3 | 0 | GPIO_3's output enable. | |
| 03h (0F07h) | REG0F07 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_3 | 7 | GPIO_3's PAD PS. | |
| | GPIO_PM_PAD_PE_3 | 6 | GPIO_3's PAD PE. | |
| | GPIO_PM_PAD_DRV1_3 | 5 | GPIO_3's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_3 | 4 | GPIO_3's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_3 | 1 | GPIO_3's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_3 | 0 | GPIO_3's FIQ final status for edge wake-up source. | |
| 04h (0F08h) | REG0F08 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_4 | 7 | GPIO_4's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_4 | 6 | GPIO_4's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_4 | 5 | GPIO_4's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_4 | 4 | GPIO_4's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_4 | 3 | GPIO_4's glitch remover enable. | |
| | GPIO_PM_IN_4 | 2 | GPIO_4's input. | |
| | GPIO_PM_OUT_4 | 1 | GPIO_4's output. | |
| | GPIO_PM_OEN_4 | 0 | GPIO_4's output enable. | |
| 04h (0F09h) | REG0F09 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_4 | 7 | GPIO_4's PAD PS. | |
| | GPIO_PM_PAD_PE_4 | 6 | GPIO_4's PAD PE. | |
| | GPIO_PM_PAD_DRV1_4 | 5 | GPIO_4's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_4 | 4 | GPIO_4's PAD DRV0. | |
| | - | 3:2 | Reserved. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_4 | 1 | GPIO_4's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_4 | 0 | GPIO_4's FIQ final status for edge wake-up source. | |
| 05h (0F0Ah) | REG0F0A | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_5 | 7 | GPIO_5's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_5 | 6 | GPIO_5's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_5 | 5 | GPIO_5's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_5 | 4 | GPIO_5's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_5 | 3 | GPIO_5's glitch remover enable. | |
| | GPIO_PM_IN_5 | 2 | GPIO_5's input. | |
| | GPIO_PM_OUT_5 | 1 | GPIO_5's output. | |
| | GPIO_PM_OEN_5 | 0 | GPIO_5's output enable. | |
| 05h (0F0Bh) | REG0F0B | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_5 | 7 | GPIO_5's PAD PS. | |
| | GPIO_PM_PAD_PE_5 | 6 | GPIO_5's PAD PE. | |
| | GPIO_PM_PAD_DRV1_5 | 5 | GPIO_5's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_5 | 4 | GPIO_5's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_5 | 1 | GPIO_5's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_5 | 0 | GPIO_5's FIQ final status for edge wake-up source. | |
| 06h (0F0Ch) | REG0F0C | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_6 | 7 | GPIO_6's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_6 | 6 | GPIO_6's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_6 | 5 | GPIO_6's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_6 | 4 | GPIO_6's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_6 | 3 | GPIO_6's glitch remover enable. | |
| | GPIO_PM_IN_6 | 2 | GPIO_6's input. | |
| | GPIO_PM_OUT_6 | 1 | GPIO_6's output. | |
| | GPIO_PM_OEN_6 | 0 | GPIO_6's output enable. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| 06h (0F0Dh) | REG0F0D | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_6 | 7 | GPIO_6's PAD PS. | |
| | GPIO_PM_PAD_PE_6 | 6 | GPIO_6's PAD PE. | |
| | GPIO_PM_PAD_DRV1_6 | 5 | GPIO_6's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_6 | 4 | GPIO_6's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_6 | 1 | GPIO_6's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_6 | 0 | GPIO_6's FIQ final status for edge wake-up source. | |
| 07h (0F0Eh) | REG0F0E | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_7 | 7 | GPIO_7's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_7 | 6 | GPIO_7's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_7 | 5 | GPIO_7's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_7 | 4 | GPIO_7's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_7 | 3 | GPIO_7's glitch remover enable. | |
| | GPIO_PM_IN_7 | 2 | GPIO_7's input. | |
| | GPIO_PM_OUT_7 | 1 | GPIO_7's output. | |
| | GPIO_PM_OEN_7 | 0 | GPIO_7's output enable. | |
| 07h (0F0Fh) | REG0F0F | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_7 | 7 | GPIO_7's PAD PS. | |
| | GPIO_PM_PAD_PE_7 | 6 | GPIO_7's PAD PE. | |
| | GPIO_PM_PAD_DRV1_7 | 5 | GPIO_7's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_7 | 4 | GPIO_7's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_7 | 1 | GPIO_7's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_7 | 0 | GPIO_7's FIQ final status for edge wake-up source. | |
| 08h (0F10h) | REG0F10 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_8 | 7 | GPIO_8's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_8 | 6 | GPIO_8's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_8 | 5 | GPIO_8's FIQ force for edge wake-up source. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | GPIO_PM_WK_FIQ_MASK_8 | 4 | GPIO_8's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_8 | 3 | GPIO_8's glitch remover enable. | |
| | GPIO_PM_IN_8 | 2 | GPIO_8's input. | |
| | GPIO_PM_OUT_8 | 1 | GPIO_8's output. | |
| | GPIO_PM_OEN_8 | 0 | GPIO_8's output enable. | |
| 08h (0F11h) | REG0F11 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_8 | 7 | GPIO_8's PAD PS. | |
| | GPIO_PM_PAD_PE_8 | 6 | GPIO_8's PAD PE. | |
| | GPIO_PM_PAD_DRV1_8 | 5 | GPIO_8's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_8 | 4 | GPIO_8's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_8 | 1 | GPIO_8's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_8 | 0 | GPIO_8's FIQ final status for edge wake-up source. | |
| 09h (0F12h) | REG0F12 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_9 | 7 | GPIO_9's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_9 | 6 | GPIO_9's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_9 | 5 | GPIO_9's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_9 | 4 | GPIO_9's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_9 | 3 | GPIO_9's glitch remover enable. | |
| | GPIO_PM_IN_9 | 2 | GPIO_9's input. | |
| | GPIO_PM_OUT_9 | 1 | GPIO_9's output. | |
| | GPIO_PM_OEN_9 | 0 | GPIO_9's output enable. | |
| 09h (0F13h) | REG0F13 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_9 | 7 | GPIO_9's PAD PS. | |
| | GPIO_PM_PAD_PE_9 | 6 | GPIO_9's PAD PE. | |
| | GPIO_PM_PAD_DRV1_9 | 5 | GPIO_9's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_9 | 4 | GPIO_9's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_9 | 1 | GPIO_9's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_S | 0 | GPIO_9's FIQ final status for edge wake-up source. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | TATUS_9 | | | |
| 0Ah (0F14h) | REG0F14 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_10 | 7 | GPIO_10's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_10 | 6 | GPIO_10's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_10 | 5 | GPIO_10's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_10 | 4 | GPIO_10's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_10 | 3 | GPIO_10's glitch remover enable. | |
| | GPIO_PM_IN_10 | 2 | GPIO_10's input. | |
| | GPIO_PM_OUT_10 | 1 | GPIO_10's output. | |
| | GPIO_PM_OEN_10 | 0 | GPIO_10's output enable. | |
| 0Ah (0F15h) | REG0F15 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_10 | 7 | GPIO_10's PAD PS. | |
| | GPIO_PM_PAD_PE_10 | 6 | GPIO_10's PAD PE. | |
| | GPIO_PM_PAD_DRV1_10 | 5 | GPIO_10's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_10 | 4 | GPIO_10's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_10 | 1 | GPIO_10's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_10 | 0 | GPIO_10's FIQ final status for edge wake-up source. | |
| 0Bh (0F16h) | REG0F16 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_11 | 7 | GPIO_11's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_11 | 6 | GPIO_11's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_11 | 5 | GPIO_11's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_11 | 4 | GPIO_11's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_11 | 3 | GPIO_11's glitch remover enable. | |
| | GPIO_PM_IN_11 | 2 | GPIO_11's input. | |
| | GPIO_PM_OUT_11 | 1 | GPIO_11's output. | |
| | GPIO_PM_OEN_11 | 0 | GPIO_11's output enable. | |
| 0Bh (0F17h) | REG0F17 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_11 | 7 | GPIO_11's PAD PS. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | GPIO_PM_PAD_PE_11 | 6 | GPIO_11's PAD PE. | |
| | GPIO_PM_PAD_DRV1_11 | 5 | GPIO_11's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_11 | 4 | GPIO_11's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_11 | 1 | GPIO_11's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_11 | 0 | GPIO_11's FIQ final status for edge wake-up source. | |
| 0Ch (0F18h) | REG0F18 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_12 | 7 | GPIO_12's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_12 | 6 | GPIO_12's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_12 | 5 | GPIO_12's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_12 | 4 | GPIO_12's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_12 | 3 | GPIO_12's glitch remover enable. | |
| | GPIO_PM_IN_12 | 2 | GPIO_12's input. | |
| | GPIO_PM_OUT_12 | 1 | GPIO_12's output. | |
| | GPIO_PM_OEN_12 | 0 | GPIO_12's output enable. | |
| 0Ch (0F19h) | REG0F19 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_12 | 7 | GPIO_12's PAD PS. | |
| | GPIO_PM_PAD_PE_12 | 6 | GPIO_12's PAD PE. | |
| | GPIO_PM_PAD_DRV1_12 | 5 | GPIO_12's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_12 | 4 | GPIO_12's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_12 | 1 | GPIO_12's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_12 | 0 | GPIO_12's FIQ final status for edge wake-up source. | |
| 0Dh (0F1Ah) | REG0F1A | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_13 | 7 | GPIO_13's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_13 | 6 | GPIO_13's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_13 | 5 | GPIO_13's FIQ force for edge wake-up source. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | GPIO_PM_WK_FIQ_MASK_13 | 4 | GPIO_13's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_13 | 3 | GPIO_13's glitch remover enable. | |
| | GPIO_PM_IN_13 | 2 | GPIO_13's input. | |
| | GPIO_PM_OUT_13 | 1 | GPIO_13's output. | |
| | GPIO_PM_OEN_13 | 0 | GPIO_13's output enable. | |
| 0Dh (0F1Bh) | REG0F1B | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_13 | 7 | GPIO_13's PAD PS. | |
| | GPIO_PM_PAD_PE_13 | 6 | GPIO_13's PAD PE. | |
| | GPIO_PM_PAD_DRV1_13 | 5 | GPIO_13's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_13 | 4 | GPIO_13's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_13 | 1 | GPIO_13's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_13 | 0 | GPIO_13's FIQ final status for edge wake-up source. | |
| 0Eh (0F1Ch) | REG0F1C | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_14 | 7 | GPIO_14's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_14 | 6 | GPIO_14's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_14 | 5 | GPIO_14's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_14 | 4 | GPIO_14's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_14 | 3 | GPIO_14's glitch remover enable. | |
| | GPIO_PM_IN_14 | 2 | GPIO_14's input. | |
| | GPIO_PM_OUT_14 | 1 | GPIO_14's output. | |
| | GPIO_PM_OEN_14 | 0 | GPIO_14's output enable. | |
| 0Eh (0F1Dh) | REG0F1D | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_14 | 7 | GPIO_14's PAD PS. | |
| | GPIO_PM_PAD_PE_14 | 6 | GPIO_14's PAD PE. | |
| | GPIO_PM_PAD_DRV1_14 | 5 | GPIO_14's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_14 | 4 | GPIO_14's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_ST | 1 | GPIO_14's FIQ raw status for edge wake-up source. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | ATUS_14 | | | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_14 | 0 | GPIO_14's FIQ final status for edge wake-up source. | |
| 0Fh (0F1Eh) | REG0F1E | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_15 | 7 | GPIO_15's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_15 | 6 | GPIO_15's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_15 | 5 | GPIO_15's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_15 | 4 | GPIO_15's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_15 | 3 | GPIO_15's glitch remover enable. | |
| | GPIO_PM_IN_15 | 2 | GPIO_15's input. | |
| | GPIO_PM_OUT_15 | 1 | GPIO_15's output. | |
| | GPIO_PM_OEN_15 | 0 | GPIO_15's output enable. | |
| 0Fh (0F1Fh) | REG0F1F | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_15 | 7 | GPIO_15's PAD PS. | |
| | GPIO_PM_PAD_PE_15 | 6 | GPIO_15's PAD PE. | |
| | GPIO_PM_PAD_DRV1_15 | 5 | GPIO_15's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_15 | 4 | GPIO_15's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_15 | 1 | GPIO_15's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_15 | 0 | GPIO_15's FIQ final status for edge wake-up source. | |
| 10h (0F20h) | REG0F20 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_16 | 7 | GPIO_16's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_16 | 6 | GPIO_16's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_16 | 5 | GPIO_16's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_16 | 4 | GPIO_16's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_16 | 3 | GPIO_16's glitch remover enable. | |
| | GPIO_PM_IN_16 | 2 | GPIO_16's input. | |
| | GPIO_PM_OUT_16 | 1 | GPIO_16's output. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | GPIO_PM_OEN_16 | 0 | GPIO_16's output enable. | |
| 10h (0F21h) | REG0F21 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_16 | 7 | GPIO_16's PAD PS. | |
| | GPIO_PM_PAD_PE_16 | 6 | GPIO_16's PAD PE. | |
| | GPIO_PM_PAD_DRV1_16 | 5 | GPIO_16's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_16 | 4 | GPIO_16's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_16 | 1 | GPIO_16's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_16 | 0 | GPIO_16's FIQ final status for edge wake-up source. | |
| 11h (0F22h) | REG0F22 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_17 | 7 | GPIO_17's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_17 | 6 | GPIO_17's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_17 | 5 | GPIO_17's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_17 | 4 | GPIO_17's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_17 | 3 | GPIO_17's glitch remover enable. | |
| | GPIO_PM_IN_17 | 2 | GPIO_17's input. | |
| | GPIO_PM_OUT_17 | 1 | GPIO_17's output. | |
| | GPIO_PM_OEN_17 | 0 | GPIO_17's output enable. | |
| 11h (0F23h) | REG0F23 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_17 | 7 | GPIO_17's PAD PS. | |
| | GPIO_PM_PAD_PE_17 | 6 | GPIO_17's PAD PE. | |
| | GPIO_PM_PAD_DRV1_17 | 5 | GPIO_17's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_17 | 4 | GPIO_17's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_17 | 1 | GPIO_17's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_17 | 0 | GPIO_17's FIQ final status for edge wake-up source. | |
| 12h (0F24h) | REG0F24 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_18 | 7 | GPIO_18's FIQ polarity for edge wake-up source. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | GPIO_PM_WK_FIQ_CLR_18 | 6 | GPIO_18's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_18 | 5 | GPIO_18's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_18 | 4 | GPIO_18's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_18 | 3 | GPIO_18's glitch remover enable. | |
| | GPIO_PM_IN_18 | 2 | GPIO_18's input. | |
| | GPIO_PM_OUT_18 | 1 | GPIO_18's output. | |
| | GPIO_PM_OEN_18 | 0 | GPIO_18's output enable. | |
| 12h (0F25h) | REG0F25 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_18 | 7 | GPIO_18's PAD PS. | |
| | GPIO_PM_PAD_PE_18 | 6 | GPIO_18's PAD PE. | |
| | GPIO_PM_PAD_DRV1_18 | 5 | GPIO_18's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_18 | 4 | GPIO_18's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_18 | 1 | GPIO_18's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_18 | 0 | GPIO_18's FIQ final status for edge wake-up source. | |
| 13h (0F26h) | REG0F26 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_19 | 7 | GPIO_19's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_19 | 6 | GPIO_19's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_19 | 5 | GPIO_19's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_19 | 4 | GPIO_19's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_19 | 3 | GPIO_19's glitch remover enable. | |
| | GPIO_PM_IN_19 | 2 | GPIO_19's input. | |
| | GPIO_PM_OUT_19 | 1 | GPIO_19's output. | |
| | GPIO_PM_OEN_19 | 0 | GPIO_19's output enable. | |
| 13h (0F27h) | REG0F27 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_19 | 7 | GPIO_19's PAD PS. | |
| | GPIO_PM_PAD_PE_19 | 6 | GPIO_19's PAD PE. | |
| | GPIO_PM_PAD_DRV1_19 | 5 | GPIO_19's PAD DRV1. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | GPIO_PM_PAD_DRV0_19 | 4 | GPIO_19's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_19 | 1 | GPIO_19's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_19 | 0 | GPIO_19's FIQ final status for edge wake-up source. | |
| 14h (0F28h) | REG0F28 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_20 | 7 | GPIO_20's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_20 | 6 | GPIO_20's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_20 | 5 | GPIO_20's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_20 | 4 | GPIO_20's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_20 | 3 | GPIO_20's glitch remover enable. | |
| | GPIO_PM_IN_20 | 2 | GPIO_20's input. | |
| | GPIO_PM_OUT_20 | 1 | GPIO_20's output. | |
| | GPIO_PM_OEN_20 | 0 | GPIO_20's output enable (IR). | |
| 14h (0F29h) | REG0F29 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_20 | 7 | GPIO_20's PAD PS. | |
| | GPIO_PM_PAD_PE_20 | 6 | GPIO_20's PAD PE. | |
| | GPIO_PM_PAD_DRV1_20 | 5 | GPIO_20's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_20 | 4 | GPIO_20's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_20 | 1 | GPIO_20's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_20 | 0 | GPIO_20's FIQ final status for edge wake-up source. | |
| 15h (0F2Ah) | REG0F2A | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_21 | 7 | GPIO_21's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_21 | 6 | GPIO_21's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_21 | 5 | GPIO_21's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_21 | 4 | GPIO_21's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_21 | 3 | GPIO_21's glitch remover enable. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | GPIO_PM_IN_21 | 2 | GPIO_21's input. | |
| | GPIO_PM_OUT_21 | 1 | GPIO_21's output. | |
| | GPIO_PM_OEN_21 | 0 | GPIO_21's output enable (UART_RX). | |
| 15h (0F2Bh) | REG0F2B | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_21 | 7 | GPIO_21's PAD PS. | |
| | GPIO_PM_PAD_PE_21 | 6 | GPIO_21's PAD PE. | |
| | GPIO_PM_PAD_DRV1_21 | 5 | GPIO_21's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_21 | 4 | GPIO_21's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_21 | 1 | GPIO_21's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_21 | 0 | GPIO_21's FIQ final status for edge wake-up source. | |
| 16h (0F2Ch) | REG0F2C | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_22 | 7 | GPIO_22's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_22 | 6 | GPIO_22's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_22 | 5 | GPIO_22's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_22 | 4 | GPIO_22's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_22 | 3 | GPIO_22's glitch remover enable. | |
| | GPIO_PM_IN_22 | 2 | GPIO_22's input. | |
| | GPIO_PM_OUT_22 | 1 | GPIO_22's output. | |
| | GPIO_PM_OEN_22 | 0 | GPIO_22's output enable (CEC). | |
| 16h (0F2Dh) | REG0F2D | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_22 | 7 | GPIO_22's PAD PS. | |
| | GPIO_PM_PAD_PE_22 | 6 | GPIO_22's PAD PE. | |
| | GPIO_PM_PAD_DRV1_22 | 5 | GPIO_22's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_22 | 4 | GPIO_22's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_22 | 1 | GPIO_22's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_22 | 0 | GPIO_22's FIQ final status for edge wake-up source. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| 17h (0F2Eh) | REG0F2E | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_23 | 7 | GPIO_23's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_23 | 6 | GPIO_23's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_23 | 5 | GPIO_23's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_23 | 4 | GPIO_23's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_23 | 3 | GPIO_23's glitch remover enable. | |
| | GPIO_PM_IN_23 | 2 | GPIO_23's input. | |
| | GPIO_PM_OUT_23 | 1 | GPIO_23's output. | |
| | GPIO_PM_OEN_23 | 0 | GPIO_23's output enable (un-connect). | |
| 17h (0F2Fh) | REG0F2F | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_23 | 7 | GPIO_23's PAD PS. | |
| | GPIO_PM_PAD_PE_23 | 6 | GPIO_23's PAD PE. | |
| | GPIO_PM_PAD_DRV1_23 | 5 | GPIO_23's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_23 | 4 | GPIO_23's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_23 | 1 | GPIO_23's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_23 | 0 | GPIO_23's FIQ final status for edge wake-up source. | |
| 18h (0F30h) | REG0F30 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_24 | 7 | GPIO_24's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_24 | 6 | GPIO_24's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_24 | 5 | GPIO_24's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_24 | 4 | GPIO_24's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_24 | 3 | GPIO_24's glitch remover enable. | |
| | GPIO_PM_IN_24 | 2 | GPIO_24's input. | |
| | GPIO_PM_OUT_24 | 1 | GPIO_24's output. | |
| | GPIO_PM_OEN_24 | 0 | GPIO_24's output enable (SPI_CZ). | |
| 18h (0F31h) | REG0F31 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_24 | 7 | GPIO_24's PAD PS. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | GPIO_PM_PAD_PE_24 | 6 | GPIO_24's PAD PE. | |
| | GPIO_PM_PAD_DRV1_24 | 5 | GPIO_24's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_24 | 4 | GPIO_24's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_24 | 1 | GPIO_24's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_24 | 0 | GPIO_24's FIQ final status for edge wake-up source. | |
| 19h (0F32h) | REG0F32 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_25 | 7 | GPIO_25's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_25 | 6 | GPIO_25's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_25 | 5 | GPIO_25's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_25 | 4 | GPIO_25's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_25 | 3 | GPIO_25's glitch remover enable. | |
| | GPIO_PM_IN_25 | 2 | GPIO_25's input. | |
| | GPIO_PM_OUT_25 | 1 | GPIO_25's output. | |
| | GPIO_PM_OEN_25 | 0 | GPIO_25's output enable (SPI_CK). | |
| 19h (0F33h) | REG0F33 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_25 | 7 | GPIO_25's PAD PS. | |
| | GPIO_PM_PAD_PE_25 | 6 | GPIO_25's PAD PE. | |
| | GPIO_PM_PAD_DRV1_25 | 5 | GPIO_25's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_25 | 4 | GPIO_25's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_25 | 1 | GPIO_25's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_25 | 0 | GPIO_25's FIQ final status for edge wake-up source. | |
| 1Ah (0F34h) | REG0F34 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_26 | 7 | GPIO_26's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_26 | 6 | GPIO_26's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_26 | 5 | GPIO_26's FIQ force for edge wake-up source. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | GPIO_PM_WK_FIQ_MASK_26 | 4 | GPIO_26's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_26 | 3 | GPIO_26's glitch remover enable. | |
| | GPIO_PM_IN_26 | 2 | GPIO_26's input. | |
| | GPIO_PM_OUT_26 | 1 | GPIO_26's output. | |
| | GPIO_PM_OEN_26 | 0 | GPIO_26's output enable (SPI_DI). | |
| 1Ah (0F35h) | REG0F35 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_26 | 7 | GPIO_26's PAD PS. | |
| | GPIO_PM_PAD_PE_26 | 6 | GPIO_26's PAD PE. | |
| | GPIO_PM_PAD_DRV1_26 | 5 | GPIO_26's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_26 | 4 | GPIO_26's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_26 | 1 | GPIO_26's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_26 | 0 | GPIO_26's FIQ final status for edge wake-up source. | |
| 1Bh (0F36h) | REG0F36 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_27 | 7 | GPIO_27's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_27 | 6 | GPIO_27's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_27 | 5 | GPIO_27's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_27 | 4 | GPIO_27's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_27 | 3 | GPIO_27's glitch remover enable. | |
| | GPIO_PM_IN_27 | 2 | GPIO_27's input. | |
| | GPIO_PM_OUT_27 | 1 | GPIO_27's output. | |
| | GPIO_PM_OEN_27 | 0 | GPIO_27's output enable (SPI_DO). | |
| 1Bh (0F37h) | REG0F37 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_27 | 7 | GPIO_27's PAD PS. | |
| | GPIO_PM_PAD_PE_27 | 6 | GPIO_27's PAD PE. | |
| | GPIO_PM_PAD_DRV1_27 | 5 | GPIO_27's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_27 | 4 | GPIO_27's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_ST | 1 | GPIO_27's FIQ raw status for edge wake-up source. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | ATUS_27 | | | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_27 | 0 | GPIO_27's FIQ final status for edge wake-up source. | |
| 1Ch (0F38h) | REG0F38 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_28 | 7 | GPIO_28's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_28 | 6 | GPIO_28's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_28 | 5 | GPIO_28's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_28 | 4 | GPIO_28's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_28 | 3 | GPIO_28's glitch remover enable. | |
| | GPIO_PM_IN_28 | 2 | GPIO_28's input. | |
| | GPIO_PM_OUT_28 | 1 | GPIO_28's output. | |
| | GPIO_PM_OEN_28 | 0 | GPIO_28's output enable. | |
| 1Ch (0F39h) | REG0F39 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_28 | 7 | GPIO_28's PAD PS. | |
| | GPIO_PM_PAD_PE_28 | 6 | GPIO_28's PAD PE. | |
| | GPIO_PM_PAD_DRV1_28 | 5 | GPIO_28's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_28 | 4 | GPIO_28's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_28 | 1 | GPIO_28's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_28 | 0 | GPIO_28's FIQ final status for edge wake-up source. | |
| 1Dh (0F3Ah) | REG0F3A | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_29 | 7 | GPIO_29's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_29 | 6 | GPIO_29's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_29 | 5 | GPIO_29's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_29 | 4 | GPIO_29's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_29 | 3 | GPIO_29's glitch remover enable. | |
| | GPIO_PM_IN_29 | 2 | GPIO_29's input. | |
| | GPIO_PM_OUT_29 | 1 | GPIO_29's output. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | GPIO_PM_OEN_29 | 0 | GPIO_29's output enable. | |
| 1Dh (0F3Bh) | REG0F3B | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_29 | 7 | GPIO_29's PAD PS. | |
| | GPIO_PM_PAD_PE_29 | 6 | GPIO_29's PAD PE. | |
| | GPIO_PM_PAD_DRV1_29 | 5 | GPIO_29's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_29 | 4 | GPIO_29's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_29 | 1 | GPIO_29's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_29 | 0 | GPIO_29's FIQ final status for edge wake-up source. | |
| 1Eh (0F3Ch) | REG0F3C | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_30 | 7 | GPIO_30's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_30 | 6 | GPIO_30's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_30 | 5 | GPIO_30's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_30 | 4 | GPIO_30's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_30 | 3 | GPIO_30's glitch remover enable. | |
| | GPIO_PM_IN_30 | 2 | GPIO_30's input. | |
| | GPIO_PM_OUT_30 | 1 | GPIO_30's output. | |
| | GPIO_PM_OEN_30 | 0 | GPIO_30's output enable. | |
| 1Eh (0F3Dh) | REG0F3D | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_30 | 7 | GPIO_30's PAD PS. | |
| | GPIO_PM_PAD_PE_30 | 6 | GPIO_30's PAD PE. | |
| | GPIO_PM_PAD_DRV1_30 | 5 | GPIO_30's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_30 | 4 | GPIO_30's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_30 | 1 | GPIO_30's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_30 | 0 | GPIO_30's FIQ final status for edge wake-up source. | |
| 1Fh (0F3Eh) | REG0F3E | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_31 | 7 | GPIO_31's FIQ polarity for edge wake-up source. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | GPIO_PM_WK_FIQ_CLR_31 | 6 | GPIO_31's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_31 | 5 | GPIO_31's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_31 | 4 | GPIO_31's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_31 | 3 | GPIO_31's glitch remover enable. | |
| | GPIO_PM_IN_31 | 2 | GPIO_31's input. | |
| | GPIO_PM_OUT_31 | 1 | GPIO_31's output. | |
| | GPIO_PM_OEN_31 | 0 | GPIO_31's output enable. | |
| 1Fh (0F3Fh) | REG0F3F | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_31 | 7 | GPIO_31's PAD PS. | |
| | GPIO_PM_PAD_PE_31 | 6 | GPIO_31's PAD PE. | |
| | GPIO_PM_PAD_DRV1_31 | 5 | GPIO_31's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_31 | 4 | GPIO_31's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_31 | 1 | GPIO_31's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_31 | 0 | GPIO_31's FIQ final status for edge wake-up source. | |
| 20h (0F40h) | REG0F40 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_32 | 7 | GPIO_32's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_32 | 6 | GPIO_32's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_32 | 5 | GPIO_32's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_32 | 4 | GPIO_32's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_32 | 3 | GPIO_32's glitch remover enable. | |
| | GPIO_PM_IN_32 | 2 | GPIO_32's input. | |
| | GPIO_PM_OUT_32 | 1 | GPIO_32's output. | |
| | GPIO_PM_OEN_32 | 0 | GPIO_32's output enable. | |
| 20h (0F41h) | REG0F41 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_32 | 7 | GPIO_32's PAD PS. | |
| | GPIO_PM_PAD_PE_32 | 6 | GPIO_32's PAD PE. | |
| | GPIO_PM_PAD_DRV1_32 | 5 | GPIO_32's PAD DRV1. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | GPIO_PM_PAD_DRV0_32 | 4 | GPIO_32's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_32 | 1 | GPIO_32's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_32 | 0 | GPIO_32's FIQ final status for edge wake-up source. | |
| 21h (0F42h) | REG0F42 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_33 | 7 | GPIO_33's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_33 | 6 | GPIO_33's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_33 | 5 | GPIO_33's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_33 | 4 | GPIO_33's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_33 | 3 | GPIO_33's glitch remover enable. | |
| | GPIO_PM_IN_33 | 2 | GPIO_33's input. | |
| | GPIO_PM_OUT_33 | 1 | GPIO_33's output. | |
| | GPIO_PM_OEN_33 | 0 | GPIO_33's output enable. | |
| 21h (0F43h) | REG0F43 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_33 | 7 | GPIO_33's PAD PS. | |
| | GPIO_PM_PAD_PE_33 | 6 | GPIO_33's PAD PE. | |
| | GPIO_PM_PAD_DRV1_33 | 5 | GPIO_33's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_33 | 4 | GPIO_33's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_33 | 1 | GPIO_33's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_33 | 0 | GPIO_33's FIQ final status for edge wake-up source. | |
| 22h (0F44h) | REG0F44 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_34 | 7 | GPIO_34's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_34 | 6 | GPIO_34's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_34 | 5 | GPIO_34's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_34 | 4 | GPIO_34's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_34 | 3 | GPIO_34's glitch remover enable. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | GPIO_PM_IN_34 | 2 | GPIO_34's input. | |
| | GPIO_PM_OUT_34 | 1 | GPIO_34's output. | |
| | GPIO_PM_OEN_34 | 0 | GPIO_34's output enable. | |
| 22h (0F45h) | REG0F45 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_34 | 7 | GPIO_34's PAD PS. | |
| | GPIO_PM_PAD_PE_34 | 6 | GPIO_34's PAD PE. | |
| | GPIO_PM_PAD_DRV1_34 | 5 | GPIO_34's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_34 | 4 | GPIO_34's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_34 | 1 | GPIO_34's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_34 | 0 | GPIO_34's FIQ final status for edge wake-up source. | |
| 23h (0F46h) | REG0F46 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_35 | 7 | GPIO_35's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_35 | 6 | GPIO_35's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_35 | 5 | GPIO_35's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_35 | 4 | GPIO_35's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_35 | 3 | GPIO_35's glitch remover enable. | |
| | GPIO_PM_IN_35 | 2 | GPIO_35's input. | |
| | GPIO_PM_OUT_35 | 1 | GPIO_35's output. | |
| | GPIO_PM_OEN_35 | 0 | GPIO_35's output enable. | |
| 23h (0F47h) | REG0F47 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_35 | 7 | GPIO_35's PAD PS. | |
| | GPIO_PM_PAD_PE_35 | 6 | GPIO_35's PAD PE. | |
| | GPIO_PM_PAD_DRV1_35 | 5 | GPIO_35's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_35 | 4 | GPIO_35's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_35 | 1 | GPIO_35's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_35 | 0 | GPIO_35's FIQ final status for edge wake-up source. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| 24h (0F48h) | REG0F48 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_36 | 7 | GPIO_36's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_36 | 6 | GPIO_36's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_36 | 5 | GPIO_36's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_36 | 4 | GPIO_36's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_36 | 3 | GPIO_36's glitch remover enable. | |
| | GPIO_PM_IN_36 | 2 | GPIO_36's input. | |
| | GPIO_PM_OUT_36 | 1 | GPIO_36's output. | |
| | GPIO_PM_OEN_36 | 0 | GPIO_36's output enable. | |
| 24h (0F49h) | REG0F49 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_36 | 7 | GPIO_36's PAD PS. | |
| | GPIO_PM_PAD_PE_36 | 6 | GPIO_36's PAD PE. | |
| | GPIO_PM_PAD_DRV1_36 | 5 | GPIO_36's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_36 | 4 | GPIO_36's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_36 | 1 | GPIO_36's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_36 | 0 | GPIO_36's FIQ final status for edge wake-up source. | |
| 25h (0F4Ah) | REG0F4A | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_37 | 7 | GPIO_37's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_37 | 6 | GPIO_37's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_37 | 5 | GPIO_37's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_37 | 4 | GPIO_37's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_37 | 3 | GPIO_37's glitch remover enable. | |
| | GPIO_PM_IN_37 | 2 | GPIO_37's input. | |
| | GPIO_PM_OUT_37 | 1 | GPIO_37's output. | |
| | GPIO_PM_OEN_37 | 0 | GPIO_37's output enable. | |
| 25h (0F4Bh) | REG0F4B | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_37 | 7 | GPIO_37's PAD PS. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | GPIO_PM_PAD_PE_37 | 6 | GPIO_37's PAD PE. | |
| | GPIO_PM_PAD_DRV1_37 | 5 | GPIO_37's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_37 | 4 | GPIO_37's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_37 | 1 | GPIO_37's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_37 | 0 | GPIO_37's FIQ final status for edge wake-up source. | |
| 26h (0F4Ch) | REG0F4C | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_38 | 7 | GPIO_38's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_38 | 6 | GPIO_38's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_38 | 5 | GPIO_38's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_38 | 4 | GPIO_38's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_38 | 3 | GPIO_38's glitch remover enable. | |
| | GPIO_PM_IN_38 | 2 | GPIO_38's input. | |
| | GPIO_PM_OUT_38 | 1 | GPIO_38's output. | |
| | GPIO_PM_OEN_38 | 0 | GPIO_38's output enable. | |
| 26h (0F4Dh) | REG0F4D | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_38 | 7 | GPIO_38's PAD PS. | |
| | GPIO_PM_PAD_PE_38 | 6 | GPIO_38's PAD PE. | |
| | GPIO_PM_PAD_DRV1_38 | 5 | GPIO_38's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_38 | 4 | GPIO_38's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_38 | 1 | GPIO_38's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_38 | 0 | GPIO_38's FIQ final status for edge wake-up source. | |
| 27h (0F4Eh) | REG0F4E | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_39 | 7 | GPIO_39's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_39 | 6 | GPIO_39's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_39 | 5 | GPIO_39's FIQ force for edge wake-up source. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | GPIO_PM_WK_FIQ_MASK_39 | 4 | GPIO_39's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_39 | 3 | GPIO_39's glitch remover enable. | |
| | GPIO_PM_IN_39 | 2 | GPIO_39's input. | |
| | GPIO_PM_OUT_39 | 1 | GPIO_39's output. | |
| | GPIO_PM_OEN_39 | 0 | GPIO_39's output enable (PAD_GT0_MDC). | |
| 27h (0F4Fh) | REG0F4F | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_39 | 7 | GPIO_39's PAD PS. | |
| | GPIO_PM_PAD_PE_39 | 6 | GPIO_39's PAD PE. | |
| | GPIO_PM_PAD_DRV1_39 | 5 | GPIO_39's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_39 | 4 | GPIO_39's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_39 | 1 | GPIO_39's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_39 | 0 | GPIO_39's FIQ final status for edge wake-up source. | |
| 28h (0F50h) | REG0F50 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_40 | 7 | GPIO_40's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_40 | 6 | GPIO_40's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_40 | 5 | GPIO_40's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_40 | 4 | GPIO_40's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_40 | 3 | GPIO_40's glitch remover enable. | |
| | GPIO_PM_IN_40 | 2 | GPIO_40's input. | |
| | GPIO_PM_OUT_40 | 1 | GPIO_40's output. | |
| | GPIO_PM_OEN_40 | 0 | GPIO_40's output enable (PAD_GT0_MDIO). | |
| 28h (0F51h) | REG0F51 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_40 | 7 | GPIO_40's PAD PS. | |
| | GPIO_PM_PAD_PE_40 | 6 | GPIO_40's PAD PE. | |
| | GPIO_PM_PAD_DRV1_40 | 5 | GPIO_40's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_40 | 4 | GPIO_40's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_ST | 1 | GPIO_40's FIQ raw status for edge wake-up source. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
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| Index (Absolute) | Mnemonic | Bit | Description | |
| | ATUS_40 | | | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_40 | 0 | GPIO_40's FIQ final status for edge wake-up source. | |
| 29h (0F52h) | REG0F52 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_41 | 7 | GPIO_41's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_41 | 6 | GPIO_41's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_41 | 5 | GPIO_41's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_41 | 4 | GPIO_41's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_41 | 3 | GPIO_41's glitch remover enable. | |
| | GPIO_PM_IN_41 | 2 | GPIO_41's input. | |
| | GPIO_PM_OUT_41 | 1 | GPIO_41's output. | |
| | GPIO_PM_OEN_41 | 0 | GPIO_41's output enable (PAD_GT0_RX_CLK). | |
| 29h (0F53h) | REG0F53 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_41 | 7 | GPIO_41's PAD PS. | |
| | GPIO_PM_PAD_PE_41 | 6 | GPIO_41's PAD PE. | |
| | GPIO_PM_PAD_DRV1_41 | 5 | GPIO_41's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_41 | 4 | GPIO_41's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_41 | 1 | GPIO_41's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_41 | 0 | GPIO_41's FIQ final status for edge wake-up source. | |
| 2Ah (0F54h) | REG0F54 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_42 | 7 | GPIO_42's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_42 | 6 | GPIO_42's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_42 | 5 | GPIO_42's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_42 | 4 | GPIO_42's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_42 | 3 | GPIO_42's glitch remover enable. | |
| | GPIO_PM_IN_42 | 2 | GPIO_42's input. | |
| | GPIO_PM_OUT_42 | 1 | GPIO_42's output. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | GPIO_PM_OEN_42 | 0 | GPIO_42's output enable (PAD_GT0_RX_CTL). | |
| 2Ah (0F55h) | REG0F55 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_42 | 7 | GPIO_42's PAD PS. | |
| | GPIO_PM_PAD_PE_42 | 6 | GPIO_42's PAD PE. | |
| | GPIO_PM_PAD_DRV1_42 | 5 | GPIO_42's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_42 | 4 | GPIO_42's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_42 | 1 | GPIO_42's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_42 | 0 | GPIO_42's FIQ final status for edge wake-up source. | |
| 2Bh (0F56h) | REG0F56 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_43 | 7 | GPIO_43's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_43 | 6 | GPIO_43's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_43 | 5 | GPIO_43's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_43 | 4 | GPIO_43's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_43 | 3 | GPIO_43's glitch remover enable. | |
| | GPIO_PM_IN_43 | 2 | GPIO_43's input. | |
| | GPIO_PM_OUT_43 | 1 | GPIO_43's output. | |
| | GPIO_PM_OEN_43 | 0 | GPIO_43's output enable (PAD_GT0_RX_D0). | |
| 2Bh (0F57h) | REG0F57 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_43 | 7 | GPIO_43's PAD PS. | |
| | GPIO_PM_PAD_PE_43 | 6 | GPIO_43's PAD PE. | |
| | GPIO_PM_PAD_DRV1_43 | 5 | GPIO_43's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_43 | 4 | GPIO_43's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_43 | 1 | GPIO_43's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_43 | 0 | GPIO_43's FIQ final status for edge wake-up source. | |
| 2Ch (0F58h) | REG0F58 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_44 | 7 | GPIO_44's FIQ polarity for edge wake-up source. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | GPIO_PM_WK_FIQ_CLR_44 | 6 | GPIO_44's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_44 | 5 | GPIO_44's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_44 | 4 | GPIO_44's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_44 | 3 | GPIO_44's glitch remover enable. | |
| | GPIO_PM_IN_44 | 2 | GPIO_44's input. | |
| | GPIO_PM_OUT_44 | 1 | GPIO_44's output. | |
| | GPIO_PM_OEN_44 | 0 | GPIO_44's output enable (PAD_GT0_RX_D1). | |
| 2Ch (0F59h) | REG0F59 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_44 | 7 | GPIO_44's PAD PS. | |
| | GPIO_PM_PAD_PE_44 | 6 | GPIO_44's PAD PE. | |
| | GPIO_PM_PAD_DRV1_44 | 5 | GPIO_44's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_44 | 4 | GPIO_44's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_44 | 1 | GPIO_44's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_44 | 0 | GPIO_44's FIQ final status for edge wake-up source. | |
| 2Dh (0F5Ah) | REG0F5A | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_45 | 7 | GPIO_45's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_45 | 6 | GPIO_45's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_45 | 5 | GPIO_45's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_45 | 4 | GPIO_45's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_45 | 3 | GPIO_45's glitch remover enable. | |
| | GPIO_PM_IN_45 | 2 | GPIO_45's input. | |
| | GPIO_PM_OUT_45 | 1 | GPIO_45's output. | |
| | GPIO_PM_OEN_45 | 0 | GPIO_45's output enable (PAD_GT0_RX_D2). | |
| 2Dh (0F5Bh) | REG0F5B | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_45 | 7 | GPIO_45's PAD PS. | |
| | GPIO_PM_PAD_PE_45 | 6 | GPIO_45's PAD PE. | |
| | GPIO_PM_PAD_DRV1_45 | 5 | GPIO_45's PAD DRV1. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | GPIO_PM_PAD_DRV0_45 | 4 | GPIO_45's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_45 | 1 | GPIO_45's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_45 | 0 | GPIO_45's FIQ final status for edge wake-up source. | |
| 2Eh (0F5Ch) | REG0F5C | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_46 | 7 | GPIO_46's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_46 | 6 | GPIO_46's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_46 | 5 | GPIO_46's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_46 | 4 | GPIO_46's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_46 | 3 | GPIO_46's glitch remover enable. | |
| | GPIO_PM_IN_46 | 2 | GPIO_46's input. | |
| | GPIO_PM_OUT_46 | 1 | GPIO_46's output. | |
| | GPIO_PM_OEN_46 | 0 | GPIO_46's output enable (PAD_GT0_RX_D3). | |
| 2Eh (0F5Dh) | REG0F5D | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_46 | 7 | GPIO_46's PAD PS. | |
| | GPIO_PM_PAD_PE_46 | 6 | GPIO_46's PAD PE. | |
| | GPIO_PM_PAD_DRV1_46 | 5 | GPIO_46's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_46 | 4 | GPIO_46's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_46 | 1 | GPIO_46's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_46 | 0 | GPIO_46's FIQ final status for edge wake-up source. | |
| 2Fh (0F5Eh) | REG0F5E | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_47 | 7 | GPIO_47's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_47 | 6 | GPIO_47's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_47 | 5 | GPIO_47's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_47 | 4 | GPIO_47's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_47 | 3 | GPIO_47's glitch remover enable. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | GPIO_PM_IN_47 | 2 | GPIO_47's input. | |
| | GPIO_PM_OUT_47 | 1 | GPIO_47's output. | |
| | GPIO_PM_OEN_47 | 0 | GPIO_47's output enable (PAD_GT0_TX_CLK). | |
| 2Fh (0F5Fh) | REG0F5F | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_47 | 7 | GPIO_47's PAD PS. | |
| | GPIO_PM_PAD_PE_47 | 6 | GPIO_47's PAD PE. | |
| | GPIO_PM_PAD_DRV1_47 | 5 | GPIO_47's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_47 | 4 | GPIO_47's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_47 | 1 | GPIO_47's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_47 | 0 | GPIO_47's FIQ final status for edge wake-up source. | |
| 30h (0F60h) | REG0F60 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_48 | 7 | GPIO_48's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_48 | 6 | GPIO_48's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_48 | 5 | GPIO_48's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_48 | 4 | GPIO_48's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_48 | 3 | GPIO_48's glitch remover enable. | |
| | GPIO_PM_IN_48 | 2 | GPIO_48's input. | |
| | GPIO_PM_OUT_48 | 1 | GPIO_48's output. | |
| | GPIO_PM_OEN_48 | 0 | GPIO_48's output enable (PAD_GT0_TX_CTL). | |
| 30h (0F61h) | REG0F61 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_48 | 7 | GPIO_48's PAD PS. | |
| | GPIO_PM_PAD_PE_48 | 6 | GPIO_48's PAD PE. | |
| | GPIO_PM_PAD_DRV1_48 | 5 | GPIO_48's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_48 | 4 | GPIO_48's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_48 | 1 | GPIO_48's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_48 | 0 | GPIO_48's FIQ final status for edge wake-up source. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| 31h (0F62h) | REG0F62 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_49 | 7 | GPIO_49's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_49 | 6 | GPIO_49's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_49 | 5 | GPIO_49's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_49 | 4 | GPIO_49's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_49 | 3 | GPIO_49's glitch remover enable. | |
| | GPIO_PM_IN_49 | 2 | GPIO_49's input. | |
| | GPIO_PM_OUT_49 | 1 | GPIO_49's output. | |
| | GPIO_PM_OEN_49 | 0 | GPIO_49's output enable (PAD_GT0_TX_D0). | |
| 31h (0F63h) | REG0F63 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_49 | 7 | GPIO_49's PAD PS. | |
| | GPIO_PM_PAD_PE_49 | 6 | GPIO_49's PAD PE. | |
| | GPIO_PM_PAD_DRV1_49 | 5 | GPIO_49's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_49 | 4 | GPIO_49's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_49 | 1 | GPIO_49's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_49 | 0 | GPIO_49's FIQ final status for edge wake-up source. | |
| 32h (0F64h) | REG0F64 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_50 | 7 | GPIO_50's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_50 | 6 | GPIO_50's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_50 | 5 | GPIO_50's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_50 | 4 | GPIO_50's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_50 | 3 | GPIO_50's glitch remover enable. | |
| | GPIO_PM_IN_50 | 2 | GPIO_50's input. | |
| | GPIO_PM_OUT_50 | 1 | GPIO_50's output. | |
| | GPIO_PM_OEN_50 | 0 | GPIO_50's output enable (PAD_GT0_TX_D1). | |
| 32h (0F65h) | REG0F65 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_50 | 7 | GPIO_50's PAD PS. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | GPIO_PM_PAD_PE_50 | 6 | GPIO_50's PAD PE. | |
| | GPIO_PM_PAD_DRV1_50 | 5 | GPIO_50's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_50 | 4 | GPIO_50's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_50 | 1 | GPIO_50's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_50 | 0 | GPIO_50's FIQ final status for edge wake-up source. | |
| 33h (0F66h) | REG0F66 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_51 | 7 | GPIO_51's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_51 | 6 | GPIO_51's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_51 | 5 | GPIO_51's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_51 | 4 | GPIO_51's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_51 | 3 | GPIO_51's glitch remover enable. | |
| | GPIO_PM_IN_51 | 2 | GPIO_51's input. | |
| | GPIO_PM_OUT_51 | 1 | GPIO_51's output. | |
| | GPIO_PM_OEN_51 | 0 | GPIO_51's output enable (PAD_GT0_TX_D2). | |
| 33h (0F67h) | REG0F67 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_51 | 7 | GPIO_51's PAD PS. | |
| | GPIO_PM_PAD_PE_51 | 6 | GPIO_51's PAD PE. | |
| | GPIO_PM_PAD_DRV1_51 | 5 | GPIO_51's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_51 | 4 | GPIO_51's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_51 | 1 | GPIO_51's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_51 | 0 | GPIO_51's FIQ final status for edge wake-up source. | |
| 34h (0F68h) | REG0F68 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_52 | 7 | GPIO_52's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_52 | 6 | GPIO_52's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_52 | 5 | GPIO_52's FIQ force for edge wake-up source. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | GPIO_PM_WK_FIQ_MASK_52 | 4 | GPIO_52's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_52 | 3 | GPIO_52's glitch remover enable. | |
| | GPIO_PM_IN_52 | 2 | GPIO_52's input. | |
| | GPIO_PM_OUT_52 | 1 | GPIO_52's output. | |
| | GPIO_PM_OEN_52 | 0 | GPIO_52's output enable (PAD_GT0_TX_D3). | |
| 34h (0F69h) | REG0F69 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_52 | 7 | GPIO_52's PAD PS. | |
| | GPIO_PM_PAD_PE_52 | 6 | GPIO_52's PAD PE. | |
| | GPIO_PM_PAD_DRV1_52 | 5 | GPIO_52's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_52 | 4 | GPIO_52's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_52 | 1 | GPIO_52's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_52 | 0 | GPIO_52's FIQ final status for edge wake-up source. | |
| 35h (0F6Ah) | REG0F6A | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_53 | 7 | GPIO_53's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_53 | 6 | GPIO_53's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_53 | 5 | GPIO_53's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_53 | 4 | GPIO_53's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_53 | 3 | GPIO_53's glitch remover enable. | |
| | GPIO_PM_IN_53 | 2 | GPIO_53's input. | |
| | GPIO_PM_OUT_53 | 1 | GPIO_53's output. | |
| | GPIO_PM_OEN_53 | 0 | GPIO_53's output enable (PAD_GT1_MDC). | |
| 35h (0F6Bh) | REG0F6B | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_53 | 7 | GPIO_53's PAD PS. | |
| | GPIO_PM_PAD_PE_53 | 6 | GPIO_53's PAD PE. | |
| | GPIO_PM_PAD_DRV1_53 | 5 | GPIO_53's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_53 | 4 | GPIO_53's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_ST | 1 | GPIO_53's FIQ raw status for edge wake-up source. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | ATUS_53 | | | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_53 | 0 | GPIO_53's FIQ final status for edge wake-up source. | |
| 36h (0F6Ch) | REG0F6C | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_54 | 7 | GPIO_54's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_54 | 6 | GPIO_54's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_54 | 5 | GPIO_54's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_54 | 4 | GPIO_54's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_54 | 3 | GPIO_54's glitch remover enable. | |
| | GPIO_PM_IN_54 | 2 | GPIO_54's input. | |
| | GPIO_PM_OUT_54 | 1 | GPIO_54's output. | |
| | GPIO_PM_OEN_54 | 0 | GPIO_54's output enable (PAD_GT1_MDIO). | |
| 36h (0F6Dh) | REG0F6D | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_54 | 7 | GPIO_54's PAD PS. | |
| | GPIO_PM_PAD_PE_54 | 6 | GPIO_54's PAD PE. | |
| | GPIO_PM_PAD_DRV1_54 | 5 | GPIO_54's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_54 | 4 | GPIO_54's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_54 | 1 | GPIO_54's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_54 | 0 | GPIO_54's FIQ final status for edge wake-up source. | |
| 37h (0F6Eh) | REG0F6E | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_55 | 7 | GPIO_55's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_55 | 6 | GPIO_55's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_55 | 5 | GPIO_55's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_55 | 4 | GPIO_55's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_55 | 3 | GPIO_55's glitch remover enable. | |
| | GPIO_PM_IN_55 | 2 | GPIO_55's input. | |
| | GPIO_PM_OUT_55 | 1 | GPIO_55's output. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | GPIO_PM_OEN_55 | 0 | GPIO_55's output enable (PAD_GT1_RX_CLK). | |
| 37h (0F6Fh) | REG0F6F | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_55 | 7 | GPIO_55's PAD PS. | |
| | GPIO_PM_PAD_PE_55 | 6 | GPIO_55's PAD PE. | |
| | GPIO_PM_PAD_DRV1_55 | 5 | GPIO_55's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_55 | 4 | GPIO_55's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_55 | 1 | GPIO_55's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_55 | 0 | GPIO_55's FIQ final status for edge wake-up source. | |
| 38h (0F70h) | REG0F70 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_56 | 7 | GPIO_56's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_56 | 6 | GPIO_56's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_56 | 5 | GPIO_56's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_56 | 4 | GPIO_56's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_56 | 3 | GPIO_56's glitch remover enable. | |
| | GPIO_PM_IN_56 | 2 | GPIO_56's input. | |
| | GPIO_PM_OUT_56 | 1 | GPIO_56's output. | |
| | GPIO_PM_OEN_56 | 0 | GPIO_56's output enable (PAD_GT1_RX_CTL). | |
| 38h (0F71h) | REG0F71 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_56 | 7 | GPIO_56's PAD PS. | |
| | GPIO_PM_PAD_PE_56 | 6 | GPIO_56's PAD PE. | |
| | GPIO_PM_PAD_DRV1_56 | 5 | GPIO_56's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_56 | 4 | GPIO_56's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_56 | 1 | GPIO_56's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_56 | 0 | GPIO_56's FIQ final status for edge wake-up source. | |
| 39h (0F72h) | REG0F72 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_57 | 7 | GPIO_57's FIQ polarity for edge wake-up source. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | GPIO_PM_WK_FIQ_CLR_57 | 6 | GPIO_57's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_57 | 5 | GPIO_57's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_57 | 4 | GPIO_57's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_57 | 3 | GPIO_57's glitch remover enable. | |
| | GPIO_PM_IN_57 | 2 | GPIO_57's input. | |
| | GPIO_PM_OUT_57 | 1 | GPIO_57's output. | |
| | GPIO_PM_OEN_57 | 0 | GPIO_57's output enable (PAD_GT1_RX_D0). | |
| 39h (0F73h) | REG0F73 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_57 | 7 | GPIO_57's PAD PS. | |
| | GPIO_PM_PAD_PE_57 | 6 | GPIO_57's PAD PE. | |
| | GPIO_PM_PAD_DRV1_57 | 5 | GPIO_57's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_57 | 4 | GPIO_57's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_57 | 1 | GPIO_57's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_57 | 0 | GPIO_57's FIQ final status for edge wake-up source. | |
| 3Ah (0F74h) | REG0F74 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_58 | 7 | GPIO_58's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_58 | 6 | GPIO_58's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_58 | 5 | GPIO_58's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_58 | 4 | GPIO_58's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_58 | 3 | GPIO_58's glitch remover enable. | |
| | GPIO_PM_IN_58 | 2 | GPIO_58's input. | |
| | GPIO_PM_OUT_58 | 1 | GPIO_58's output. | |
| | GPIO_PM_OEN_58 | 0 | GPIO_58's output enable (PAD_GT1_RX_D1). | |
| 3Ah (0F75h) | REG0F75 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_58 | 7 | GPIO_58's PAD PS. | |
| | GPIO_PM_PAD_PE_58 | 6 | GPIO_58's PAD PE. | |
| | GPIO_PM_PAD_DRV1_58 | 5 | GPIO_58's PAD DRV1. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | GPIO_PM_PAD_DRV0_58 | 4 | GPIO_58's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_58 | 1 | GPIO_58's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_58 | 0 | GPIO_58's FIQ final status for edge wake-up source. | |
| 3Bh (0F76h) | REG0F76 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_59 | 7 | GPIO_59's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_59 | 6 | GPIO_59's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_59 | 5 | GPIO_59's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_59 | 4 | GPIO_59's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_59 | 3 | GPIO_59's glitch remover enable. | |
| | GPIO_PM_IN_59 | 2 | GPIO_59's input. | |
| | GPIO_PM_OUT_59 | 1 | GPIO_59's output. | |
| | GPIO_PM_OEN_59 | 0 | GPIO_59's output enable (PAD_GT1_RX_D2). | |
| 3Bh (0F77h) | REG0F77 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_59 | 7 | GPIO_59's PAD PS. | |
| | GPIO_PM_PAD_PE_59 | 6 | GPIO_59's PAD PE. | |
| | GPIO_PM_PAD_DRV1_59 | 5 | GPIO_59's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_59 | 4 | GPIO_59's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_59 | 1 | GPIO_59's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_59 | 0 | GPIO_59's FIQ final status for edge wake-up source. | |
| 3Ch (0F78h) | REG0F78 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_60 | 7 | GPIO_60's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_60 | 6 | GPIO_60's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_60 | 5 | GPIO_60's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_60 | 4 | GPIO_60's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_60 | 3 | GPIO_60's glitch remover enable. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | GPIO_PM_IN_60 | 2 | GPIO_60's input. | |
| | GPIO_PM_OUT_60 | 1 | GPIO_60's output. | |
| | GPIO_PM_OEN_60 | 0 | GPIO_60's output enable (PAD_GT1_RX_D3). | |
| 3Ch (0F79h) | REG0F79 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_60 | 7 | GPIO_60's PAD PS. | |
| | GPIO_PM_PAD_PE_60 | 6 | GPIO_60's PAD PE. | |
| | GPIO_PM_PAD_DRV1_60 | 5 | GPIO_60's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_60 | 4 | GPIO_60's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_60 | 1 | GPIO_60's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_60 | 0 | GPIO_60's FIQ final status for edge wake-up source. | |
| 3Dh (0F7Ah) | REG0F7A | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_61 | 7 | GPIO_61's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_61 | 6 | GPIO_61's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_61 | 5 | GPIO_61's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_61 | 4 | GPIO_61's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_61 | 3 | GPIO_61's glitch remover enable. | |
| | GPIO_PM_IN_61 | 2 | GPIO_61's input. | |
| | GPIO_PM_OUT_61 | 1 | GPIO_61's output. | |
| | GPIO_PM_OEN_61 | 0 | GPIO_61's output enable (PAD_GT1_TX_CLK). | |
| 3Dh (0F7Bh) | REG0F7B | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_61 | 7 | GPIO_61's PAD PS. | |
| | GPIO_PM_PAD_PE_61 | 6 | GPIO_61's PAD PE. | |
| | GPIO_PM_PAD_DRV1_61 | 5 | GPIO_61's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_61 | 4 | GPIO_61's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_61 | 1 | GPIO_61's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_61 | 0 | GPIO_61's FIQ final status for edge wake-up source. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| 3Eh (0F7Ch) | REG0F7C | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_62 | 7 | GPIO_62's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_62 | 6 | GPIO_62's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_62 | 5 | GPIO_62's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_62 | 4 | GPIO_62's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_62 | 3 | GPIO_62's glitch remover enable. | |
| | GPIO_PM_IN_62 | 2 | GPIO_62's input. | |
| | GPIO_PM_OUT_62 | 1 | GPIO_62's output. | |
| | GPIO_PM_OEN_62 | 0 | GPIO_62's output enable (PAD_GT1_TX_CTL). | |
| 3Eh (0F7Dh) | REG0F7D | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_62 | 7 | GPIO_62's PAD PS. | |
| | GPIO_PM_PAD_PE_62 | 6 | GPIO_62's PAD PE. | |
| | GPIO_PM_PAD_DRV1_62 | 5 | GPIO_62's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_62 | 4 | GPIO_62's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_62 | 1 | GPIO_62's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_62 | 0 | GPIO_62's FIQ final status for edge wake-up source. | |
| 3Fh (0F7Eh) | REG0F7E | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_63 | 7 | GPIO_63's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_63 | 6 | GPIO_63's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_63 | 5 | GPIO_63's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_63 | 4 | GPIO_63's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_63 | 3 | GPIO_63's glitch remover enable. | |
| | GPIO_PM_IN_63 | 2 | GPIO_63's input. | |
| | GPIO_PM_OUT_63 | 1 | GPIO_63's output. | |
| | GPIO_PM_OEN_63 | 0 | GPIO_63's output enable (PAD_GT1_TX_D0). | |
| 3Fh (0F7Fh) | REG0F7F | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_63 | 7 | GPIO_63's PAD PS. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | GPIO_PM_PAD_PE_63 | 6 | GPIO_63's PAD PE. | |
| | GPIO_PM_PAD_DRV1_63 | 5 | GPIO_63's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_63 | 4 | GPIO_63's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_63 | 1 | GPIO_63's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_63 | 0 | GPIO_63's FIQ final status for edge wake-up source. | |
| 40h (0F80h) | REG0F80 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_64 | 7 | GPIO_64's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_64 | 6 | GPIO_64's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_64 | 5 | GPIO_64's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_64 | 4 | GPIO_64's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_64 | 3 | GPIO_64's glitch remover enable. | |
| | GPIO_PM_IN_64 | 2 | GPIO_64's input. | |
| | GPIO_PM_OUT_64 | 1 | GPIO_64's output. | |
| | GPIO_PM_OEN_64 | 0 | GPIO_64's output enable (PAD_GT1_TX_D1). | |
| 40h (0F81h) | REG0F81 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_64 | 7 | GPIO_64's PAD PS. | |
| | GPIO_PM_PAD_PE_64 | 6 | GPIO_64's PAD PE. | |
| | GPIO_PM_PAD_DRV1_64 | 5 | GPIO_64's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_64 | 4 | GPIO_64's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_64 | 1 | GPIO_64's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_64 | 0 | GPIO_64's FIQ final status for edge wake-up source. | |
| 41h (0F82h) | REG0F82 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_65 | 7 | GPIO_65's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_65 | 6 | GPIO_65's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_65 | 5 | GPIO_65's FIQ force for edge wake-up source. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | GPIO_PM_WK_FIQ_MASK_65 | 4 | GPIO_65's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_65 | 3 | GPIO_65's glitch remover enable. | |
| | GPIO_PM_IN_65 | 2 | GPIO_65's input. | |
| | GPIO_PM_OUT_65 | 1 | GPIO_65's output. | |
| | GPIO_PM_OEN_65 | 0 | GPIO_65's output enable (PAD_GT1_TX_D2). | |
| 41h (0F83h) | REG0F83 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_65 | 7 | GPIO_65's PAD PS. | |
| | GPIO_PM_PAD_PE_65 | 6 | GPIO_65's PAD PE. | |
| | GPIO_PM_PAD_DRV1_65 | 5 | GPIO_65's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_65 | 4 | GPIO_65's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_65 | 1 | GPIO_65's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_65 | 0 | GPIO_65's FIQ final status for edge wake-up source. | |
| 42h (0F84h) | REG0F84 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_66 | 7 | GPIO_66's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_66 | 6 | GPIO_66's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_66 | 5 | GPIO_66's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_66 | 4 | GPIO_66's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_66 | 3 | GPIO_66's glitch remover enable. | |
| | GPIO_PM_IN_66 | 2 | GPIO_66's input. | |
| | GPIO_PM_OUT_66 | 1 | GPIO_66's output. | |
| | GPIO_PM_OEN_66 | 0 | GPIO_66's output enable (PAD_GT1_TX_D3). | |
| 42h (0F85h) | REG0F85 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_66 | 7 | GPIO_66's PAD PS. | |
| | GPIO_PM_PAD_PE_66 | 6 | GPIO_66's PAD PE. | |
| | GPIO_PM_PAD_DRV1_66 | 5 | GPIO_66's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_66 | 4 | GPIO_66's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_ST | 1 | GPIO_66's FIQ raw status for edge wake-up source. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | ATUS_66 | | | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_66 | 0 | GPIO_66's FIQ final status for edge wake-up source. | |
| 43h (0F86h) | REG0F86 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_67 | 7 | GPIO_67's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_67 | 6 | GPIO_67's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_67 | 5 | GPIO_67's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_67 | 4 | GPIO_67's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_67 | 3 | GPIO_67's glitch remover enable. | |
| | GPIO_PM_IN_67 | 2 | GPIO_67's input. | |
| | GPIO_PM_OUT_67 | 1 | GPIO_67's output. | |
| | GPIO_PM_OEN_67 | 0 | GPIO_67's output enable (PAD_PM_HDMI_CEC). | |
| 43h (0F87h) | REG0F87 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_67 | 7 | GPIO_67's PAD PS. | |
| | GPIO_PM_PAD_PE_67 | 6 | GPIO_67's PAD PE. | |
| | GPIO_PM_PAD_DRV1_67 | 5 | GPIO_67's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_67 | 4 | GPIO_67's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_67 | 1 | GPIO_67's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_67 | 0 | GPIO_67's FIQ final status for edge wake-up source. | |
| 44h (0F88h) | REG0F88 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_68 | 7 | GPIO_68's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_68 | 6 | GPIO_68's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_68 | 5 | GPIO_68's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_68 | 4 | GPIO_68's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_68 | 3 | GPIO_68's glitch remover enable. | |
| | GPIO_PM_IN_68 | 2 | GPIO_68's input. | |
| | GPIO_PM_OUT_68 | 1 | GPIO_68's output. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | GPIO_PM_OEN_68 | 0 | GPIO_68's output enable (PAD_PM_SPI_WPZ). | |
| 44h (0F89h) | REG0F89 | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_68 | 7 | GPIO_68's PAD PS. | |
| | GPIO_PM_PAD_PE_68 | 6 | GPIO_68's PAD PE. | |
| | GPIO_PM_PAD_DRV1_68 | 5 | GPIO_68's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_68 | 4 | GPIO_68's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_68 | 1 | GPIO_68's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_68 | 0 | GPIO_68's FIQ final status for edge wake-up source. | |
| 45h (0F8Ah) | REG0F8A | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_69 | 7 | GPIO_69's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_69 | 6 | GPIO_69's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_69 | 5 | GPIO_69's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_69 | 4 | GPIO_69's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_69 | 3 | GPIO_69's glitch remover enable. | |
| | GPIO_PM_IN_69 | 2 | GPIO_69's input. | |
| | GPIO_PM_OUT_69 | 1 | GPIO_69's output. | |
| | GPIO_PM_OEN_69 | 0 | GPIO_69's output enable (PAD_PM_SPI_HOLDZ). | |
| 45h (0F8Bh) | REG0F8B | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_69 | 7 | GPIO_69's PAD PS. | |
| | GPIO_PM_PAD_PE_69 | 6 | GPIO_69's PAD PE. | |
| | GPIO_PM_PAD_DRV1_69 | 5 | GPIO_69's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_69 | 4 | GPIO_69's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_69 | 1 | GPIO_69's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_69 | 0 | GPIO_69's FIQ final status for edge wake-up source. | |
| 46h (0F8Ch) | REG0F8C | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_70 | 7 | GPIO_70's FIQ polarity for edge wake-up source. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | GPIO_PM_WK_FIQ_CLR_70 | 6 | GPIO_70's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_70 | 5 | GPIO_70's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_70 | 4 | GPIO_70's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_70 | 3 | GPIO_70's glitch remover enable. | |
| | GPIO_PM_IN_70 | 2 | GPIO_70's input. | |
| | GPIO_PM_OUT_70 | 1 | GPIO_70's output. | |
| | GPIO_PM_OEN_70 | 0 | GPIO_70's output enable (PAD_PM_SPI_RSTZ). | |
| 46h (0F8Dh) | REG0F8D | 7:0 | Default : 0x00 | Access : RO, R/W |
| | GPIO_PM_PAD_PS_70 | 7 | GPIO_70's PAD PS. | |
| | GPIO_PM_PAD_PE_70 | 6 | GPIO_70's PAD PE. | |
| | GPIO_PM_PAD_DRV1_70 | 5 | GPIO_70's PAD DRV1. | |
| | GPIO_PM_PAD_DRV0_70 | 4 | GPIO_70's PAD DRV0. | |
| | - | 3:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_70 | 1 | GPIO_70's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_70 | 0 | GPIO_70's FIQ final status for edge wake-up source. | |
| 47h (0F8Eh) | REG0F8E | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_71 | 7 | GPIO_71's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_71 | 6 | GPIO_71's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_71 | 5 | GPIO_71's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_71 | 4 | GPIO_71's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_71 | 3 | GPIO_71's glitch remover enable. | |
| | GPIO_PM_IN_71 | 2 | GPIO_71's input. | |
| | GPIO_PM_OUT_71 | 1 | GPIO_71's output. | |
| | GPIO_PM_OEN_71 | 0 | GPIO_71's output enable (PAD_PM_SD_CDZ). | |
| 47h (0F8Fh) | REG0F8F | 7:0 | Default : 0x00 | Access : RO |
| | - | 7:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_71 | 1 | GPIO_71's FIQ raw status for edge wake-up source. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_71 | 0 | GPIO_71's FIQ final status for edge wake-up source. | |
| 48h (0F90h) | REG0F90 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_72 | 7 | GPIO_72's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_72 | 6 | GPIO_72's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_72 | 5 | GPIO_72's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_72 | 4 | GPIO_72's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_72 | 3 | GPIO_72's glitch remover enable. | |
| | GPIO_PM_IN_72 | 2 | GPIO_72's input. | |
| | GPIO_PM_OUT_72 | 1 | GPIO_72's output. | |
| | GPIO_PM_OEN_72 | 0 | GPIO_72's output enable (PAD_VID0). | |
| 48h (0F91h) | REG0F91 | 7:0 | Default : 0x00 | Access : RO |
| | - | 7:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_72 | 1 | GPIO_72's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_72 | 0 | GPIO_72's FIQ final status for edge wake-up source. | |
| 49h (0F92h) | REG0F92 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_73 | 7 | GPIO_73's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_73 | 6 | GPIO_73's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_73 | 5 | GPIO_73's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_73 | 4 | GPIO_73's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_73 | 3 | GPIO_73's glitch remover enable. | |
| | GPIO_PM_IN_73 | 2 | GPIO_73's input. | |
| | GPIO_PM_OUT_73 | 1 | GPIO_73's output. | |
| | GPIO_PM_OEN_73 | 0 | GPIO_73's output enable (PAD_VID1). | |
| 49h (0F93h) | REG0F93 | 7:0 | Default : 0x00 | Access : RO |
| | - | 7:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_73 | 1 | GPIO_73's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_S | 0 | GPIO_73's FIQ final status for edge wake-up source. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| | TATUS_73 | | | |
| 4Ah (0F94h) | REG0F94 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_74 | 7 | GPIO_74's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_74 | 6 | GPIO_74's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_74 | 5 | GPIO_74's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_74 | 4 | GPIO_74's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_74 | 3 | GPIO_74's glitch remover enable. | |
| | GPIO_PM_IN_74 | 2 | GPIO_74's input. | |
| | GPIO_PM_OUT_74 | 1 | GPIO_74's output. | |
| | GPIO_PM_OEN_74 | 0 | GPIO_74's output enable (PAD_LED0). | |
| 4Ah (0F95h) | REG0F95 | 7:0 | Default : 0x00 | Access : RO |
| | - | 7:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_74 | 1 | GPIO_74's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_74 | 0 | GPIO_74's FIQ final status for edge wake-up source. | |
| 4Bh (0F96h) | REG0F96 | 7:0 | Default : 0x11 | Access : RO, R/W, WO |
| | GPIO_PM_WK_FIQ_POL_75 | 7 | GPIO_75's FIQ polarity for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_CLR_75 | 6 | GPIO_75's FIQ clear for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FORCE_75 | 5 | GPIO_75's FIQ force for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_MASK_75 | 4 | GPIO_75's FIQ mask for edge wake-up source. | |
| | GPIO_PM_GLHRM_EN_75 | 3 | GPIO_75's glitch remover enable. | |
| | GPIO_PM_IN_75 | 2 | GPIO_75's input. | |
| | GPIO_PM_OUT_75 | 1 | GPIO_75's output. | |
| | GPIO_PM_OEN_75 | 0 | GPIO_75's output enable (PAD_LED1). | |
| 4Bh (0F97h) | REG0F97 | 7:0 | Default : 0x00 | Access : RO |
| | - | 7:2 | Reserved. | |
| | GPIO_PM_WK_FIQ_RAW_STATUS_75 | 1 | GPIO_75's FIQ raw status for edge wake-up source. | |
| | GPIO_PM_WK_FIQ_FINAL_STATUS_75 | 0 | GPIO_75's FIQ final status for edge wake-up source. | |

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| PM_GPIO Register (Bank = 0F) | | | | |
|---|---|---|---|---|
| Index (Absolute) | Mnemonic | Bit | Description | |
| 7Eh (0FFCh) | REG0FFC | 7:0 | Default : 0x00 | Access : R/W |
| | RESERVE5[7:0] | 7:0 | RESERVE5 (for HW ECO ONLY).<br>[1:0]: for GCR_PWRGD_LVL_H.<br>[15:2]: reserved. | |
| 7Eh (0FFDh) | REG0FFD | 7:0 | Default : 0x00 | Access : R/W |
| | RESERVE5[15:8] | 7:0 | See description of '0FFCh'. | |
| 7Fh (0FFEh) | REG0FFE | 7:0 | Default : 0xFF | Access : R/W |
| | RESERVE6[7:0] | 7:0 | RESERVE6 (for HW ECO ONLY). | |
| 7Fh (0FFFh) | REG0FFF | 7:0 | Default : 0xFF | Access : R/W |
| | RESERVE6[15:8] | 7:0 | See description of '0FFEh'. | |

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