SSD202D
SAR Module Description

1. AC/DC SPECIFICATION

1.1. Overview

Parameter	Min	Typ	Max	Unit
SAR ADC Input	0		AVDD_NODIE	V

SAR(Successive Approximation Register) ADC are a common configuration for medium to high resolution ADC with sampling rates below 5Msps. The resolution of SAR ADC is generally 8-16 bits. Features such as low power consumption and small size. This ASIC contain three SAR ports, the precision is 10bit.

1.2. Function Description

The SAR module has the following features:

- Supports ioctl interface to initialize SAR and get SAR_ADC value

1.3. Operating Mode

The precision of SAR is 10bit, so the range of the obtained value is between 0~0x3ff. For example, if the reference voltage is 3.3V, the obtained value is 0x3DD, and the obtained voltage is 0x3DD/0x3FF * 3.3 = 3.19V.

2. REGISTER DESCRIPTION

2.1. PM_SAR Register (Bank = 14)

PM_SAR Register (Bank = 14)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (1400h)	REG1400	7:0	Default : 0x40	Access : R/W
	SAR_START	7	SAR start signal.	
	SAR_PD	6	SAR digital power down.	
	SAR_MODE	5	Select SAR digital operation mode. 0: One-shot. 1: Freerun.	
	SINGLE	4	Enable SINGLE channel mode. 0: Disable. 1: Enable.	
	KEYPAD_LEVEL	3	Level of keypad.	
	SAR_SINGLE_CH[2:0]	2:0	Select channel for single channel mode.	
00h (1401h)	REG1401	7:0	Default : 0x09	Access : R/W
	-	7:4	Reserved.	
	SAR_8CH_EN	3	1: SAR 8 channel. 0: SAR 4 channel.	
	SAR_SEL	2	SAR selection.	
	SAR_FREERUN	1	SAR atop freerun mode. 0: Controlled by digital (default). 1: Freerun.	
	SARADC_PD	0	SAR atop power down. 1: Power down. 0: Enable SAR atop.	
01h (1402h)	REG1402	7:0	Default : 0x00	Access : R/W
	CKSAMP_PRD[7:0]	7:0	CKSAMP_PRD.	
02h (1404h)	REG1404	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	GCR_SAR_CH8_MUXSEL[2:0]	2:0	SAR CH8 input MUX selection.	
02h (1405h)	REG1405	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	

PM_SAR Register (Bank = 14)				
Index (Absolute)	Mnemonic	Bit	Description	
	GCR_SAR_CH8_EN	0	0: SAR channel = CH0~CH7 decided by GCR_SAR_CHSEL. 1: SAR channel = CH8.	
10h (1420h)	REG1420	7:0	Default : 0x00	Access : R/W
	PM_DMY[7:0]	7:0		
11h (1422h)	REG1422	7:0	Default : 0x3F	Access : R/W
	-	7:6	Reserved.	
	SAR_AISEL[5:0]	5:0	Pad GPIO/Ain switch: 1: Analog input. 0: GPIO.	
11h (1423h)	REG1423	7:0	Default : 0x3F	Access : R/W
	-	7:6	Reserved.	
	OEN_SAR_GPIO[5:0]	5:0	Output enable for GPIO pad. 0: Enable. 1: Disable.	
12h (1424h)	REG1424	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	I_SAR_GPIO[5:0]	5:0	Output data for GPIO pad.	
12h (1425h)	REG1425	7:0	Default : 0x00	Access : RO
	-	7:6	Reserved.	
	C_SAR_GPIO[5:0]	5:0	Input data for GPIO pad.	
13h (1426h)	REG1426	7:0	Default : 0x00	Access : R/W
	SAR_TEST[7:0]	7:0	SAR ADC test mode control.	
13h (1427h)	REG1427	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SAR_TEST[9:8]	1:0	See description of '1426h'.	
14h (1428h)	REG1428	7:0	Default : 0xFF	Access : R/W
	SAR_INT_MASK[7:0]	7:0	Interrupt mask for sar_int. 0: Enable. 1: Disable.	
14h (1429h)	REG1429	7:0	Default : 0x01	Access : R/W
	-	7:1	Reserved.	
	SAR_INT_MASK[8]	0	See description of '1428h'.	
15h (142Ah)	REG142A	7:0	Default : 0x00	Access : WO
	SAR_INT_CLR[7:0]	7:0	Interrupt clear for sar_int.	

PM_SAR Register (Bank = 14)				
Index (Absolute)	Mnemonic	Bit	Description	
15h (142Bh)	REG142B	7:0	Default : 0x00	Access : WO
	-	7:1	Reserved.	
	SAR_INT_CLR[8]	0	See description of '142Ah'.	
16h (142Ch)	REG142C	7:0	Default : 0x00	Access : R/W
	SAR_INT_FORCE[7:0]	7:0	Force interrupt for sar_int.	
16h (142Dh)	REG142D	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	SAR_INT_FORCE[8]	0	See description of '142Ch'.	
17h (142Eh)	REG142E	7:0	Default : 0x00	Access : RO
	SAR_INT_STATUS[7:0]	7:0	Status of sar_int.	
17h (142Fh)	REG142F	7:0	Default : 0x00	Access : RO
	-	7:1	Reserved.	
	SAR_INT_STATUS[8]	0	See description of '142Eh'.	
18h (1430h)	REG1430	7:0	Default : 0x00	Access : RO
	-	7:2	Reserved.	
	SAR_RDY	1	SAR ready signal.	
	CMP_OUT	0	SAR compare out signal.	
19h (1432h)	REG1432	7:0	Default : 0x1F	Access : R/W
	SAR_CH8_REF_V_SEL	7	Channel 8 reference voltage select (0: 2.0V, 1: 3.3V).	
	SAR_CH7_REF_V_SEL	6	Channel 7 reference voltage select (0: 2.0V, 1: 3.3V).	
	SAR_CH6_REF_V_SEL	5	Channel 6 reference voltage select (0: 2.0V, 1: 3.3V).	
	SAR_CH5_REF_V_SEL	4	Channel 5 reference voltage select (0: 2.0V, 1: 3.3V).	
	SAR_CH4_REF_V_SEL	3	Channel 4 reference voltage select (0: 2.0V, 1: 3.3V).	
	SAR_CH3_REF_V_SEL	2	Channel 3 reference voltage select (0: 2.0V, 1: 3.3V).	
	SAR_CH2_REF_V_SEL	1	Channel 2 reference voltage select (0: 2.0V, 1: 3.3V).	
	SAR_CH1_REF_V_SEL	0	Channel 1 reference voltage select (0: 2.0V, 1: 3.3V).	
20h (1440h)	REG1440	7:0	Default : 0x00	Access : R/W
	SAR_CH1_UPB[7:0]	7:0	Channel 1 upper bound.	
20h (1441h)	REG1441	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SAR_CH1_UPB[9:8]	1:0	See description of '1440h'.	
21h (1442h)	REG1442	7:0	Default : 0x00	Access : R/W
	SAR_CH2_UPB[7:0]	7:0	Channel 2 upper bound.	

PM_SAR Register (Bank = 14)				
Index (Absolute)	Mnemonic	Bit	Description	
21h (1443h)	REG1443	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SAR_CH2_UPB[9:8]	1:0	See description of '1442h'.	
22h (1444h)	REG1444	7:0	Default : 0x00	Access : R/W
	SAR_CH3_UPB[7:0]	7:0	Channel 3 upper bound.	
22h (1445h)	REG1445	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SAR_CH3_UPB[9:8]	1:0	See description of '1444h'.	
23h (1446h)	REG1446	7:0	Default : 0x00	Access : R/W
	SAR_CH4_UPB[7:0]	7:0	Channel 4 upper bound.	
23h (1447h)	REG1447	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SAR_CH4_UPB[9:8]	1:0	See description of '1446h'.	
24h (1448h)	REG1448	7:0	Default : 0x00	Access : R/W
	SAR_CH5_UPB[7:0]	7:0	Channel 5 upper bound.	
24h (1449h)	REG1449	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SAR_CH5_UPB[9:8]	1:0	See description of '1448h'.	
25h (144Ah)	REG144A	7:0	Default : 0x00	Access : R/W
	SAR_CH6_UPB[7:0]	7:0	Channel 6 upper bound.	
25h (144Bh)	REG144B	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SAR_CH6_UPB[9:8]	1:0	See description of '144Ah'.	
26h (144Ch)	REG144C	7:0	Default : 0x00	Access : R/W
	SAR_CH7_UPB[7:0]	7:0	Channel 7 upper bound.	
26h (144Dh)	REG144D	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SAR_CH7_UPB[9:8]	1:0	See description of '144Ch'.	
27h (144Eh)	REG144E	7:0	Default : 0x00	Access : R/W
	SAR_CH8_UPB[7:0]	7:0	Channel 8 upper bound.	
27h (144Fh)	REG144F	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SAR_CH8_UPB[9:8]	1:0	See description of '144Eh'.	

PM_SAR Register (Bank = 14)				
Index (Absolute)	Mnemonic	Bit	Description	
30h (1460h)	REG1460	7:0	Default : 0x00	Access : R/W
	SAR_CH1_LOB[7:0]	7:0	Channel 1 lower bound.	
30h (1461h)	REG1461	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SAR_CH1_LOB[9:8]	1:0	See description of '1460h'.	
31h (1462h)	REG1462	7:0	Default : 0x00	Access : R/W
	SAR_CH2_LOB[7:0]	7:0	Channel 2 lower bound.	
31h (1463h)	REG1463	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SAR_CH2_LOB[9:8]	1:0	See description of '1462h'.	
32h (1464h)	REG1464	7:0	Default : 0x00	Access : R/W
	SAR_CH3_LOB[7:0]	7:0	Channel 3 lower bound.	
32h (1465h)	REG1465	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SAR_CH3_LOB[9:8]	1:0	See description of '1464h'.	
33h (1466h)	REG1466	7:0	Default : 0x00	Access : R/W
	SAR_CH4_LOB[7:0]	7:0	Channel 4 lower bound.	
33h (1467h)	REG1467	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SAR_CH4_LOB[9:8]	1:0	See description of '1466h'.	
34h (1468h)	REG1468	7:0	Default : 0x00	Access : R/W
	SAR_CH5_LOB[7:0]	7:0	Channel 5 lower bound.	
34h (1469h)	REG1469	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SAR_CH5_LOB[9:8]	1:0	See description of '1468h'.	
35h (146Ah)	REG146A	7:0	Default : 0x00	Access : R/W
	SAR_CH6_LOB[7:0]	7:0	Channel 6 lower bound.	
35h (146Bh)	REG146B	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SAR_CH6_LOB[9:8]	1:0	See description of '146Ah'.	
36h (146Ch)	REG146C	7:0	Default : 0x00	Access : R/W
	SAR_CH7_LOB[7:0]	7:0	Channel 7 lower bound.	
36h	REG146D	7:0	Default : 0x00	Access : R/W

PM_SAR Register (Bank = 14)				
Index (Absolute)	Mnemonic	Bit	Description	
(146Dh)	-	7:2	Reserved.	
	SAR_CH7_LOB[9:8]	1:0	See description of '146Ch'.	
37h (146Eh)	REG146E	7:0	Default : 0x00	Access : R/W
	SAR_CH8_LOB[7:0]	7:0	Channel 8 lower bound.	
37h (146Fh)	REG146F	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SAR_CH8_LOB[9:8]	1:0	See description of '146Eh'.	
40h (1480h)	REG1480	7:0	Default : 0x00	Access : RO
	SAR_ADC_CH1_DATA[7:0]	7:0	SAR ADC output 1.	
40h (1481h)	REG1481	7:0	Default : 0x00	Access : RO
	-	7:2	Reserved.	
	SAR_ADC_CH1_DATA[9:8]	1:0	See description of '1480h'.	
41h (1482h)	REG1482	7:0	Default : 0x00	Access : RO
	SAR_ADC_CH2_DATA[7:0]	7:0	SAR ADC output 2.	
41h (1483h)	REG1483	7:0	Default : 0x00	Access : RO
	-	7:2	Reserved.	
	SAR_ADC_CH2_DATA[9:8]	1:0	See description of '1482h'.	
42h (1484h)	REG1484	7:0	Default : 0x00	Access : RO
	SAR_ADC_CH3_DATA[7:0]	7:0	SAR ADC output 3.	
42h (1485h)	REG1485	7:0	Default : 0x00	Access : RO
	-	7:2	Reserved.	
	SAR_ADC_CH3_DATA[9:8]	1:0	See description of '1484h'.	
43h (1486h)	REG1486	7:0	Default : 0x00	Access : RO
	SAR_ADC_CH4_DATA[7:0]	7:0	SAR ADC output 4.	
43h (1487h)	REG1487	7:0	Default : 0x00	Access : RO
	-	7:2	Reserved.	
	SAR_ADC_CH4_DATA[9:8]	1:0	See description of '1486h'.	
44h (1488h)	REG1488	7:0	Default : 0x00	Access : RO
	SAR_ADC_CH5_DATA[7:0]	7:0	SAR ADC output 5.	
44h (1489h)	REG1489	7:0	Default : 0x00	Access : RO
	-	7:2	Reserved.	
	SAR_ADC_CH5_DATA[9:8]	1:0	See description of '1488h'.	
45h	REG148A	7:0	Default : 0x00	Access : RO

PM_SAR Register (Bank = 14)				
Index (Absolute)	Mnemonic	Bit	Description	
(148Ah)	SAR_ADC_CH6_DATA[7:0]	7:0	SAR ADC output 6.	
45h (148Bh)	REG148B	7:0	Default : 0x00	Access : RO
	-	7:2	Reserved.	
	SAR_ADC_CH6_DATA[9:8]	1:0	See description of '148Ah'.	
46h (148Ch)	REG148C	7:0	Default : 0x00	Access : RO
	SAR_ADC_CH7_DATA[7:0]	7:0	SAR ADC output 7.	
46h (148Dh)	REG148D	7:0	Default : 0x00	Access : RO
	-	7:2	Reserved.	
	SAR_ADC_CH7_DATA[9:8]	1:0	See description of '148Ch'.	
47h (148Eh)	REG148E	7:0	Default : 0x00	Access : RO
	SAR_ADC_CH8_DATA[7:0]	7:0	SAR ADC output 8.	
47h (148Fh)	REG148F	7:0	Default : 0x00	Access : RO
	-	7:2	Reserved.	
	SAR_ADC_CH8_DATA[9:8]	1:0	See description of '148Eh'.	
50h (14A0h)	REG14A0	7:0	Default : 0x0C	Access : R/W
	SMCARD_INT_TIME_CNT_H[3:0]	7:4	Smcard power_good interrupt time count for high pulse.	
	SMCARD_INT_LEVEL	3	Select smcard power_good interrupt level. 1'b0: active low. 1'b1: active high.	
	SMCARD_INT_SEL[2:0]	2:0	Select smcard power_good interrupt from: 3'b000: channel 1. 3'b001: channel 2. 3'b010: channel 3. 3'b011: channel 4. 3'b100: VPLUG_IN_PWRGD of pm_sar_atop.	
50h (14A1h)	REG14A1	7:0	Default : 0x00	Access : RO, R/W
	-	7	Reserved.	
	SMCARD_INT	6	Smcard power_good post interrupt time.	
	SMCARD_INT_PULSE	5	Smcard power_good pre interrupt time count.	
	SMCARD_INT_TIME_CNT_EN	4	Smcard power_good interrupt time count enable.	
	SMCARD_INT_TIME_CNT_L[3:0]	3:0	Smcard power_good interrupt time count for low pulse.	
51h	REG14A2	7:0	Default : 0x0C	Access : R/W

PM_SAR Register (Bank = 14)				
Index (Absolute)	Mnemonic	Bit	Description	
(14A2h)	FCIE_INT_TIME_CNT_H[3:0]	7:4	Fcie power_good interrupt time count for high pulse.	
	FCIE_INT_LEVEL	3	Select fcie power_good interrupt level. 1'b0: active low. 1'b1: active high.	
	FCIE_INT_SEL[2:0]	2:0	Select fcie power_good interrupt from: 3'b000: channel 1. 3'b001: channel 2. 3'b010: channel 3. 3'b011: channel 4. 3'b100: VPLUG_IN_PWRGD of pm_sar_atop.	
51h (14A3h)	REG14A3	7:0	Default : 0x00	Access : RO, R/W
	-	7	Reserved.	
	FCIE_INT	6	Fcie power_good post interrupt time.	
	FCIE_INT_PULSE	5	Fcie power_good pre interrupt time count.	
	FCIE_INT_TIME_CNT_EN	4	Fcie power_good interrupt time count enable.	
	FCIE_INT_TIME_CNT_L[3:0]	3:0	Fcie power_good interrupt time count for low pulse.	
60h (14C0h)	REG14C0	7:0	Default : 0x02	Access : R/W
	-	7:3	Reserved.	
	SAR_INT_DIRECT2TOP_SEL[2:0]	2:0	Select sar_channel interrupt direct connection to intr_ctrl_top. 3'd0: channel 1. 3'd1: channel 2. 3'd2: channel 3. 3'd3: channel 4. 3'd4: channel 5. 3'd5: channel 6. 3'd6: channel 7. 3'd7: channel 8.	
70h (14E0h)	REG14E0	7:0	Default : 0x00	Access : RO
	-	7:4	Reserved.	
	TSEN_PROCESS_CODE[3:0]	3:0	Pm_sar_atop tsensor process code.	

2.2. PM_SAR Register (Bank = 14)

PM_SAR Register (Bank = 14)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (1401h)	REG1401	7:0	Default : 0x00	Access : R/W, WO
	-	7	Reserved.	
	SAR_LOAD_EN	6	Enable load SAR code.	
	-	5	Reserved.	
	SAR_SW_RST	4	Software reset (active high) for sar_top.	
	-	3:0	Reserved.	